

TC74HC590AP, TC74HC590AF

8 – BIT BINARY COUNTER / REGISTER WITH 3 – STATE OUTPUTS

The TC74HC590A is a high speed CMOS 8-BIT COUNTER/REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

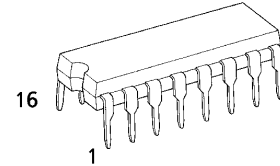
The internal counter counts on the positive going edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{\text{CCKEN}}$) is low. When Counter Clear ($\overline{\text{CCLR}}$) is low, the internal counter is cleared asynchronously to the clock.

Data in the internal counter are loaded into the register at positive going edge of Register Clock (RCK), and the register outputs are controlled by enable input ($\overline{\text{G}}$).

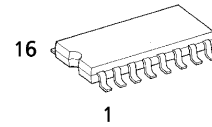
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{\text{MAX}} = 62\text{MHz}(\text{typ.})$ at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Output Drive Capability..... 15 LSTTL Loads For QA~QH
10 LSTTL Loads For $\overline{\text{RCO}}$
- Symmetrical Output Impedance...
 $|I_{\text{OH}}| = I_{\text{OL}} = 6\text{mA}(\text{Min.})$ For QA~QH
 $|I_{\text{OH}}| = I_{\text{OL}} = 4\text{mA}(\text{Min.})$ For $\overline{\text{RCO}}$
- Balanced Propagation Delays..... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS590

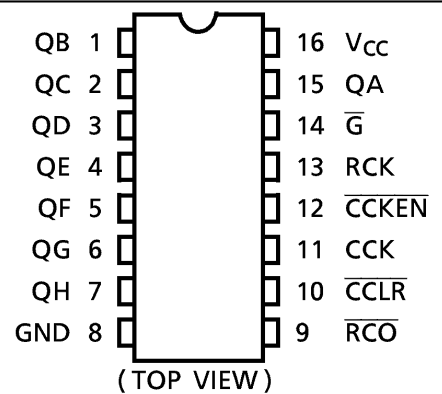


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



TRUTH TABLE

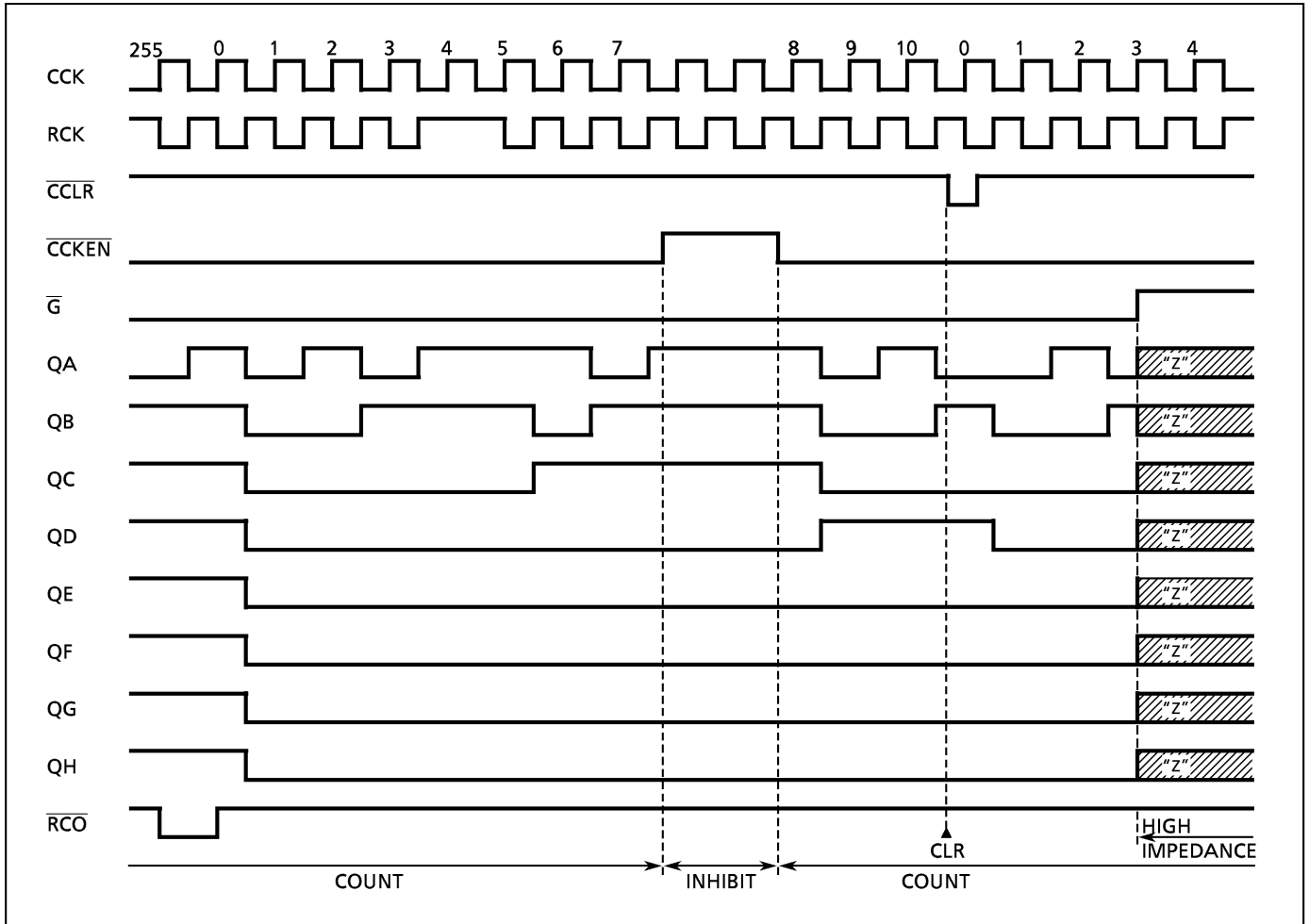
INPUT					FUNCTION
G	RCK	CCLR	CCKEN	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	\uparrow	X	X	X	COUNTER DATA IS STORED INTO REGISTER
X	\downarrow	X	X	X	REGISTER STATE IS NOT CHANGED
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	\uparrow	ADVANCE ONE COUNT
X	X	H	L	\downarrow	NO COUNT
X	X	H	H	X	NO COUNT

X : Don't care

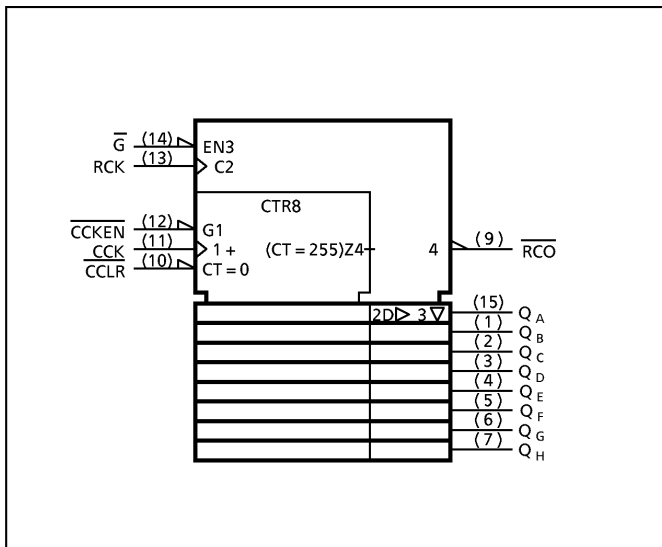
$$\overline{\text{RCO}} = \overline{\text{QA}}' \cdot \overline{\text{QB}}' \cdot \overline{\text{QC}}' \cdot \overline{\text{QD}}' \cdot \overline{\text{QE}}' \cdot \overline{\text{QF}}' \cdot \overline{\text{QG}}' \cdot \overline{\text{QH}}'$$

(QA'~QH' : Internal outputs of the counter)

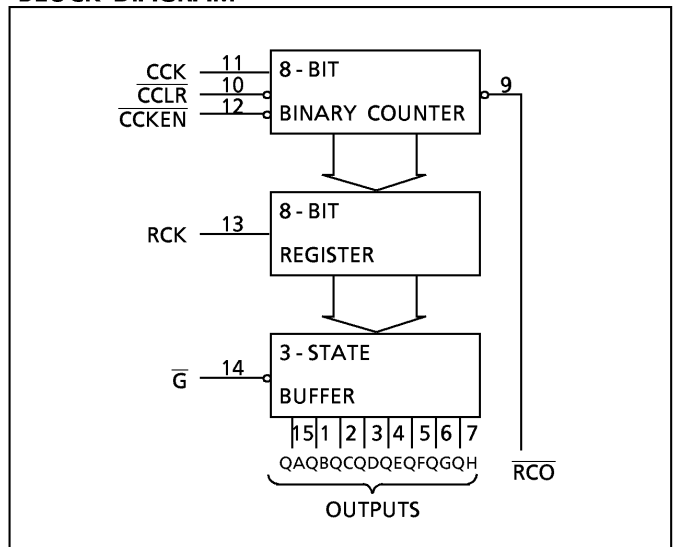
TIMING CHART



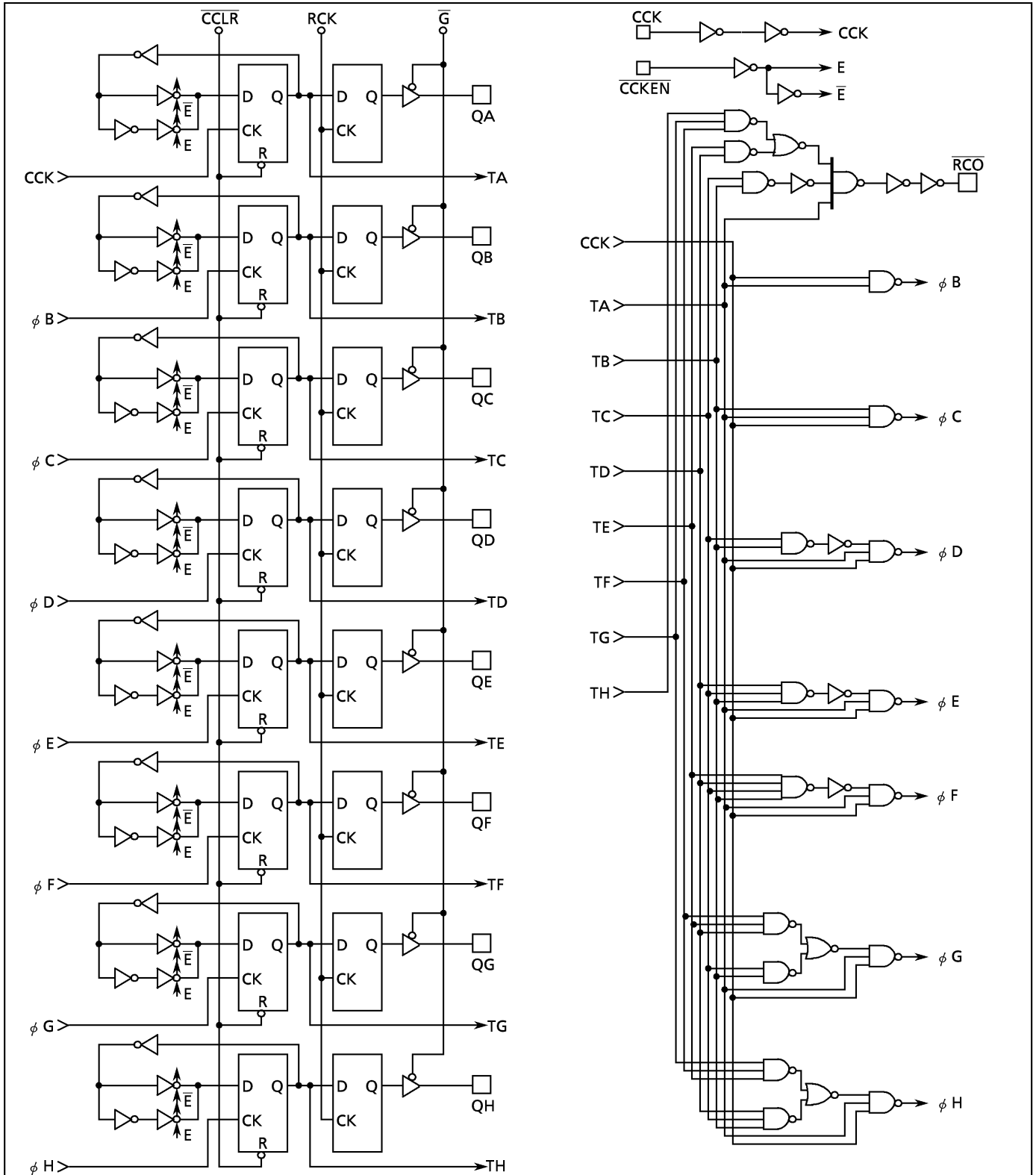
IEC LOGIC SYMBOL



BLOCK DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current (RCO) ($Q_A \sim Q_H$)	I_{OUT}	± 25 ± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V _{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
		R \overline{CO} I _{OH} = -4 mA I _{OH} = -5.2 mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
		QA~QH I _{OH} = -6 mA I _{OH} = -7.8 mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		R \overline{CO} I _{OL} = 4 mA I _{OL} = 5.2 mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
		QA~QH I _{OL} = 6 mA I _{OL} = 7.8 mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	6.0	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	6.0	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input t_r = t_f = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CCK, RCK)	t _{w(H)} t _{w(L)}		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CCLR)	t _{w(L)}		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (CCKEN-CCK)	t _s		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Set-up Time (CCK-RCK)	t _s		2.0	—	200	250	
			4.5	—	40	50	
			6.0	—	34	43	
Minimum Hold Time	t _h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time (CCLR)	t _{rem}		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	33	26	
			6.0	—	39	31	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time ($\overline{\text{RCO}}$)	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time ($\text{CCK} - \overline{\text{RCO}}$)	t_{pLH} t_{pHL}		—	18	28	
Propagation Delay Time ($\text{CCLR} - \overline{\text{RCO}}$)	t_{pLH}		—	20	30	
Maximum Clock Frequency	f_{MAX}		32	62	—	MHz

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
					MIN.	TYP.	MAX.	MIN.	MAX.		
Output Transition Time (Q_n)	t_{TLH} t_{THL}		50	2.0	—	25	60	—	75	ns	
				4.5	—	7	12	—	15		
				6.0	—	6	10	—	13		
Output Transition Time ($\overline{\text{RCO}}$)	t_{TLH} t_{THL}		50	2.0	—	30	75	—	95	ns	
				4.5	—	8	15	—	19		
				6.0	—	7	13	—	16		
Propagation Delay Time ($\text{CCK} - \overline{\text{RCO}}$)	t_{pLH} t_{pHL}		50	2.0	—	75	163	—	205	ns	
				4.5	—	22	33	—	41		
				6.0	—	17	28	—	35		
Propagation Delay Time ($\text{CCLR} - \overline{\text{RCO}}$)	t_{pLH}		50	2.0	—	78	175	—	220	ns	
				4.5	—	23	35	—	44		
				6.0	—	18	30	—	37		
Propagation Delay Time ($\text{RCK} - Q_n$)	t_{pLH} t_{pHL}		50	2.0	—	62	145	—	180	ns	
				4.5	—	19	29	—	36		
				6.0	—	15	25	—	31		
			150	2.0	—	78	185	—	230		ns
				4.5	—	24	37	—	46		
				6.0	—	19	31	—	39		
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1\text{k}\Omega$	50	2.0	—	43	105	—	130	ns	
				4.5	—	14	21	—	26		
				6.0	—	12	18	—	22		
			150	2.0	—	58	150	—	190		ns
				4.5	—	19	30	—	38		
				6.0	—	16	26	—	33		
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1\text{k}\Omega$	50	2.0	—	33	105	—	130	ns	
				4.5	—	16	21	—	26		
				6.0	—	12	18	—	22		
Maximum Clock Frequency	f_{MAX}		50	2.0	6	12	—	5	—	MHz	
				4.5	30	51	—	24	—		
				6.0	35	80	—	28	—		
Input Capacitance	C_{IN}				—	5	10	—	10	pF	
Power Dissipation Capacitance	$C_{\text{PD}} (1)$				—	34	—	—	—		

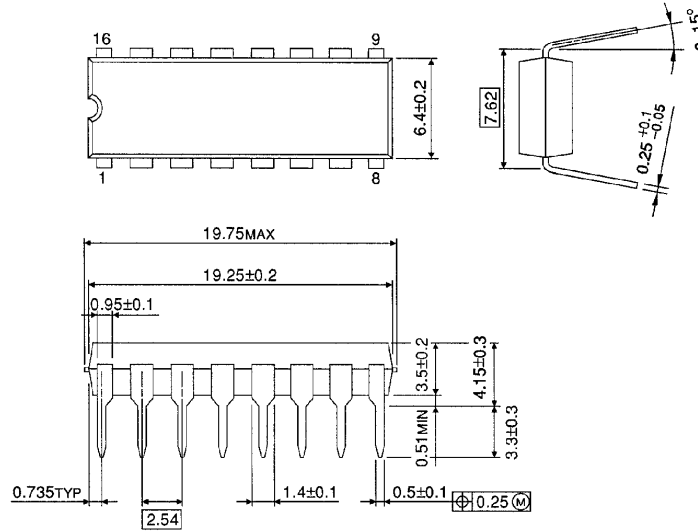
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

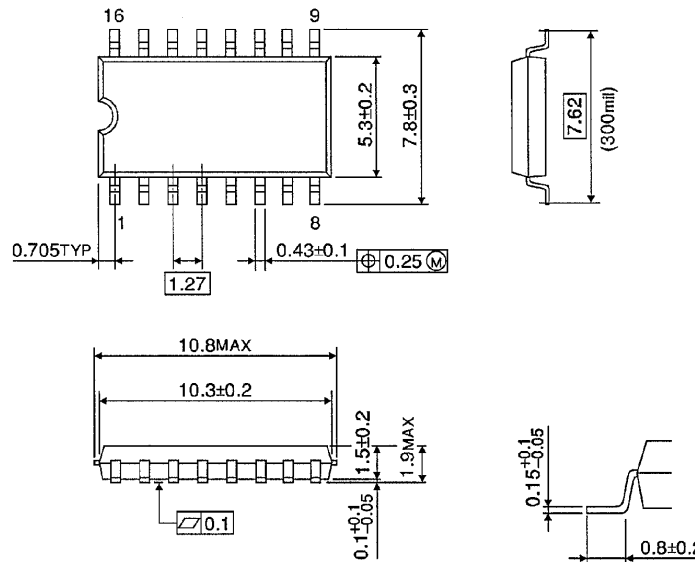
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

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000707EBA

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