TC1235 TC1236 TC1237

Inverting Dual ($-V_{IN}$, $-2V_{IN}$) Charge Pump Voltage Converters with Shutdown

FEATURES

- 10-Pin MSOP Package
- Operates from 1.8V to 5.5V
- Up to 5mA Output Current at $-V_{IN}$ Pin
- Up to 1mA Output Current at $-2V_{IN}$ Pin
- Power-Saving Shutdown Mode
- $-V_{IN}$ and $-2V_{IN}$ Outputs Available
- Low Active Supply Current
  - .... 120µA (MAX) for TC1235
  - .... 360µA (MAX) for TC1236
  - .... 1.5mA (MAX) for TC1237
- Fully Compatible with 1.8V Logic Systems

TYPICAL APPLICATIONS

- LCD Panel Bias
- Cellular Phones PA Bias
- Pagers
- PDAs, Portable Dataloggers
- Battery Powered Devices

GENERAL DESCRIPTION

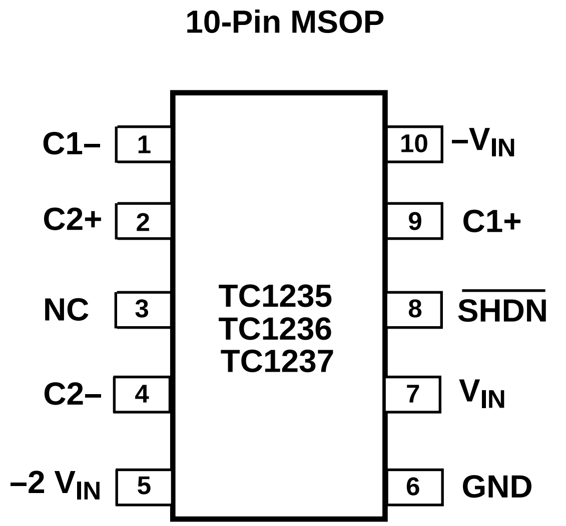
The TC1235/1236/1237 are CMOS dual inverting charge pump voltage converters with a low power shutdown mode in MSOP 10-Pin packages. Only four external capacitors are required for full circuit implementation. Switching frequencies are 12kHz for the TC1235, 35kHz for the TC1236 and 125kHz for the TC1237. When the shutdown pin is held at a logic low, the device goes into a very low power mode of operation, consuming less than 1µA of supply current.

These devices provide both a negative voltage inversion (available at the $-V_{IN}$ output), and a negative doubling voltage inversion (available at the $-2 V_{IN}$ output) with a low output impedance capable of providing output currents up to 5mA for the $-V_{IN}$ output and 1mA for the $-2V_{IN}$ output. The input voltage can range from +1.8V to +5.5V.

ORDERING INFORMATION

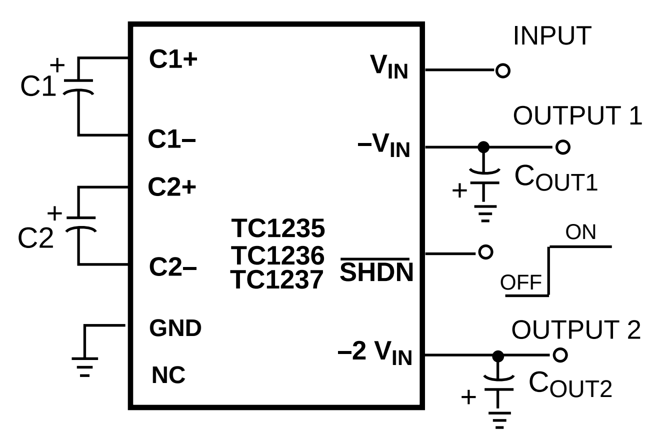
Part No.	Package	Osc Freq (KHz)	Temp Range
TC1235EUN	10-Pin MSOP	12	–40°C to +85°C
TC1236EUN	10-Pin MSOP	35	–40°C to +85°C
TC1237EUN	10-Pin MSOP	125	–40°C to +85°C

PIN CONFIGURATION



Notes: 1) C1 and C_{OUT1} must have a voltage rating greater than or equal to V_{IN}
2) C2 and C_{OUT2} must have a voltage rating greater than or equal to $2V_{IN}$

TYPICAL OPERATING CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Input Voltage (V_{IN} to GND) .... +6.0V, – 0.3V
Output Voltage ($-V_{IN}$, $-2V_{IN}$ to GND) .... –12.0V, + 0.3V
Current at $-V_{IN}$, $-2V_{IN}$ Pins 10mA
Short-Circuit Duration $-V_{IN}$, $-2V_{IN}$ to GND .... Indefinite
Operating Temperature Range .... – 40°C to +85°C
Power Dissipation ($T_A \leq 70$°C) MSOP-10 .... 320mW
Storage Temperature (Unbiased) .... – 65°C to +150°C
Lead Temperature (Soldering, 10sec) .... +260°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

T_A = –40°C to +85°C, V_{IN} = +5V, C1 = 3.3µF, C2 = 1µF (TC1235); C1 = 1µF, C2 = 0.33µF (TC1236); C1 = 0.33µF, C2 = 0.1µF (TC1237), $\overline{SHDN}$ = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C.

Symbol	Parameter	Device	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply Current	TC1235 TC1236 TC1237	$\overline{SHDN}$ = V_{IN} $\overline{SHDN}$ = V_{IN} $\overline{SHDN}$ = V_{IN}	— — —	75 200 625	120 360 1500	µA
I_{SHDN}	Shutdown Supply Current	All	$\overline{SHDN}$ = GND, V_{IN} = +5V	—	0.1	1	µA
V_{MIN}	Minimum Supply Voltage	All	R_{LOAD} = 1kΩ for $-V_{IN}$ output R_{LOAD} = 10kΩ for $-2V_{IN}$ output	1.8	—	—	V
V_{MAX}	Maximum Supply Voltage	All	R_{LOAD} = 1kΩ for $-V_{IN}$ output R_{LOAD} = 10kΩ for $-2V_{IN}$ output	—	—	5.5	V
F_{OSC}	Oscillator Frequency	TC1235 TC1236 TC1237		8.4 24.5 65	12 35 125	15.6 45.5 170	kHz
V_{IH}	Shutdown Input Logic High	All	V_{IN} = V_{MIN} to V_{MAX}	1.4	—	—	V
V_{IL}	Shutdown Input Logic low	All	V_{IN} = V_{MIN} to V_{MAX}	—	—	0.4	V
V_{EFF1}	Voltage Conversion Efficiency (Stage 1)	All	R_{LOAD} = ∞ for $-V_{IN}$ output R_{LOAD} = ∞ for $-2V_{IN}$ output	96	99.5	—	%
V_{EFF2}	Voltage Conversion Efficiency (Stage 2)	All	R_{LOAD} = ∞ for $-V_{IN}$ output R_{LOAD} = ∞ for $-2V_{IN}$ output	94	99	—	%
R_{OUT1}	Output Resistance for $-V_{IN}$ output (Note 1)	All	I_{LOAD} = 0.5mA to 5mA No Load at $-V_{IN}$ Output	—	45	80	Ω
R_{OUT2}	Output Resistance for $-2V_{IN}$ output (Note 1)	All	I_{LOAD} = 0.1mA to 1mA No Load at $-2V_{IN}$ Output	—	135	420	Ω
T_{WK1}	Wake-Up Time From Shutdown Mode Stage 1	TC1235 TC1236 TC1237	R_{LOAD} = 1kΩ for $-V_{IN}$ Output R_{LOAD} = 10kΩ for $-2V_{IN}$ Output	— — —	650 250 100	— — —	µsec
T_{WK2}	Wake-Up Time From Shutdown Mode Stage 2	TC1235 TC1236 TC1237	R_{LOAD} = 1kΩ for $-V_{IN}$ Output R_{LOAD} = 10kΩ for $-2V_{IN}$ Output	— — —	750 280 120	— —	µsec

NOTES: 1. Capacitor contribution is approximately 20% of the output impedance [ESR = 1 / pump frequency x capacitance)].

PIN DESCRIPTION

Pin Number	Name	Description
1	C1–	C1 Commutation Capacitor Negative Terminal.
2	C2+	C2 Commutation Capacitor Positive Terminal.
3	NC	No Connection.
4	C2–	C2 Commutation Capacitor Negative Terminal.
5	$-2V_{IN}$	Doubling Inverting Charge Pump Output (–2 x V_{IN}).
6	GND	Ground.
7	V_{IN}	Positive Power Supply Input.
8	$\overline{SHDN}$	Shutdown Input (Active Low).
9	C1+	C1 Commutation Capacitor Positive Terminal.
10	$-V_{IN}$	Inverting Charge Pump Output (–1 x V_{IN}).

DETAILED DESCRIPTION

The TC1235/1236/1237 dual charge pump converters perform both a –1x and –2x multiply of the voltage applied to the V_{IN} pin. Output '– V_{IN}' provides a negative voltage inversion of the V_{IN} supply, while output '-2 V_{IN}' provides a negative doubling inversion of V_{IN}. Conversion is performed using two **synchronous** switching matrices and four external capacitors. When the shutdown input is held at a logic low both stages go into a very low power mode of operation consuming less than 1uA of supply current.

Figure 1 (below) is a block diagram representation of the TC1235/1236/1237 architecture. The first switching stage inverts the voltage present at V_{IN} and the second stage uses the '–V_{IN}' output generated from the first stage to produce the '–2V_{IN}' output function from the second stage switching matrix.

Each device contains an on-board oscillator that synchronously controls the operation of the charge pump switching matrices. The TC1235 synchronously switches at 12KHz, the TC1236 synchronously switches at 35KHz, and the TC1237 synchronously switches at 125KHz. The different oscillator frequencies for this device family allow the user to trade-off capacitor size versus supply current. Faster oscillators can use smaller external capacitors but will consume more supply current (see Electrical Characteristics Table).

When the shutdown input is in a low state, the oscillator and both switch matrices are powered off placing the TC1235/1236/1237 in the shutdown mode. When the V_{IN} supply input is powered from an external battery, the shutdown mode minimizes power consumption, which in turn will extend the life of the battery.

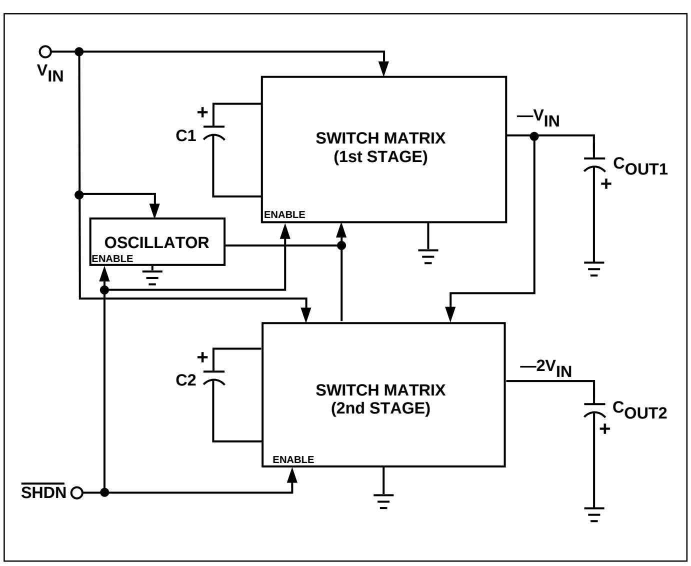


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

Output Voltage Considerations

The TC1235/1236/1237 performs voltage conversions but does not provide any type of regulation. The two output voltage stages will droop in a linear manner with respect to their respective load currents. The value of the equivalent output resistance of the '-V_{IN}' output is approximately 50Ω nominal at +25°C and V_{IN} = +5V. The value of the '-2V_{IN}' output and is approximately 140Ω nominal at +25°C and V_{IN} = +5V. In this particular case, '-V_{IN}' is approximately – 5V and '–2V_{IN}' is approximately –10V at very light loads, and each stage will droop according to the equation below:

$$V_{DROOP} = I_{OUT} \times R_{OUT}$$
$$[-V_{IN}\ \text{OUTPUT}] = V_{OUT1} = -(V_{IN} - V_{DROOP1})$$
$$[-2V_{IN}\ \text{OUTPUT}] = V_{OUT2} = V_{OUT1} - (V_{IN} - V_{DROOP2})$$

where V_{DROOP1} is the output voltage droop contributed from stage 1 loading , and V_{DROOP2} is the output voltage droop from stage 2 loading.

Charge Pump Efficiency

The overall power efficiency of the two charge pump stages is affected by four factors:

(1) Losses from power consumed by the internal oscillator, switch drive, etc. (which vary with input voltage, temperature and oscillator frequency).

(2) I^2R losses due to the on-resistance of the MOSFET switches on-board each charge pump.

(3) Charge pump capacitor losses due to effective series resistance (ESR).

(4) Losses that occur during charge transfer (from the commutation capacitor to the output capacitor) when a voltage difference between the two capacitors exists.

Most of the conversion losses are due to factor (2), (3) and (4) above. The losses for the first stage are given by Equation 1a and the losses for the second stage are given by Equation 1b.

$$P1_{LOSS\,(2,3,4)} = I_{OUT1}{}^{2} \times R_{OUT1}$$
$$\text{where } R_{OUT1} = \left[\, 1 / [\, f_{OSC}(C1)\,] + 8R_{SWITCH1} + 4ESR_{C1} + ESR_{COUT1} \,\right]$$

$$P2_{LOSS\ (2,3,4)} = I_{OUT2}{}^{2} \times R_{OUT2}$$
$$\text{where } R_{OUT2} = \left[1 / [f_{OSC}(C2)] + 8R_{SWITCH2} + 4ESR_{C2} + ESR_{COUT2} \right]$$

Equation 1b.

The internal switch resistance for the first stage (i.e. $R_{SWITCH1}$) is approximately 3Ω and the switch resistance for the second stage (i.e. $R_{SWITCH2}$) is approximately 7Ω.

The losses in the circuit due to factor (4) above are also shown in Equation 2a for stage 1 and Equation 2b for stage 2. The output voltage ripple for stage 1 is given by Equation 3a and the output voltage ripple for stage 2 is given by Equation 3b.

$$P_{LOSS1\ (4)} = \left[(0.5)(C1)(V_{IN}{}^{2} - V_{OUT1}{}^{2}) + (0.5)(C_{OUT1})(V_{RIPPLE1}{}^{2} - 2V_{OUT1}V_{RIPPLE1}) \right] \times f_{OSC}$$

Equation 2a.

$$P_{LOSS2\ (4)} = \left[(0.5)(C2)(V_{IN}{}^{2} - V_{OUT2}{}^{2}) + (0.5)(C_{OUT2})(V_{RIPPLE2}{}^{2} - 2V_{OUT2}V_{RIPPLE2}) \right] \times f_{OSC}$$

Equation 2b.

$$V_{RIPPLE1} = [I_{OUT1} / (f_{OSC})(C_{OUT1})] + 2(I_{OUT1})(ESR_{COUT1})$$

Equation 3a.

$$V_{RIPPLE2} = [I_{OUT2} / (f_{OSC})(C_{OUT2})] + 2(I_{OUT2})(ESR_{COUT2})$$

Equation 3b.

Capacitor Selection

In order to maintain the lowest output resistance and output ripple voltage, it is recommended that low ESR capacitors be used. Additionally, larger values of C1 and C2 will lower the output resistance and larger values of C_{OUT1} and C_{OUT2} will reduce output ripple. (See Equations 1a, 1b, 3a, and 3b). **NOTE: For proper charge pump operation, C1 and C_{OUT1} must have a voltage rating greater than or equal to V_{IN}, while C2 and C_{OUT2} must have a voltage rating greater than or equal to $2V_{IN}$.**

Table 1a shows various values of C1 and the corresponding output resistance values for V_{IN}=5V @ +25°C for stage 1 and Table 1b shows various values of C2 and the corresponding output resistance values for V_{IN}=5V @ +25°C for stage 2. It assumes a 0.1Ω ESR_{C1}, a 0.1Ω ESR_{C2}, a 3Ω $R_{SWITCH1}$, and a 7Ω $R_{SWITCH2}$.

Table 2a shows the output voltage ripple for various values of C_{OUT1} and Table 2b shows the output voltage ripple for various values of C_{OUT2} (again assuming V_{IN} = 5V @ +25°C). The $V_{RIPPLE1}$ values assume a 3mA output load current for stage 1 and a 0.1Ω ESR_{COUT1}. The $V_{RIPPLE2}$ values assume a 200µA output load current for stage 2 and a 0.1Ω ESR_{COUT1}.

Table 1a. Output Resistance vs. C1 (ESR = 0.1Ω). For Stage 1

C1 (µF)	TC1235 R_{OUT} (Ω)	TC1236 R_{OUT} (Ω)	TC1237 R_{OUT} (Ω)
0.47	202	85	42
1	108	53	33
3.3	50	33	27

Table 1b. Output Resistance vs. C2 (ESR = 0.1Ω). For Stage 2

C2 (µF)	TC1235 R_{OUT} (Ω)	TC1236 R_{OUT} (Ω)	TC1237 R_{OUT} (Ω)
0.1	890	342	137
0.47	239	117	74
1	140	85	65

Table 2a. Output Voltage Ripple vs. C_{OUT1} (ESR = 0.1Ω) For Stage 1 (I_{OUT1} = 3mA)

C_{OUT1} (µF)	TC1235 $V_{RIPPLE1}$ (mV)	TC1236 $V_{RIPPLE1}$ (mV)	TC1237 $V_{RIPPLE1}$ (mV)
0.47	533	183	52
1	251	86	25
3.3	76	27	8

Table 2b. Output Voltage Ripple vs. C_{OUT2} (ESR = 0.1Ω) For Stage 2 (I_{OUT2} = 200µA)

C_{OUT2} (µF)	TC1235 $V_{RIPPLE2}$ (mV)	TC1236 $V_{RIPPLE2}$ (mV)	TC1237 $V_{RIPPLE2}$ (mV)
0.1	167	57	16
0.47	36	12	3.4
1	17	5.8	1.6

Input Supply Bypassing

The V_{IN} input should be capacitively bypassed to reduce AC impedance and minimize noise effects due to the switching internal to the device. It is recommended that a large value capacitor (at least equal to C1) be connected from V_{IN} to GND for optimal circuit performance.

Shutdown Input

The TC12351/1236/1237 is enabled when /SHDN is high, and disabled when /SHDN is low. This input cannot be allowed to float. (If /SHDN is not required, see the TC1225/1226/1227 data sheet.) The /SHDN input should be limited to 0.3V above V_{IN} to avoid significant current flows.

Dual Voltage Inverter

The most common application for the TC1235/1236/1237 devices is the dual voltage inverter (Figure 2). This application uses four external capacitors: C1, C2, C_{OUT1}, and C_{OUT2} (NOTE: a power supply bypass capacitor is recommended). The outputs are equal to – V_{IN} and –2VIN plus any voltage drops due to loading. Refer to Tables 1a, 1b, 2a, and 2b for capacitor selection guidelines.

Device	C_{IN}	C1	C2	C_{OUT1}	C_{OUT2}
TC1235	3.3µF	3.3µF	1µF	3.3µF	1µF
TC1236	1µF	1µF	0.33µF	1µF	0.33µF
TC1237	0.33µF	0.33µF	0.1µF	0.33µF	0.1µF

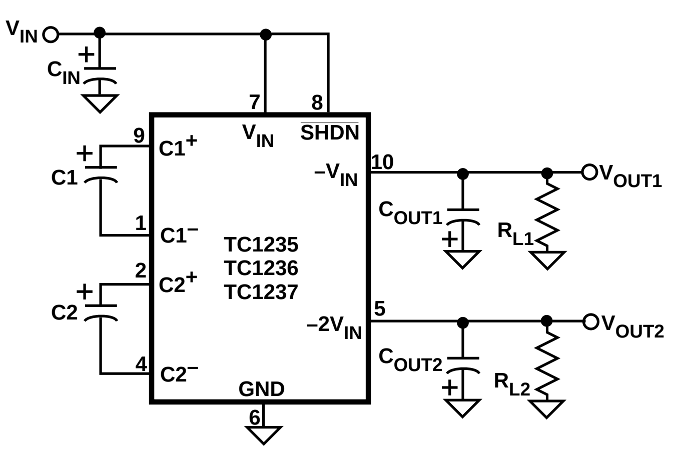


Figure 2. Dual Voltage Inverter Test Circuit

Layout Considerations

As with any switching power supply circuit good layout practice is recommended. Mount components as close together as possible to minimize stray inductance and capacitance. Also use a large ground plane to minimize noise leakage into other circuitry.

TC1235 DEMO Card

The TC1235 DEMO Card is a 2.0" x 2.0" card containing both a TC1235 and two cascaded TC1219s that allow the user to compare the operation of each approach for generating a –1X and –2X function. Each circuit is fully assembled with the required external capacitors along with variable load resistors that allow the user to vary the output load current of each stage. For convenience, several test points and jumpers are available for measuring various voltages and currents on the demo board.

Figure 3 is a schematic of the TC1235 DEMO Card, and Figure 4 shows the assembly drawing and artwork for the board. Table 3 lists the voltages that are monitored by the test points and Table 4 lists the currents that can be measured using the jumpers.

Table 3. TC1235 DEMO Card Test Points

TEST POINT	VOLTAGE MEASUREMENT
TP1	VIN [+5V]
TP2	GROUND
TP3	GROUND
TP4	TC1219 U1 OUTPUT [-5V(1)]
TP5	TC1219 U2 OUTPUT [-10V(1)]
TP6	TC1235 STAGE 1 OUTPUT [-5V(2)]
TP7	TC1235 STAGE 2 OUTPUT [-10V(2)]
TP8	EXTERNAL /SHDN INPUT
TP9	TC1219 U1 /SHDN INPUT
TP10	TC1235 U3 /SHDN INPUT

Table 4. TC1235 DEMO Card Jumpers

JUMPER	CURRENT MEASUREMNT
J1	DUAL TC1219 QUIESCENT CURRENT
J2	TC1235 QUIESCENT CURRENT
J3	TC1219 U1 [-5V(1)] LOAD CURRENT
J4	TC1219 U2 [-10V(1)] LOAD CURRENT
J5	TC1235 STAGE 1 [-5V(2)] LOAD CURRENT
J6	TC1235 STAGE 2 [-10V(2)] LOAD CURRENT
J7	TC1219 U1 /SHDN INPUT CURRENT
J8	TC1235 U3 /SHDN INPUT CURRENT
J9	GROUND EXTERNAL /SHDN INPUT

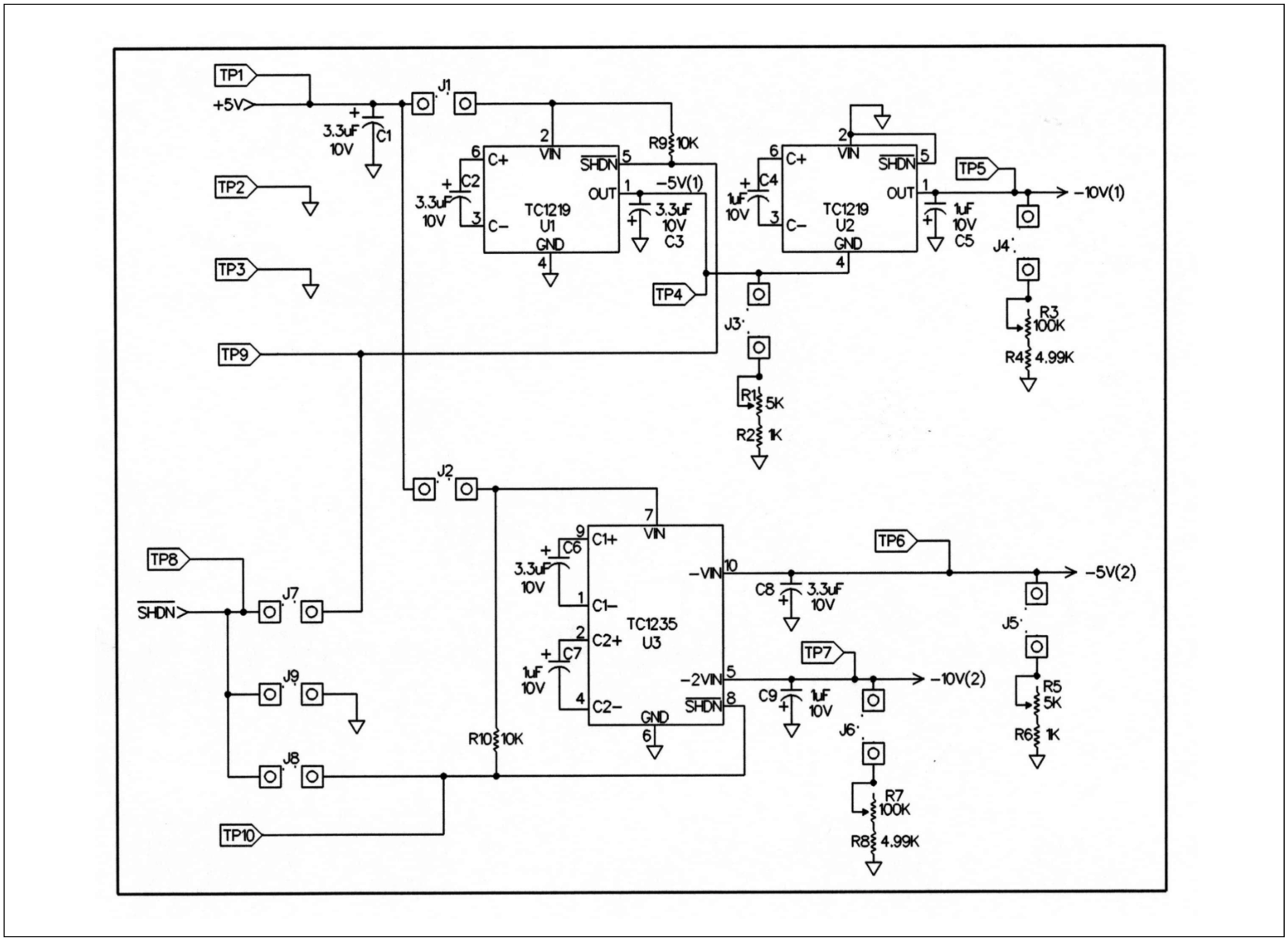


Figure 3. TC1235 DEMO Card Schematic

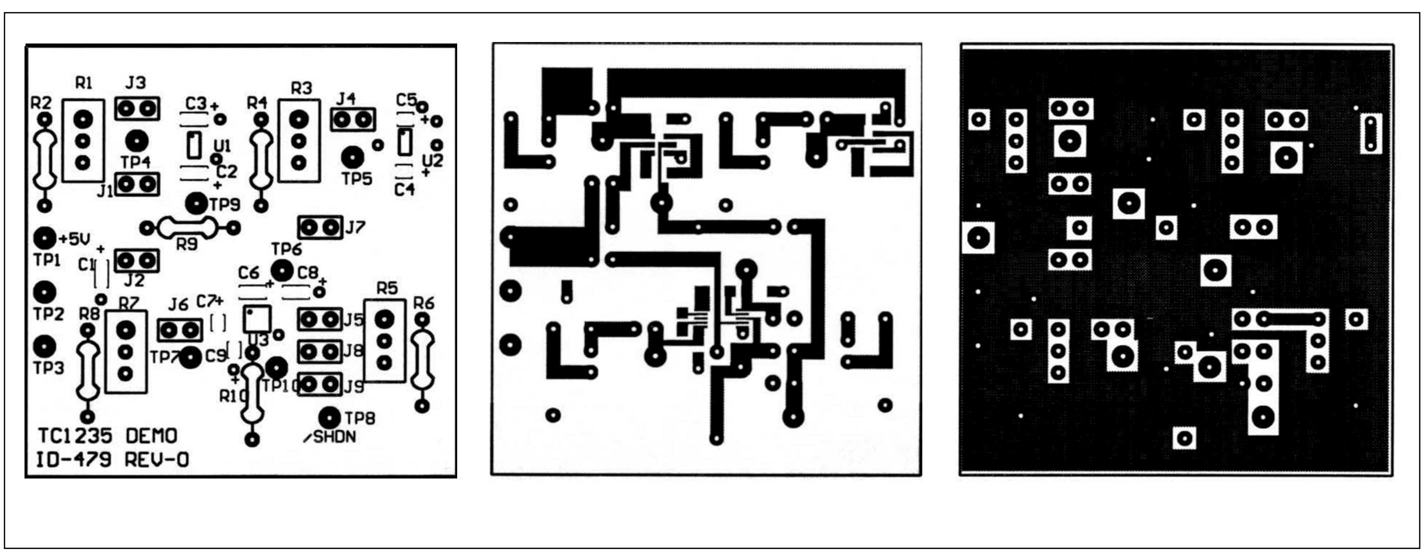
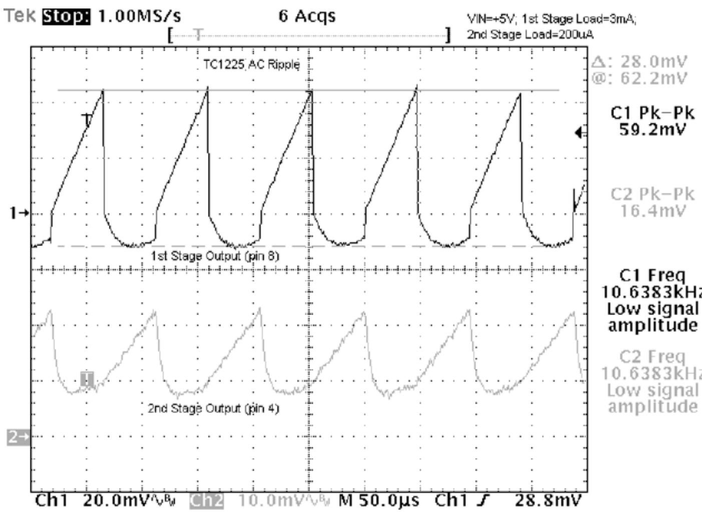
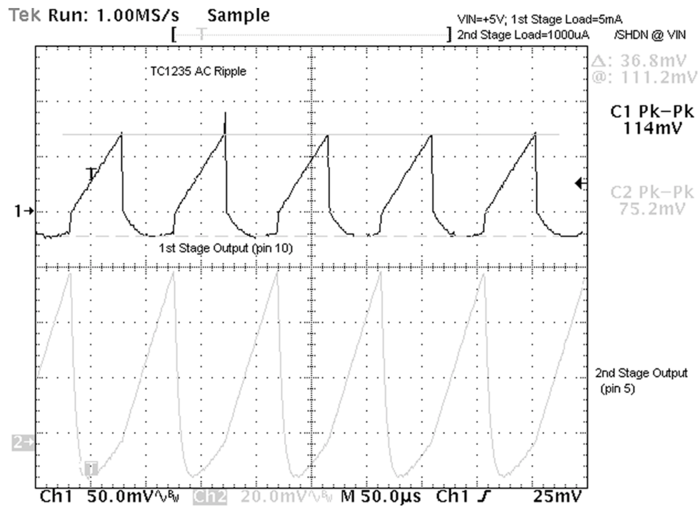
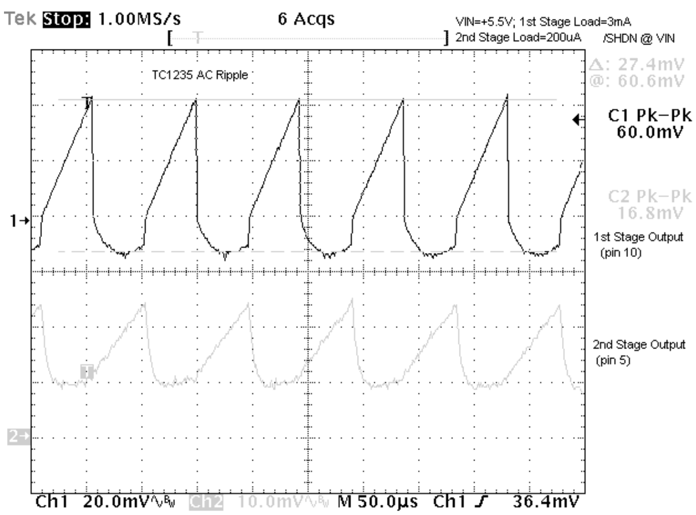


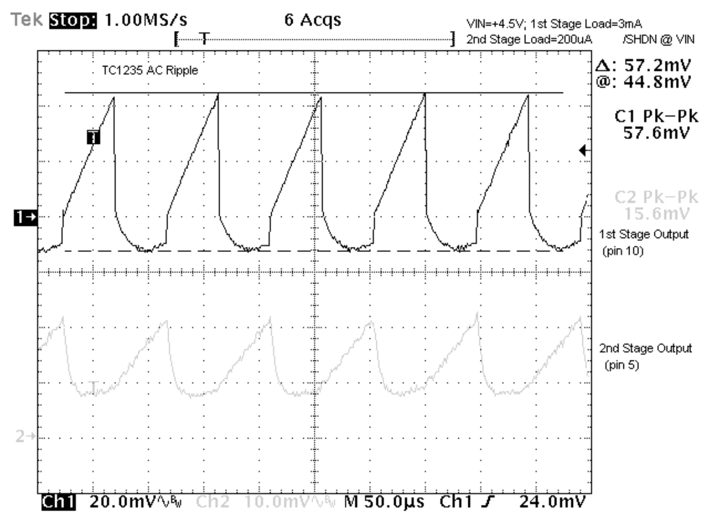
Figure 4. TC1235 DEMO Card Assembly Drawing and Artwork

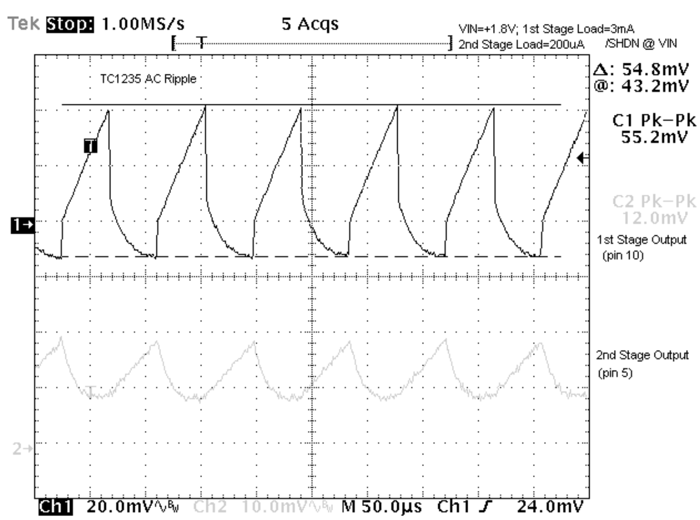
TYPICAL RIPPLE WAVEFORMS





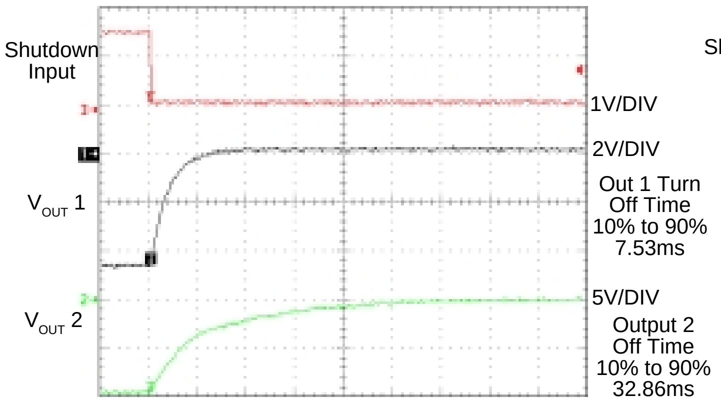






TYPICAL RIPPLE WAVEFORMS

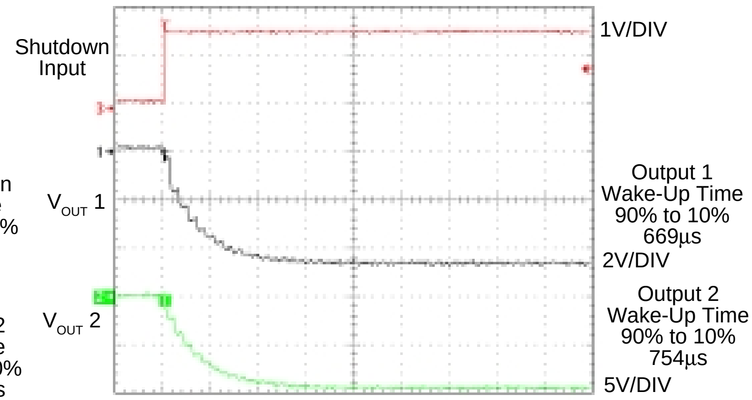
TC1235 TURN OFF TIME



HORIZ = 10ms/DIV

Conditions:
C1, $C_{OUT}1 = 3.3\mu f$, C2, $C_{OUT}2 = 1\mu f$, $V_{IN} = 5V$

TC1235 WAKE-UP TIME FROM SHUTDOWN

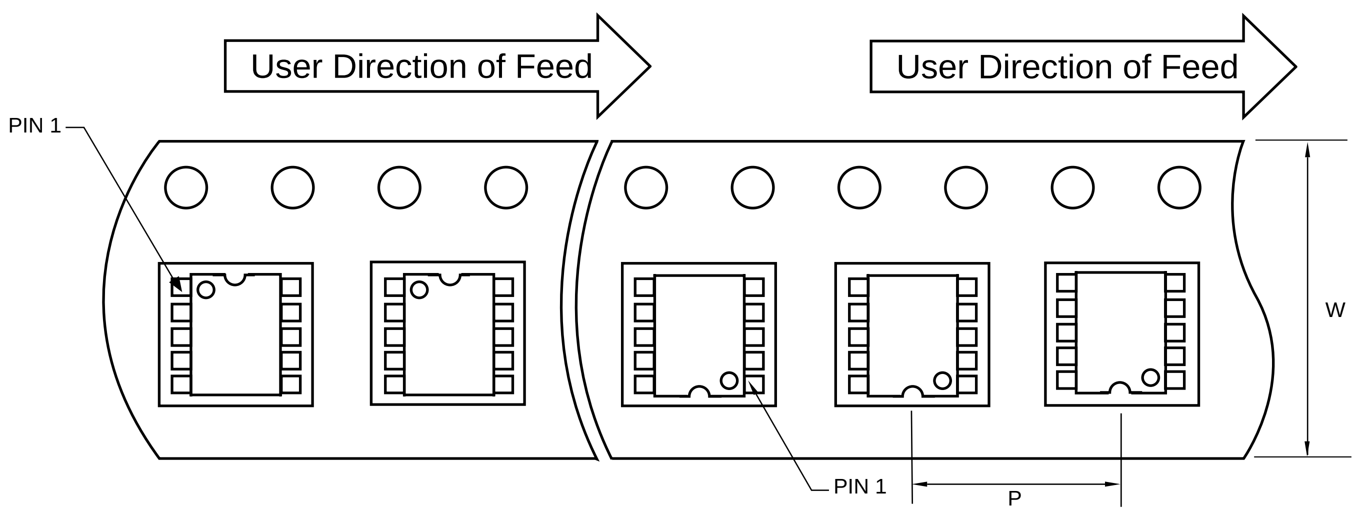


HORIZ = 500µs/DIV

Conditions:
C1, $C_{OUT}1 = 3.3\mu f$, C2, $C_{OUT}2 = 1\mu f$, $V_{IN} = 5V$

TAPING FORM

Component Taping Orientation for 10-Pin MSOP Devices



Standard Reel Component Orientation for TR Suffix Device

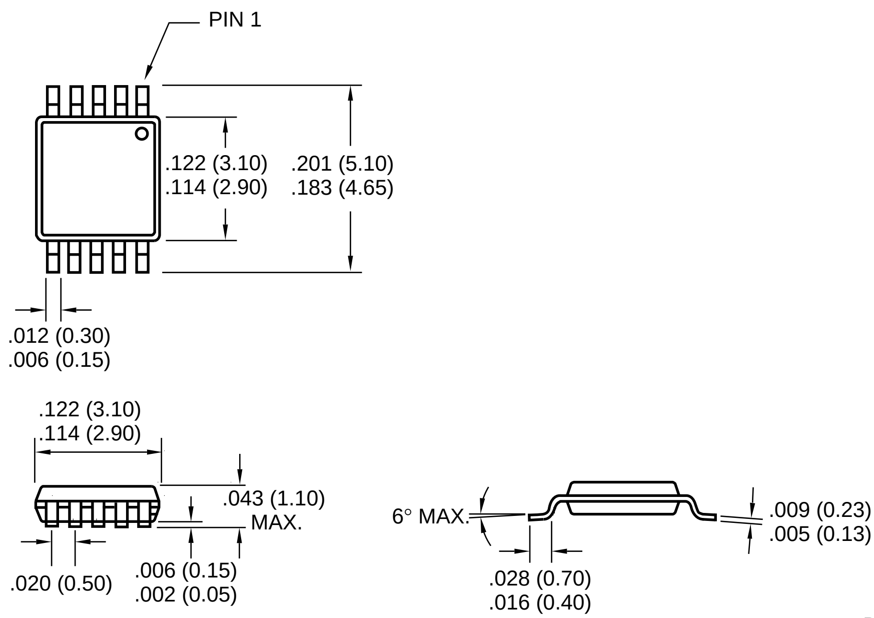
Reverse Reel Component Orientation for RT Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
10-Pin MSOP	12 mm	8 mm	2500	13 in

PACKAGE DIMENSIONS

10-Pin MSOP



Dimensions: inches (mm)

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