

SN74S1051

12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

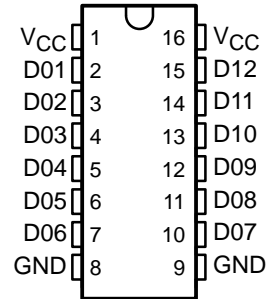
SDLS018B – SEPTEMBER 1990 – REVISED MARCH 2003

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current to 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems

description/ordering information

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

D, N, NS, OR PW PACKAGE
(TOP VIEW)

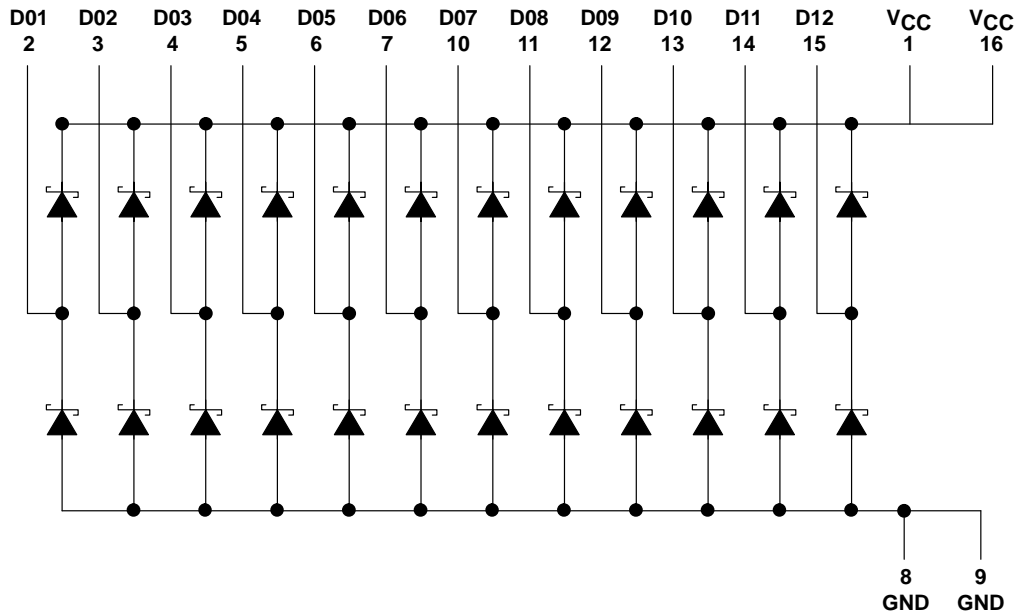


ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------------|---------------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74S1051N | SN74S1051N |
| | SOIC – D | Tube | SN74S1051D | S1051 |
| | | Tape and reel | SN74S1051DR | |
| | SOP – NS | Tape and reel | SN74S1051NSR | 74S1051 |
| TSSOP – PW | Tape and reel | SN74S1051PWR | S1051 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic diagrams



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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12-BIT SCHOTTKY BARRIER DIODE

BUS-TERMINATION ARRAY

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Steady-state reverse voltage, V_R | 7 V |
| Continuous forward current, I_F : Any D terminal from GND or to V_{CC} | 50 mA |
| Total through all GND or V_{CC} terminals | 170 mA |
| Repetitive peak forward current‡, I_{FRM} : Any D terminal from GND or V_{CC} | 200 mA |
| Total through all GND or V_{CC} terminals | 1 A |
| Package thermal impedance, θ_{JA} (see Note 1): D package | 73°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_w \leq 100 \mu s$, duty cycle $\leq 20\%$.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP§ | MAX | UNIT |
|-----------|------------------------|--|------------------------|------|------|-----|---------|
| V_F | Static forward voltage | To V_{CC} | $I_F = 18 \text{ mA}$ | 0.85 | 1.05 | V | |
| | | | $I_F = 50 \text{ mA}$ | 1.05 | 1.3 | | |
| | | From GND | $I_F = 18 \text{ mA}$ | 0.75 | 0.95 | | |
| | | | $I_F = 50 \text{ mA}$ | 0.95 | 1.2 | | |
| V_{FM} | Peak forward voltage | | $I_F = 200 \text{ mA}$ | 1.45 | | V | |
| I_R | Static reverse current | To V_{CC} | $V_R = 7 \text{ V}$ | | | 5 | μA |
| | | From GND | | | 5 | | |
| C_t | Total capacitance | $V_R = 0 \text{ V}, f = 1 \text{ MHz}$ | | 8 | 16 | pF | |
| | | $V_R = 2 \text{ V}, f = 1 \text{ MHz}$ | | 4 | 8 | | |

§ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ C$.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

| PARAMETER | | TEST CONDITIONS | | MIN | TYP§ | MAX | UNIT |
|-----------|----------------------------|-------------------------------|------------|------|------|-----|------|
| I_x | Internal crosstalk current | Total I_F current = 1 A, | See Note 3 | 0.8 | 2 | mA | |
| | | Total I_F current = 198 mA, | See Note 3 | 0.02 | 0.2 | | |

§ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ C$.

NOTE 3: I_x is measured under the following conditions with one diode static, all others switching:

Switching diodes: $t_w = 100 \mu s$, duty cycle = 20%

Static diode: $V_R = 5 \text{ V}$

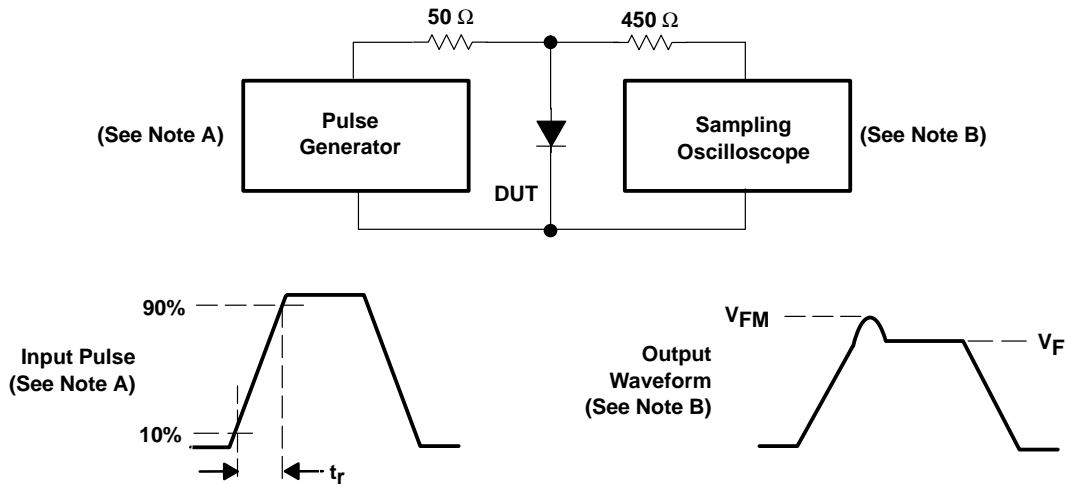
The static diode input current is the internal crosstalk current, I_x .

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

| PARAMETER | | TEST CONDITIONS | | | | MIN | TYP | MAX | UNIT |
|-----------|-----------------------|---|--|--|--|-----|-----|-----|------|
| t_{rr} | Reverse recovery time | $I_F = 10 \text{ mA}, I_{RM(REC)} = 10 \text{ mA}, I_{R(REC)} = 1 \text{ mA}, R_L = 100 \Omega$ | | | | 8 | 16 | ns | |

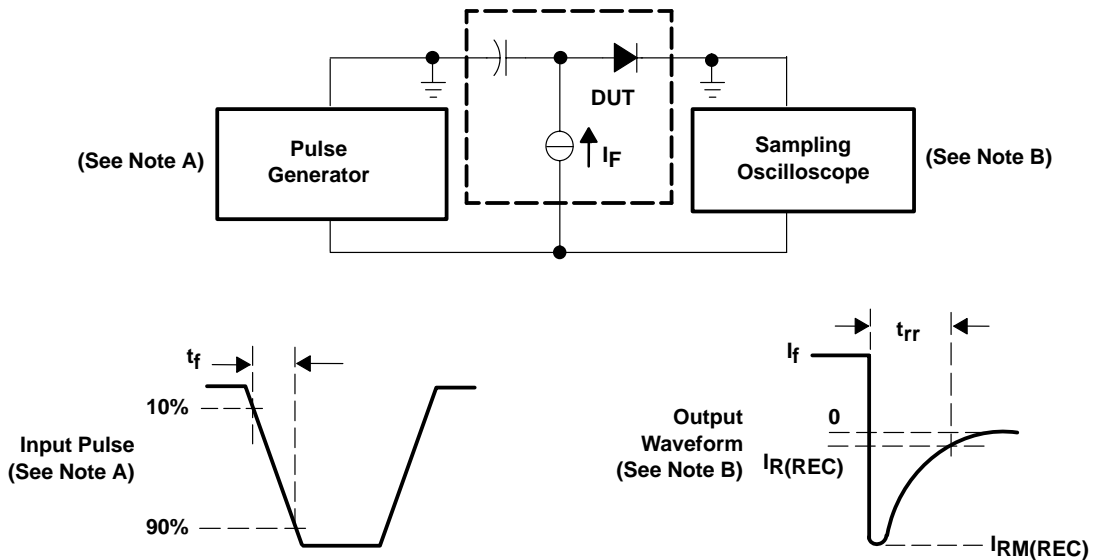


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_r = 20$ ns, $Z_O = 50$ Ω , freq = 500 Hz, duty cycle = 1%.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω , $C_i \leq 5$ pF.

Figure 1. Forward Recovery Voltage



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 0.5$ ns, $Z_O = 50$ Ω , $t_w \geq 50$ ns, duty cycle = 1%.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω , $C_i \leq 5$ pF.

Figure 2. Reverse Recovery Time

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APPLICATION INFORMATION

Large negative transients at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split-resistor or Thevenin-equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line because a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. Typical current-versus-voltage curves for the SN74S1051 are shown in Figures 3 and 4.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 5 was evaluated. The resulting waveforms with and without the diode are shown in Figure 6.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

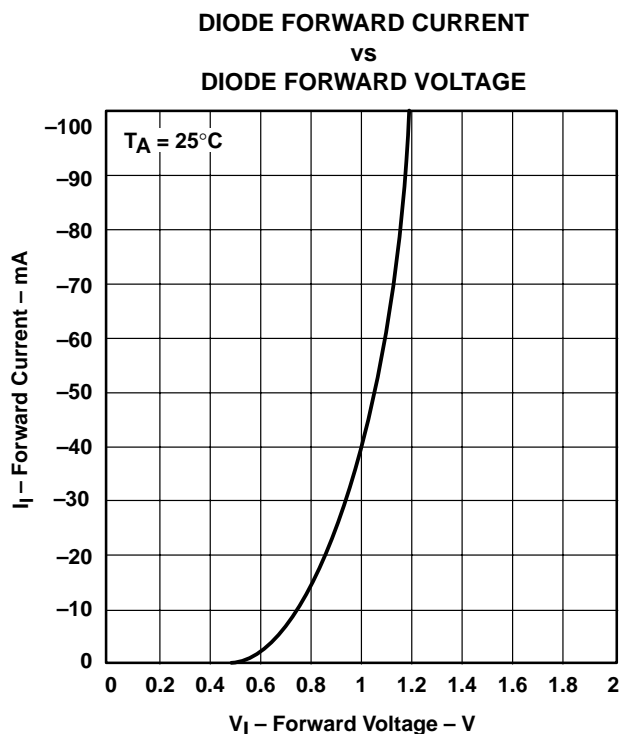
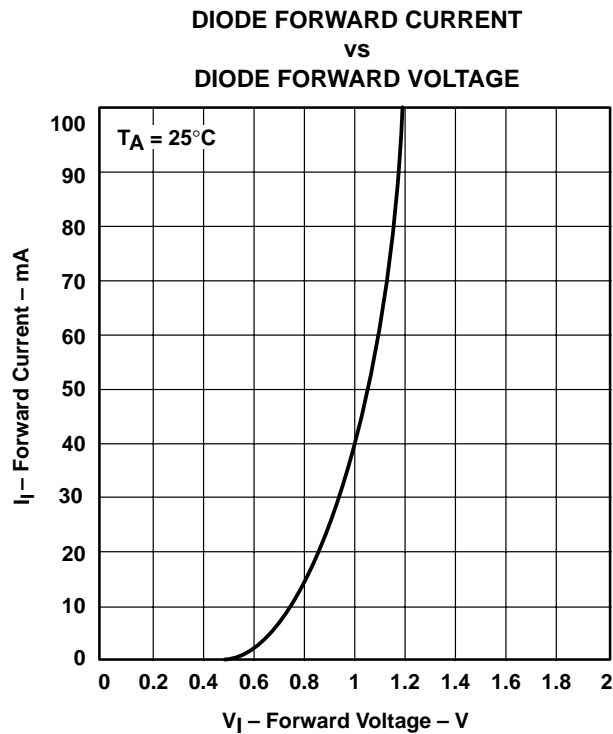


Figure 3. Typical Input Current vs Input Voltage
(Lower Diode)



**Figure 4. Typical Input Current vs Input Voltage
(Upper Diode)**

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APPLICATION INFORMATION

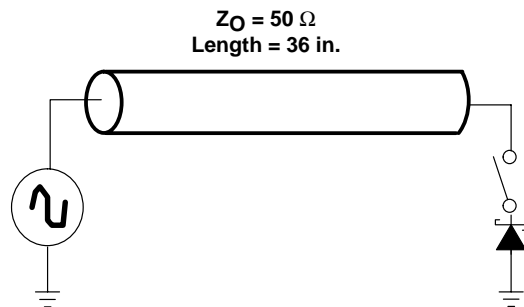


Figure 5. Diode Test Setup

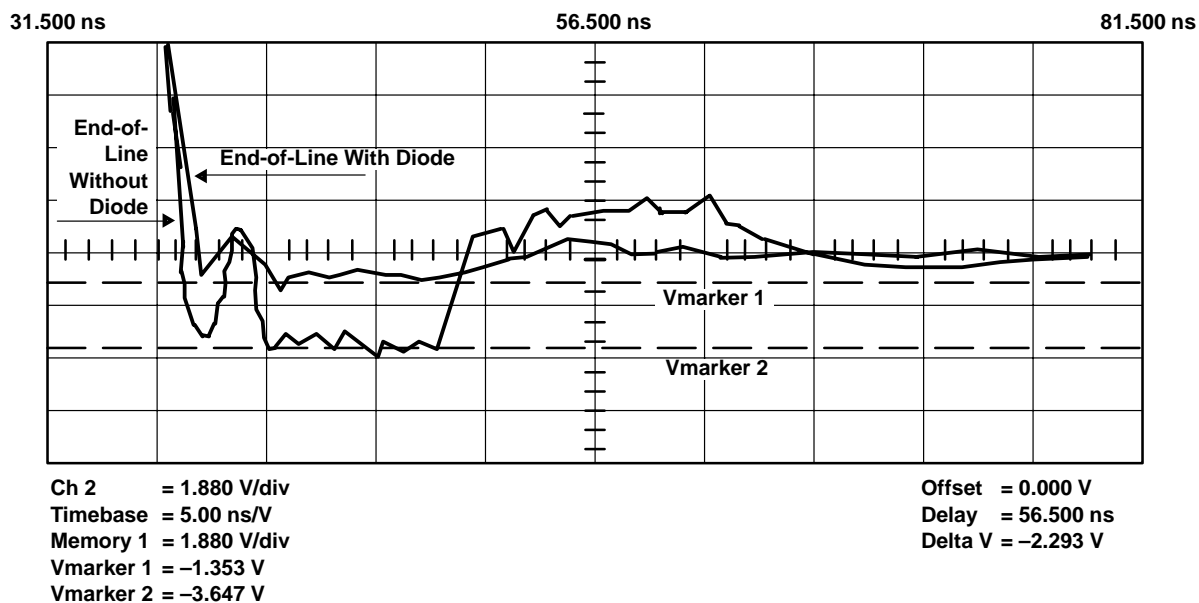


Figure 6. Reduction of Negative Transients at the End of a Transmission Line

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| SN74S1051D | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74S1051DR | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74S1051N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74S1051NSR | ACTIVE | SO | NS | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74S1051PW | ACTIVE | TSSOP | PW | 16 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74S1051PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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