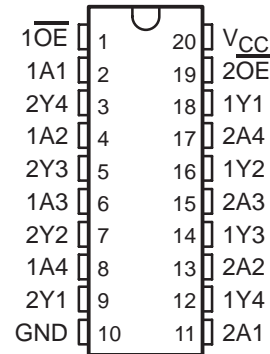


SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

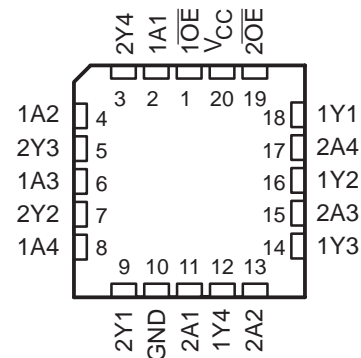
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
<0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
>2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LV240A . . . J OR W PACKAGE
SN74LV240A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV240A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------|----------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube of 25 | SN74LV240ADW | LV240A |
| | | Reel of 2000 | SN74LV240ADWR | |
| | SOP – NS | Reel of 2000 | SN74LV240ANSR | 74LV240A |
| | SSOP – DB | Reel of 2000 | SN74LV240ADBR | LV240A |
| | TSSOP – PW | Tube of 70 | SN74LV240APW | LV240A |
| | | Reel of 2000 | SN74LV240APWR | |
| Reel of 250 | | SN74LV240APWT | | |
| TVSOP – DGV | Reel of 2000 | SN74LV240ADGVR | LV240A | |
| -55°C to 125°C | CDIP – J | Tube of 20 | SNJ54LV240AJ | SNJ54LV240AJ |
| | CFP – W | Tube of 85 | SNJ54LV240AW | SNJ54LV240AW |
| | LCCC – FK | Tube of 55 | SNJ54LV240AFK | SNJ54LV240AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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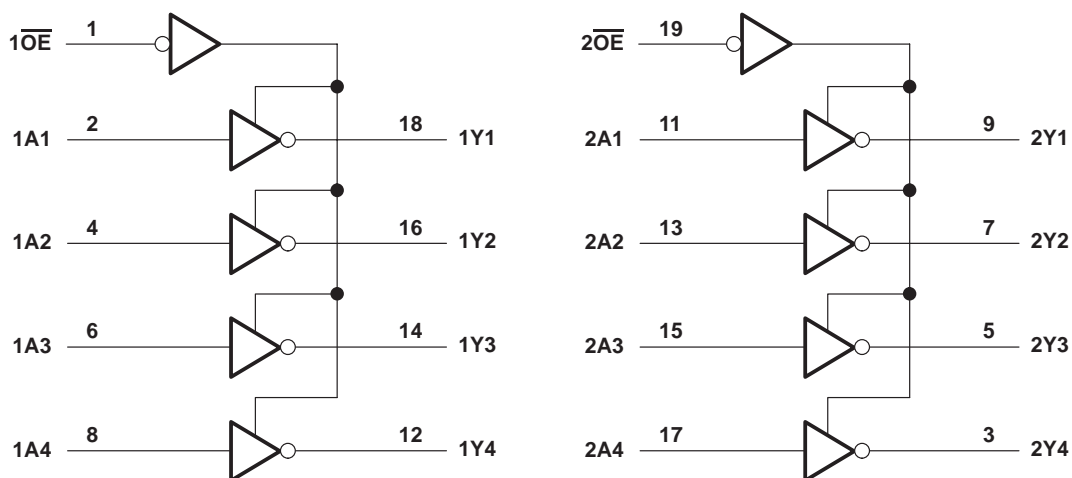
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

logic diagram (positive logic)



SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

| | | SN54LV240A | | SN74LV240A | | UNIT | |
|---------------------|------------------------------------|---|---------------------|---------------------|-----|--------------------|---------------|
| | | MIN | MAX | MIN | MAX | | |
| V_{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V | |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | 1.5 | | V | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | 0.5 | 0.5 | | V | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | | | |
| V_I | Input voltage | 0 | 5.5 | 0 | 5.5 | V | |
| V_O | Output voltage | High or low state | 0 | V_{CC} | 0 | V_{CC} | V |
| | | 3-state | 0 | 5.5 | 0 | 5.5 | |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | | -50 | | -50 | μA |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | -2 | | -2 | mA |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | -8 | | -8 | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | -16 | | -16 | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | | 50 | | 50 | μA |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | 2 | | 2 | mA |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | 8 | | 8 | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | 16 | | 16 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | 200 | | 200 | ns/V |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | 100 | | 100 | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | 20 | | 20 | |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | $^{\circ}\text{C}$ | |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | SN54LV240A | | | SN74LV240A | | | UNIT |
|-----------|----------------------------------|--------------|--------------|-----|-----|--------------|-----|-----|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{OH} | $I_{OH} = -50\ \mu\text{A}$ | 2 V to 5.5 V | $V_{CC}-0.1$ | | | $V_{CC}-0.1$ | | | V |
| | $I_{OH} = -2\ \text{mA}$ | 2.3 V | 2 | | | 2 | | | |
| | $I_{OH} = -8\ \text{mA}$ | 3 V | 2.48 | | | 2.48 | | | |
| | $I_{OH} = -16\ \text{mA}$ | 4.5 V | 3.8 | | | 3.8 | | | |
| V_{OL} | $I_{OL} = 50\ \mu\text{A}$ | 2 V to 5.5 V | | | | 0.1 | | | V |
| | $I_{OL} = 2\ \text{mA}$ | 2.3 V | | | | 0.4 | | | |
| | $I_{OL} = 8\ \text{mA}$ | 3 V | | | | 0.44 | | | |
| | $I_{OL} = 16\ \text{mA}$ | 4.5 V | | | | 0.55 | | | |
| I_I | $V_I = 5.5\ \text{V}$ or GND | 0 to 5.5 V | | | | ± 1 | | | μA |
| I_{OZ} | $V_O = V_{CC}$ or GND | 5.5 V | | | | ± 5 | | | μA |
| I_{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V | | | | 20 | | | μA |
| I_{off} | V_I or $V_O = 0$ to 5.5 V | 0 | | | | 5 | | | μA |
| C_i | $V_I = V_{CC}$ or GND | 3.3 V | 2.3 | | | 2.3 | | | pF |

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SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV240A | | SN74LV240A | | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|-------|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | $C_L = 15\text{ pF}$ | 6.3* | 11.6* | | 1* | 14* | 1 | 14 | ns |
| t_{en} | \overline{OE} | Y | | 8.5* | 14.6* | | 1* | 17* | 1 | 17 | |
| t_{dis} | \overline{OE} | Y | | 9.7* | 14.1* | | 1* | 16* | 1 | 16 | |
| t_{pd} | A | Y | $C_L = 50\text{ pF}$ | 8.2 | 14.4 | | 1 | 17 | 1 | 17 | ns |
| t_{en} | \overline{OE} | Y | | 10.3 | 17.8 | | 1 | 21 | 1 | 21 | |
| t_{dis} | \overline{OE} | Y | | 14.2 | 19.2 | | 1 | 21 | 1 | 21 | |
| $t_{sk(o)}$ | | | | | | 2 | | | | 2 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV240A | | SN74LV240A | | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|-------|-----|------------|-------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | $C_L = 15\text{ pF}$ | 4.6* | 7.5* | | 1* | 9* | 1 | 9 | ns |
| t_{en} | \overline{OE} | Y | | 6.2* | 10.6* | | 1* | 12.5* | 1 | 12.5 | |
| t_{dis} | \overline{OE} | Y | | 8.3* | 12.5* | | 1* | 13.5* | 1 | 13.5 | |
| t_{pd} | A | Y | $C_L = 50\text{ pF}$ | 5.9 | 11 | | 1 | 12.5 | 1 | 12.5 | ns |
| t_{en} | \overline{OE} | Y | | 7.5 | 14.1 | | 1 | 16 | 1 | 16 | |
| t_{dis} | \overline{OE} | Y | | 11.8 | 15 | | 1 | 17 | 1 | 17 | |
| $t_{sk(o)}$ | | | | | | 1.5 | | | | 1.5 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV240A | | SN74LV240A | | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|-------|-----|------------|-------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | $C_L = 15\text{ pF}$ | 3.4* | 5.5* | | 1* | 6.5* | 1 | 6.5 | ns |
| t_{en} | \overline{OE} | Y | | 4.6* | 7.3* | | 1* | 8.5* | 1 | 8.5 | |
| t_{dis} | \overline{OE} | Y | | 7.4* | 12.2* | | 1* | 13.5* | 1 | 13.5 | |
| t_{pd} | A | Y | $C_L = 50\text{ pF}$ | 4.4 | 7.5 | | 1 | 8.5 | 1 | 8.5 | ns |
| t_{en} | \overline{OE} | Y | | 5.6 | 9.3 | | 1 | 10.5 | 1 | 10.5 | |
| t_{dis} | \overline{OE} | Y | | 9.7 | 14.2 | | 1 | 15.5 | 1 | 15.5 | |
| $t_{sk(o)}$ | | | | | | 1 | | | | 1 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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SN54LV240A, SN74LV240A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

| PARAMETER | SN74LV240A | | | UNIT |
|--|------------|-------|------|------|
| | MIN | TYP | MAX | |
| $V_{OL(P)}$ Quiet output, maximum dynamic V_{OL} | | 0.56 | | V |
| $V_{OL(V)}$ Quiet output, minimum dynamic V_{OL} | | -0.49 | | V |
| $V_{OH(V)}$ Quiet output, minimum dynamic V_{OH} | | 2.82 | | V |
| $V_{IH(D)}$ High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ Low-level dynamic input voltage | | | 0.99 | V |

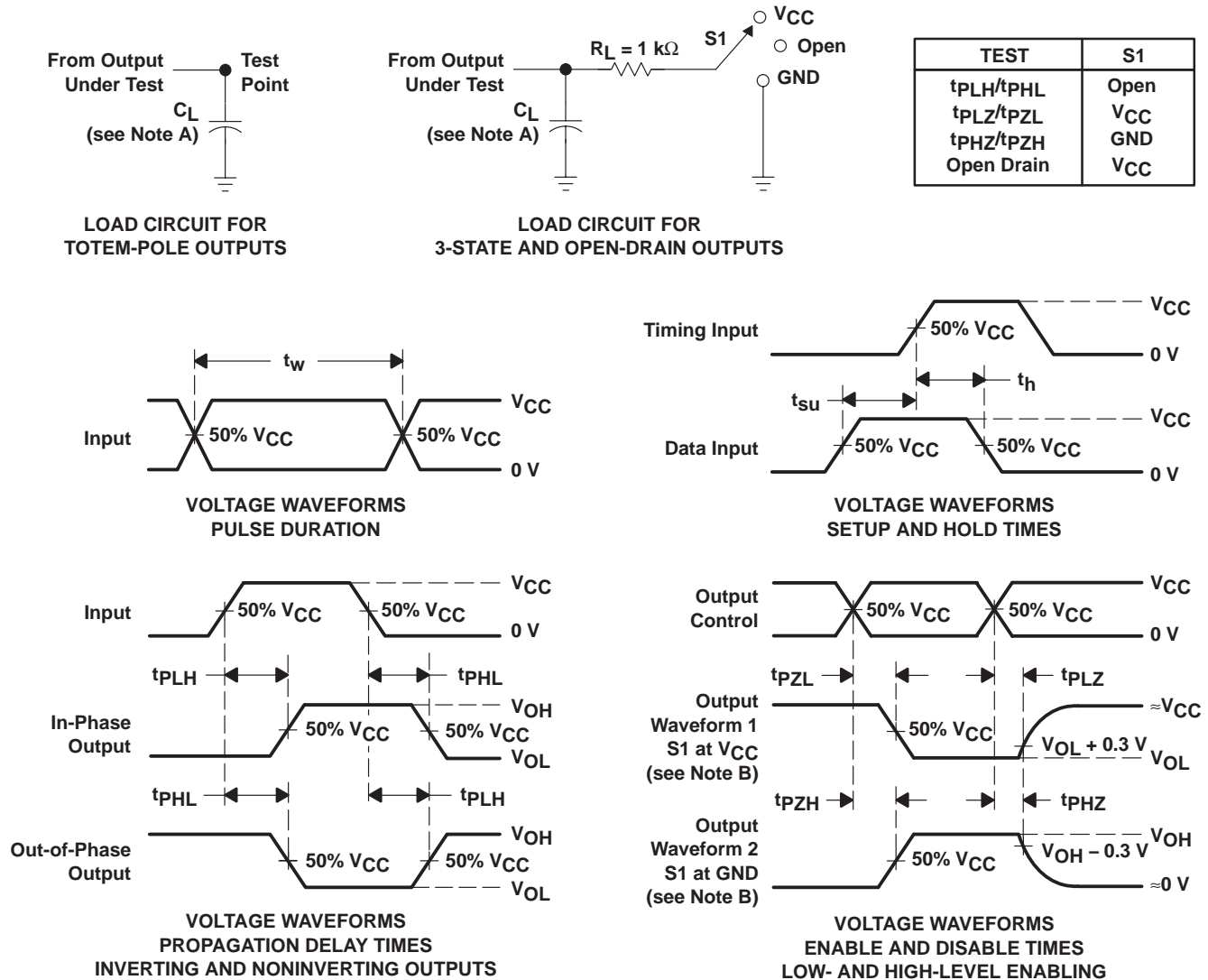
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|--|--|----------|------|------|
| C_{pd} Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 3.3 V | 14 | pF |
| | | 5 V | 16.4 | |



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| SN74LV240ADBLE | OBSOLETE | SSOP | DB | 20 | | None | Call TI | Call TI |
| SN74LV240ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LV240ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LV240ADW | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LV240ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LV240ANSR | ACTIVE | SO | NS | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LV240APW | ACTIVE | TSSOP | PW | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LV240APWLE | OBSOLETE | TSSOP | PW | 20 | | None | Call TI | Call TI |
| SN74LV240APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LV240APWT | ACTIVE | TSSOP | PW | 20 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

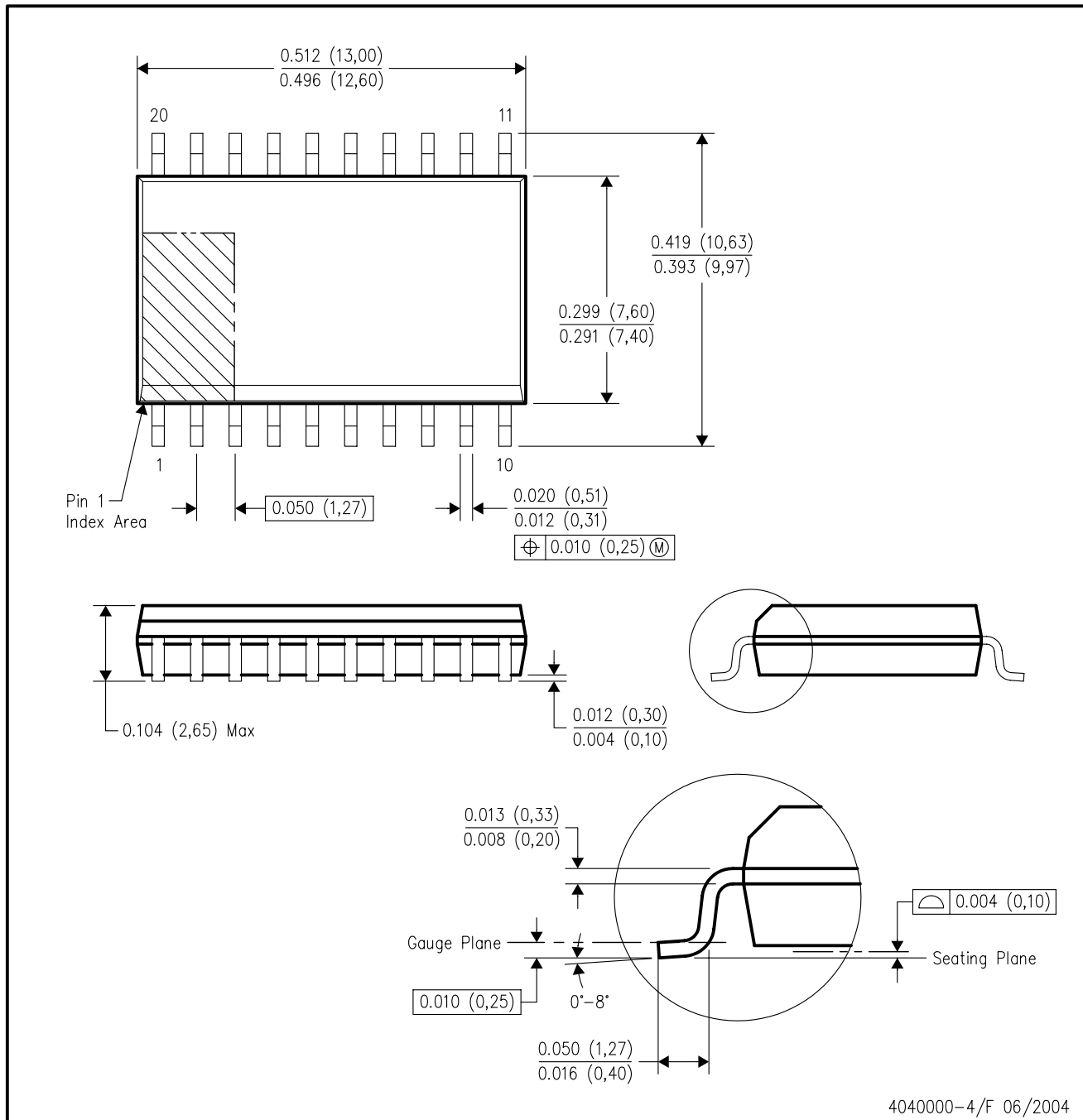
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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