*Designer's™ Data Sheet*

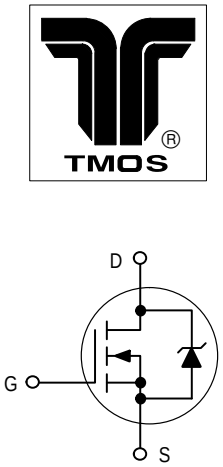
# TMOS E-FET™
# High Energy Power FET
# D²PAK for Surface Mount

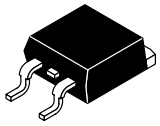
## N–Channel Enhancement–Mode Silicon Gate

**MTB8N50E**

**TMOS POWER FET**
**8.0 AMPERES**
**500 VOLTS**
**$R_{DS(on)}$ = 0.8 OHM**

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



**CASE 418B–02, Style 2**
**D²PAK**

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specifically Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 500 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 500 | Vdc |
| Gate–to–Source Voltage – Continuous<br>– Non–repetitive (tp ≤ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |
| Drain Current — Continuous @ $T_C$ = 25°C<br>— Continuous @ $T_C$ = 100°C<br>— Single Pulse (tp ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 8.0<br>5.0<br>32 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 125<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – STARTING $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, PEAK $I_L$ = 8.0 Apk, L = 16 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 510 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient<br>– Junction–to–Ambient (1) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | <br>°C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 sec. | $T_L$ | 260 | °C |

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**REV 1**

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 500 | — | — | Vdc |
| Temperature Coefficient (Positive) | | | — | 500 | — | mV/°C |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 500 Vdc, $V_{GS}$ = 0 Vdc) | | | — | — | 10 | |
| ($V_{DS}$ = 400 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | — | — | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | — | — | 100 | nAdc |
| **ON CHARACTERISTICS (1)** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 3.0 | 4.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | — | 6.3 | — | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 4.0 Adc) | | $R_{DS(on)}$ | — | 0.6 | 0.8 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc) | | $V_{DS(on)}$ | | | | Vdc |
| ($I_D$ = 8.0 Adc) | | | — | — | 7.2 | |
| ($I_D$ = 4.0 Adc, $T_J$ = 125°C) | | | — | — | 6.4 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 4.0 Adc) | | $g_{FS}$ | 4.0 | — | — | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | — | 1450 | 1680 | pF |
| Output Capacitance | | $C_{oss}$ | — | 190 | 264 | |
| Transfer Capacitance | | $C_{rss}$ | — | 45.4 | 144 | |
| **SWITCHING CHARACTERISTICS (2)** | | | | | | |
| Turn–On Delay Time | ($R_{Gon}$ = 9.1 Ω) | $t_{d(on)}$ | — | 15 | 50 | ns |
| Rise Time | | $t_r$ | — | 33 | 72 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | — | 40 | 150 | |
| Fall Time | | $t_f$ | — | 32 | 60 | |
| Gate Charge (see Figure 8) | ($V_{DS}$ = 400 Vdc, $I_D$ = 8.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | — | 40 | 64 | nC |
| | | $Q_1$ | — | 8.0 | — | |
| | | $Q_2$ | — | 17 | — | |
| | | $Q_3$ | — | 17.3 | — | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | | $V_{SD}$ | | | | Vdc |
| ($I_S$ = 8.0 Adc, $V_{GS}$ = 0 Vdc) | | | — | 1.2 | 2.0 | |
| ($I_S$ = 8.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | — | 1.1 | — | |
| Reverse Recovery Time | ($I_S$ = 8.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | — | 320 | — | ns |
| | | $t_a$ | — | 179 | — | |
| | | $t_b$ | — | 141 | — | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | — | 3.0 | — | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | — | 4.5 | — | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | — | 7.5 | — | |

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

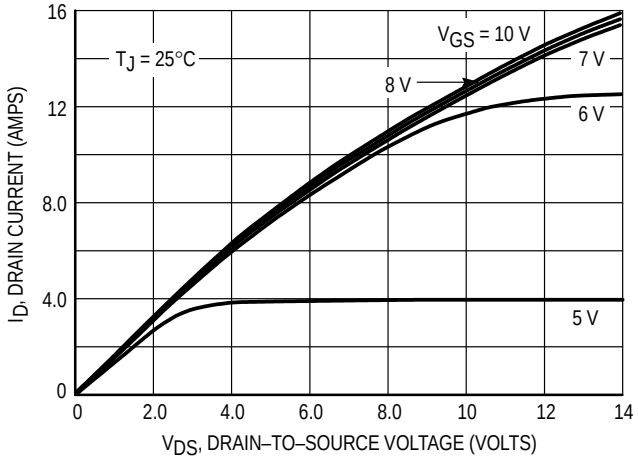



**Figure 1. On–Region Characteristics**

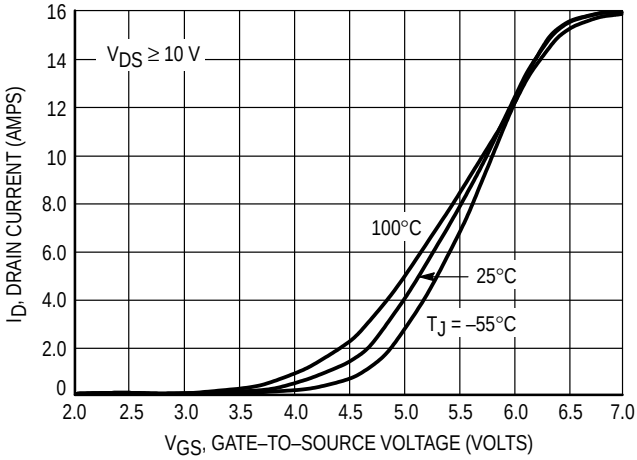



**Figure 2. Transfer Characteristics**

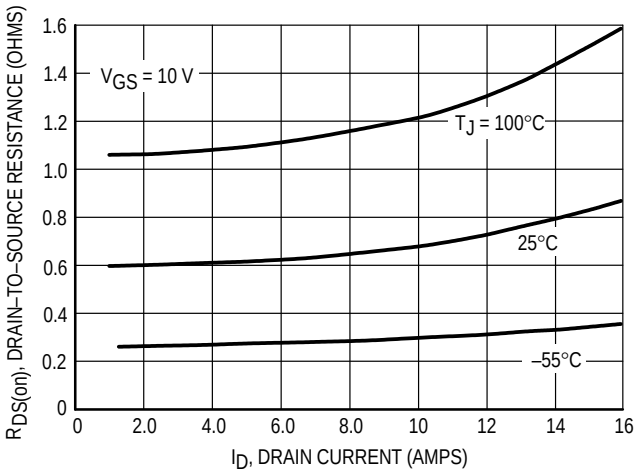



**Figure 3. On–Resistance versus Drain Current and Temperature**

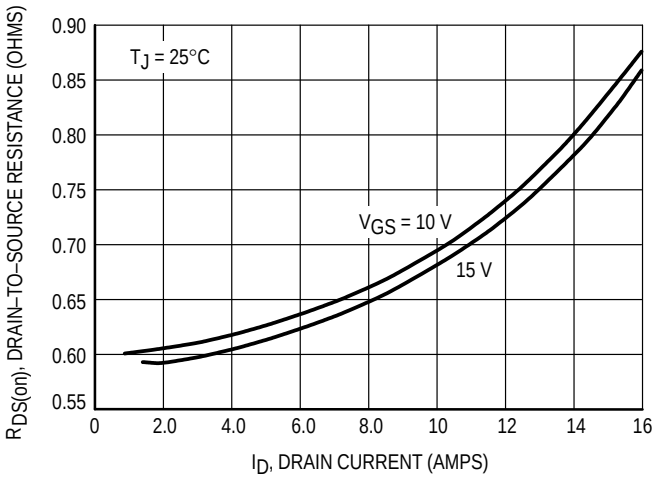



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

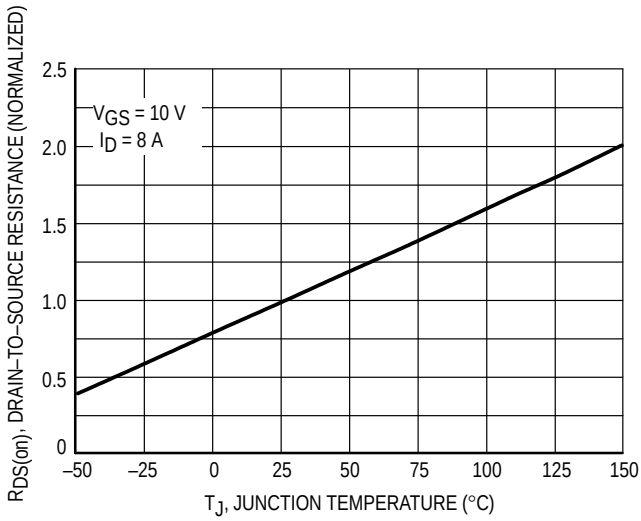



**Figure 5. On–Resistance Variation with Temperature**

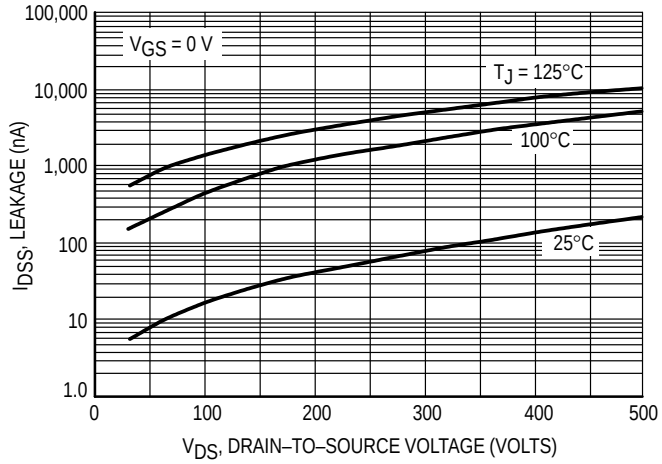



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## TYPICAL ELECTRICAL CHARACTERISTICS

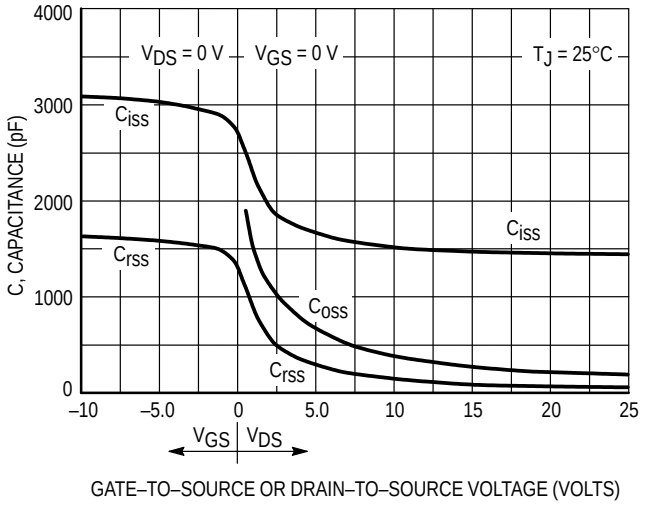



**Figure 7. Capacitance Variation**

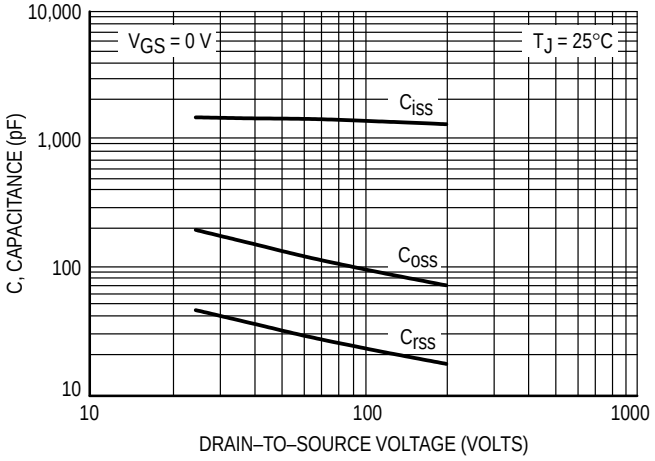



**Figure 8. High Voltage Capacitance Variation**

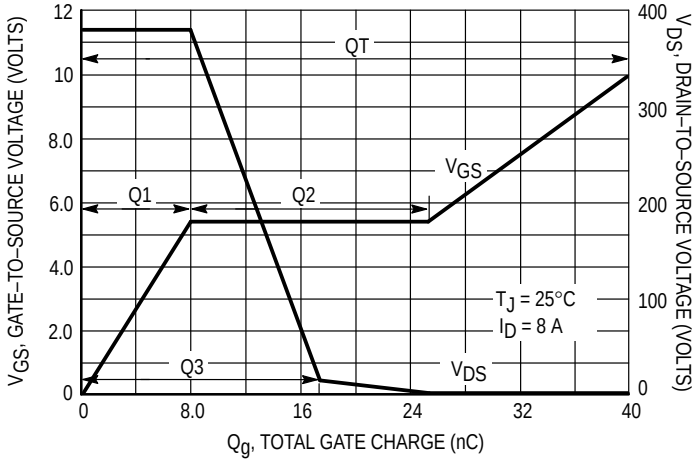



**Figure 9. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

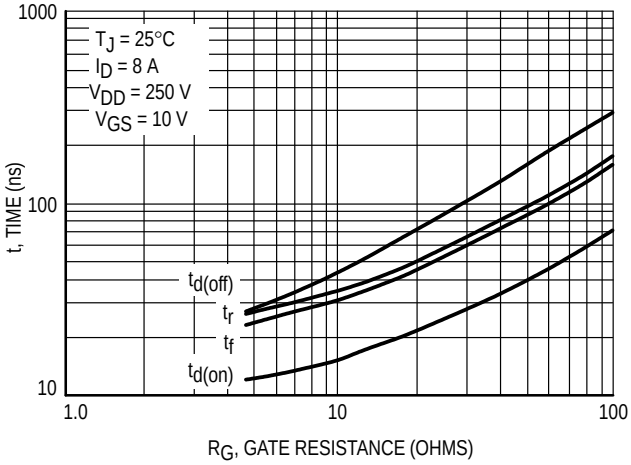



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

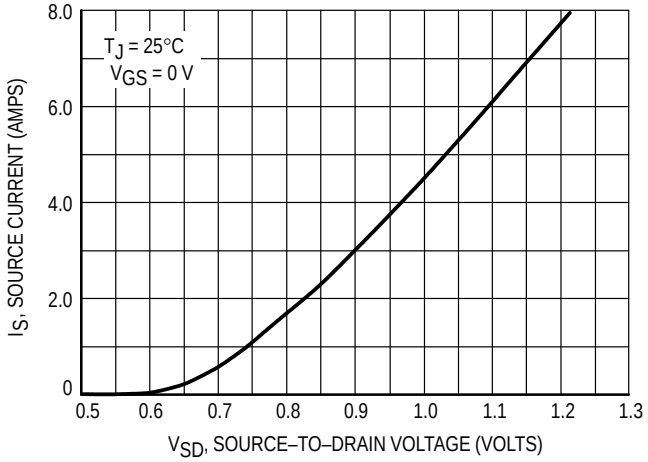



**Figure 11. Diode Forward Voltage versus Current**

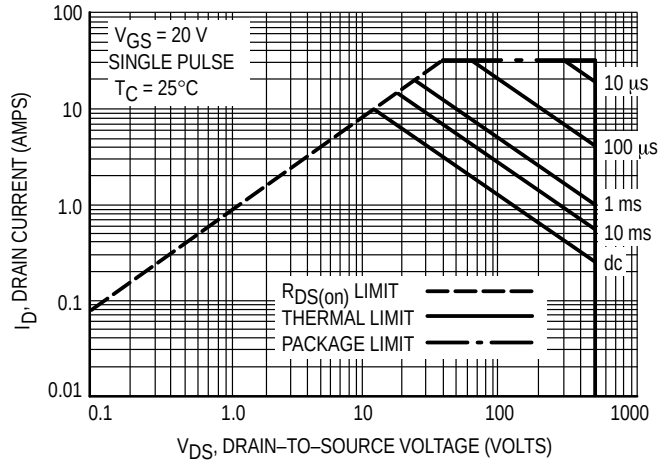



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

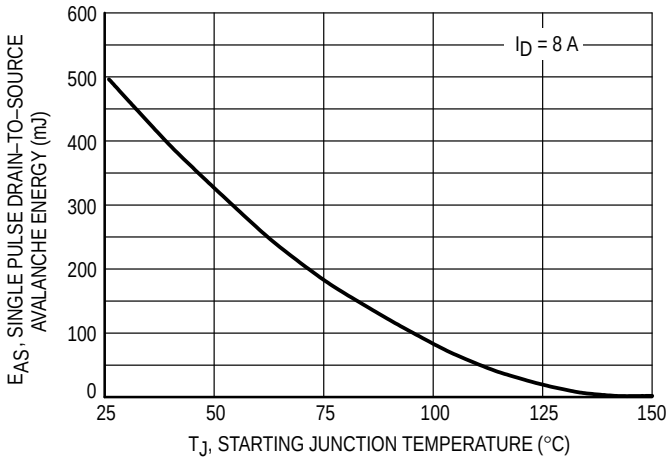



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

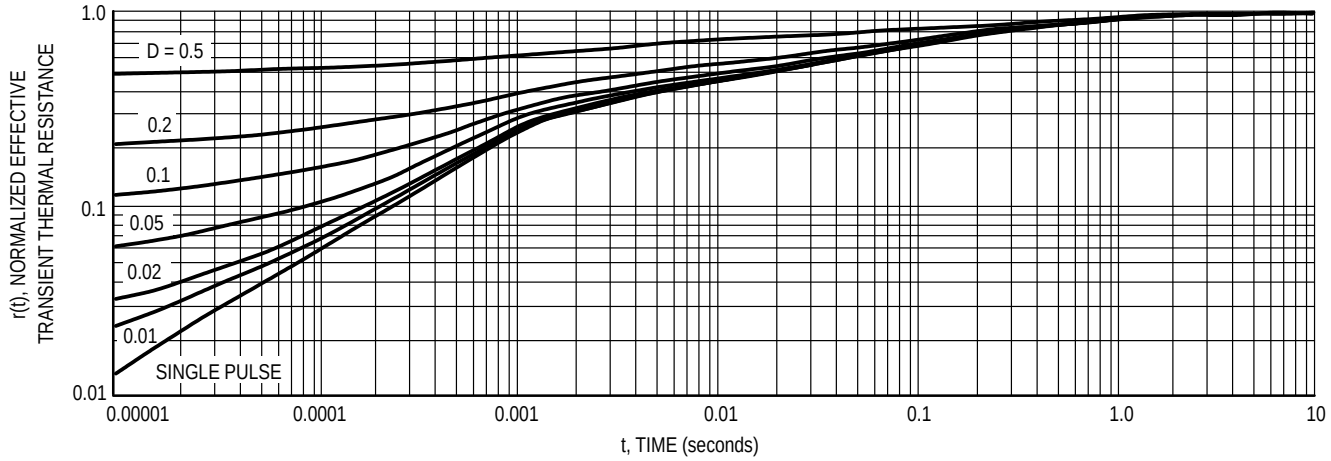
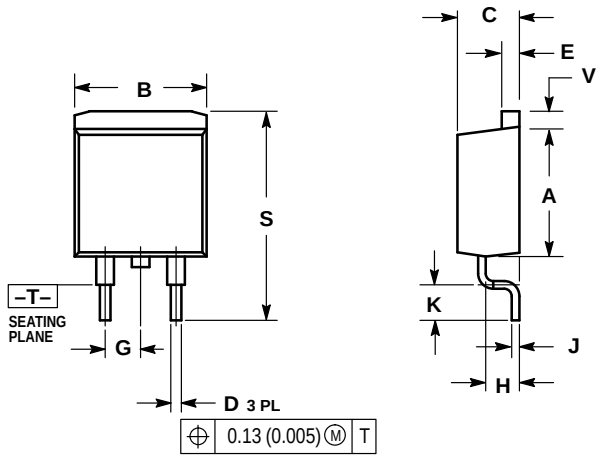



**Figure 14. Thermal Response**

## PACKAGE DIMENSIONS




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.340 | 0.380 | 8.64 | 9.65 |
| B | 0.380 | 0.405 | 9.65 | 10.29 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.020 | 0.035 | 0.51 | 0.89 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.080 | 0.110 | 2.03 | 2.79 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.090 | 0.110 | 2.29 | 2.79 |
| S | 0.575 | 0.625 | 14.60 | 15.88 |
| V | 0.045 | 0.055 | 1.14 | 1.40 |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

**CASE 418B–02**
**ISSUE B**



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