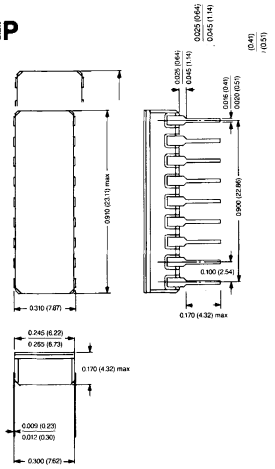
FEATURES

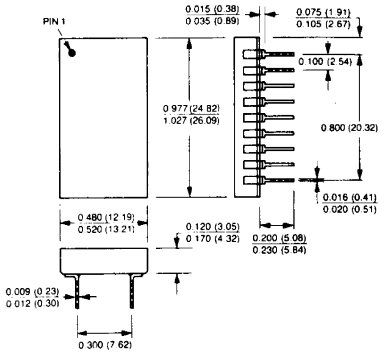
- 2.5μsec Maximum Conversion Time (MN5130, MN5140)
- Small 18-pin DIP
- ±1/2 LSB Linearity and No Missing Codes Guaranteed Over Temperature
- Full Mil Operation −55°C to +125°C
- MIL-PRF-38534 Screening Optional.

18 PIN DIP

MN5120



MN5130 and MN5140



Dimensions in Inches (millimeters)

DESCRIPTION

The MN5120, MN5130 and MN5140 Series are a family of 8-bit, high-speed, successive approximation analog-to-digital converters in small, 18-pin, hermetically sealed dual-in-line packages. All devices incorporate our own thin-film resistor networks and are functionally laser trimmed as complete devices to meet all published specifications without external adjustments.

Each Series offers analog input ranges of 0 to +10V, 0 to −10V, ±5V and ±10V. MN5120 Series devices complete a conversion in 6μsec. MN5130 and MN5140 Series devices complete a conversion in 2.5μsec. The MN5120 and MN5130 Series devices operate from ±15V supplies. MN5140 devices operate from ±12V supplies. All units require a +5V logic supply.

These A/D's are fully specified and tested for linearity and accuracy at room temperature and at both the high and low extremes of the specified operating temperature range. Devices may be ordered for either 0°C to +70°C or −55°C to +125°C ("H" models) operation, and all guarantee ±1/2 LSB linearity over their entire operating temperature range. Full scale absolute accuracy is guaranteed to be better than ±1 LSB at +25°C and better than ±2LSBs over temperature. For military/aerospace or harsh-environment commercial/industrial application, "H/B CH" are fully screened to MIL-PRF-38534.

Low cost, 8-bit resolution and high conversion speeds make MN5120, MN5130 and MN5140 Series A/D's excellent choices for digitizing data in microprocessor-based systems for industrial-control and monitoring applications. Adjustment-free operation, accuracy and linearity specs guaranteed from −55°C to +125°C, and optional MIL-PRF-38534 screening make them excellent choices for military/aerospace and avionics applications.

MN5120 MN5130 MN5140 SERIES 8-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	−55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
Positive Supply (+Vcc, Pin 1)	+18 Volts
Negative Supply (−Vcc, Pin 18)	−18 Volts
Logic Supply (+Vdd, Pin 12)	−0.5 to +7 Volts
Analog Input (Pin 2)	±15 Volts
Digital Inputs (Pins 8, 10)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN51XX H/B CH

Standard Part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated)

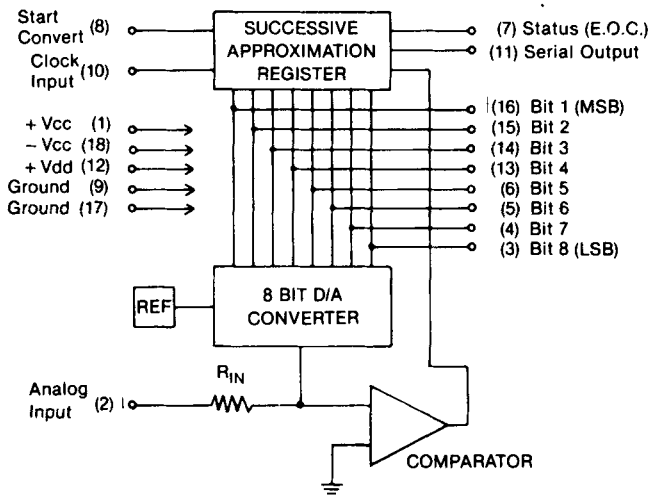
ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range: MN5120, MN5130, MN5140		0 to −10		Volts
MN5121, MN5131, MN5141		−5 to +5		Volts
MN5122, MN5132, MN5142		−10 to +10		Volts
MN5123, MN5133, MN5143		0 to +10		Volts
Input Impedance: MN5120, MN5130, MN5140		5		KΩ
MN5121, MN5131, MN5141		5		KΩ
MN5122, MN5132, MN5142		10		KΩ
MN5123, MN5133, MN5143		5		KΩ
DIGITAL INPUTS (ALL UNITS)				
Logic Levels: Logic "1"	2.0			Volts
Logic "0"			0.8	Volts
Clock Input (Note 1): Pulse Width High	25			nSec
Pulse Width Low	50			nSec
Loading (Note 2)			1	TTL Load
Frequency (Note 3): MN5120 Series			1.33	MHz
MN5130 Series			3.2	MHz
MN5140 Series			3.2	MHz
Start Convert Input: Loading High (Note 2)			2	TTL Loads
Loading Low (Note 2)			1	TTL Load
Setup Time Start Low to Clock (Note 4)	20			nSec
DIGITAL OUTPUTS (ALL UNITS)				
Logic Levels: Logic "1"	2.4	3.6		Volts
Logic "0"		0.2	0.4	Volts
Output Coding (Note 5): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Output Drive Capability, All Outputs (Note 2): Logic "1"	11			TTL Loads
Logic "0"	5			TTL Loads
TRANSFER CHARACTERISTICS (ALL UNITS)				
Linearity Error (Note 6): 0°C to +70°C		±¼	±½	LSB
−55°C to +125°C ("H" Models)			±½	LSB
Differential Linearity Error		±½		LSB
No Missing Codes	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 7, 8):				
+25°C		±½	±1	LSB
−55°C to +125°C (Note 10)		±1	±2	LSB
Zero Error (Notes 7, 8): +25°C		±¼	±1	LSB
−55°C to +125°C (Note 10)		±½	±1	LSB
Unipolar Offset Error, 0 to +10V Range (Notes 7, 8):				
+25°C		±¼	±1	LSB
−55°C to +125°C (Note 10)		±½	±1	LSB
Unipolar Offset Error, 0 to −10V Range (Notes 7, 8):				
+25°C		±½	±1	LSB
−55°C to +125°C (Note 10)		±1	±2	LSB
Bipolar Offset Error, ±5V and ±10V Ranges (Notes 7, 8):				
+25°C		±½	±1	LSB
−55°C to +125°C (Note 10)		±1	±2	LSB
Offset Drift (Note 9): 0 to +10V Range		±1		ppm of FSR/°C
0 to −10V Range		±10		ppm of FSR/°C
±5V and ±10V Ranges		±10		ppm of FSR/°C
Gain Error (Note 7)		±0.1		%
Gain Drift		±20		ppm/°C

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (Note 3): MN5120 Series MN5130 Series MN5140 Series			6 2.5 2.5	µSec µSec µSec
POWER SUPPLY REQUIREMENTS (ALL UNITS)				
Power Supply Range (Note 11): ± Vcc + Vdd	± 11 + 4.75	 + 5.00	± 17 + 5.25	Volts Volts
Power Supply Rejection (Note 11): + Vcc – Vcc		± 0.02 ± 0.01		%FSR/%Vs %FSR/%Vs
Current Drain (Note 11): + Vcc – Vcc + Vdd		12 – 10 70	16 – 18 100	mA mA mA
Power Consumption (All Units)		680	1010	mW

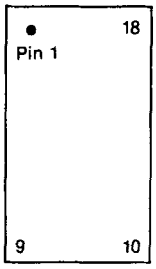
SPECIFICATION NOTES:

1. The clock may be asymmetrical with minimum positive or negative pulse width. See Note 3.
2. One TTL load is defined as sinking 40 µA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.
3. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) output pulse. See Timing Diagram. For the MN5120 series, the maximum conversion time of 6 µSec corresponds to an external clock frequency of 1.33 MHz. For the MN5130 and MN5140 series, the maximum conversion time of 2.5 µSec corresponds to an external clock frequency of 3.2 MHz. Micro Networks guarantees Absolute Accuracy and Linearity at and below these clock frequencies.
4. In order to reset the converter, START CONVERT must be brought low at least 20 nSec prior to a low to high clock transition. See Timing Diagram.
5. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding (page 8) and Timing Diagram.
6. Micro Networks tests and guarantees maximum linearity error at room temperature and at both extremes of the specified operating temperature range.
7. See Absolute Accuracy section below for explanation of how Micro Networks tests and specifies Absolute Accuracy, Offset, Gain and Zero Errors.
8. 1 LSB for an 8 bit converter corresponds to ± 0.39%FSR. See Note 9.
9. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected input range. For the ± 10V input range, FSR is 20 volts, and 1 LSB is equal to 78 mV. For the 0 to ± 10V and ± 5V ranges, FSR is 10 volts, and 1 LSB is equal to 39 mV.
10. For Commercial Models, this specification applies over the 0°C to + 70°C range. See Ordering Information.
11. For the MN5120 and MN5130 Series the positive and negative power supply (+ Vcc and – Vcc) requirements are + 15V and – 15V. For the MN5140 series the + Vcc and – Vcc requirements are + 12V and – 12V. All units will operate over a ± Vcc range of ± 11V to ± 17V with reduced accuracy, and all units require a + 5V logic supply (+ Vdd).

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Positive Supply (+ Vcc)	18	Negative Supply (– Vcc)
2	Analog Input	17	Ground
3	Bit 8 (LSB)	16	Bit 1 (MSB)
4	Bit 7	15	Bit 2
5	Bit 6	14	Bit 3
6	Bit 5	13	Bit 4
7	Status (E.O.C.)	12	+ 5V Supply (+ Vdd)
8	Start Convert	11	Serial Output
9	Ground	10	Clock Input

ABSOLUTE ACCURACY ERROR

A given digital output code is valid for a band of analog input voltages that is ideally 1 LSB wide. This is demonstrated in the next column where portions of the theoretical analog input/digital output transfer function of the MN5122, MN5132, and MN5142 A/D converters (±10V input range) are sketched.

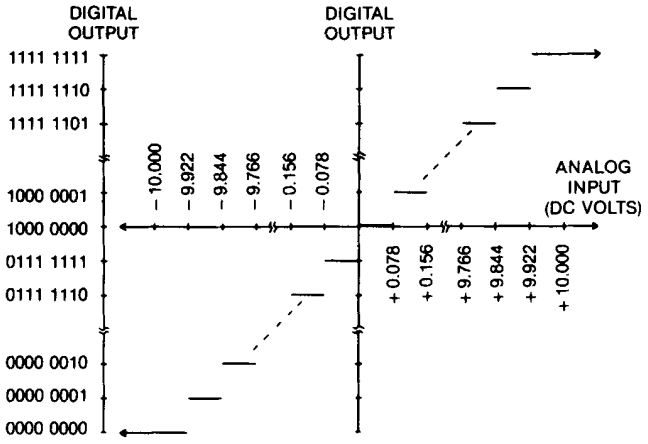
Notice that, ideally, any analog input between zero and +0.078V (1 LSB = 0.078 volts) will give a digital output of 1000 0000. If we assign this code to the nominal midrange of the analog input band for which it is valid, we can say that the 1000 0000 digital code corresponds to analog inputs of +0.039V ±0.039V (+0.039V ± ½ LSB). The ± ½ LSB is a quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error and its magnitude can be reduced only by going to higher resolution converters.

It is difficult and time consuming to measure the center of a quantization level (the +0.039 volts in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the voltages at which the digital outputs change from one code to the next. The *Absolute Accuracy Error* of a voltage input A/D converter is the difference between the actual, *unadjusted*, analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR (see Note 9 above). Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors.

For the MN5120/30/40 A/D Converters, we test Absolute Accuracy Error at both endpoints of unipolar input ranges and at both endpoints and the midpoint of bipolar input ranges. These tests are performed at room temperature and at the high and low extremes of the specified operating temperature range. The specifications appear in the table as the Full Scale Absolute Accuracy and Zero Errors.

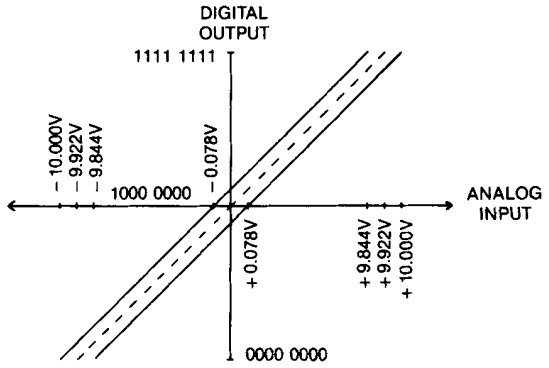
EXAMPLE: Return to the ideal analog input/digital output transfer function of the MN5122, MN5132, and MN5142 sketched above. Notice that the digital output data should change from 0000 0000 to 0000 0001 when the input voltage increases from −10.000V to −9.922V. It should change from 0000 0001 back to 0000 0000 as the input voltage is decreased from some more positive voltage to −9.922V. This voltage, −9.922V, is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "0". The 0111 1111 to 1000 0000 transition (the major transition) ideally occurs at the zero volt analog input. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "1", is ideally +9.922V.

For the MN5122H, MN5132H, and MN5142H (±10V input range, −55°C to +125°C operation), Micro Networks measures the three transition voltages just discussed at −55°C, +25°C, and +125°C. We guarantee that the positive and negative full scale LSB transition voltages will be within ±1 LSB (±78mV) of their ideal values at +25°C and within ±2 LSB's (±156mV)of their ideal values over the entire −55°C to +125°C operating temperature range. This is our Full Scale Absolute Accuracy Error specification. We also guarantee that the major transition voltage will be within ±1 LSB (±78mV) of its ideal value (zero volts) over the entire −55°C to +125°C operating temperature range. This is our Zero Error specification.

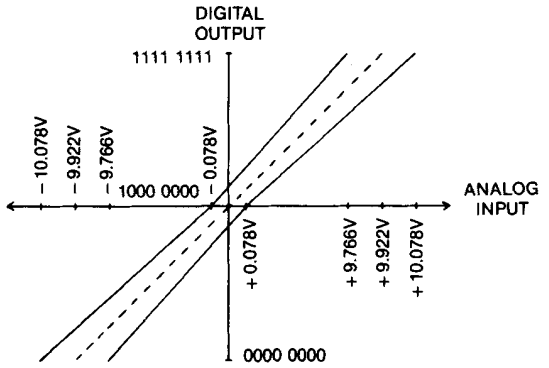


These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5122H, MN5132H, and MN5124H, that the actual transfer function will be ± ½ LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at −55°C and +125°C.

For temperatures intermediate to +25°C and −55°C or +125°C, maximum absolute accuracy errors can be interpolated. At +75°C, for example, Full Scale Absolute Accuracy Error will be ±1.5 LSB's.



ABSOLUTE ACCURACY +25°C



ABSOLUTE ACCURACY −55°C, +125°C

Unipolar and Bipolar Offset Errors are both Absolute Accuracy Errors. Their definitions differ with respect to where along the converter's analog input/digital output transfer function the errors are to be measured, i.e., different analog errors are measured at different digital output code transitions.

OFFSET ERROR—Space does not permit a theoretical discussion of the definitions and origins of Offset Error. Suffice it to say that for the MN5120, MN5130, and MN5140 Series A/D's, Offset Error is the difference between the ideal and the actual input voltages at which the 0000 0000 to 0000 0001 output transition takes place. It is the Absolute Accuracy Error measured for the 0000 0000 to 0000 0001 transition. For the MN5123, MN5133, and MN5143 converters (0 to +10V input range), Unipolar Offset Error is the same as Zero Error, and it indicates how accurate the converters will be when the analog input is around zero volts. For the MN5120, MN5130, and MN5140 converters (0 to −10V input range), Unipolar Offset Error is equivalent to Full Scale Absolute Accuracy Error, and it indicates how accurate the converters will be around −10 volts. For the bipolar converters (±5V and ±10V input ranges), Bipolar Offset Error is also equivalent to Full Scale Absolute Accuracy Error, and it indicates how accurate the converters will be around their negative full scale input points.

It is redundant to specify Offset Errors after specifying Full Scale Absolute Accuracy and Zero Errors the way Micro Networks does. We have provided the Offset Error specs to simplify comparing the MN5120, MN5130, and MN5140 Series to other 8 bit A/D's. Be sure you clearly understand each manufacturer's specification definitions before you compare converters solely on a data sheet basis.

GAIN ERROR—Gain Error is the difference between the ideal and the measured values of a converter's Full Scale Range (minus 2 LSB); it is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 1111 1110 to 1111 1111 transition minus that measured for the 0000 0000 to 0000 0001 transition.

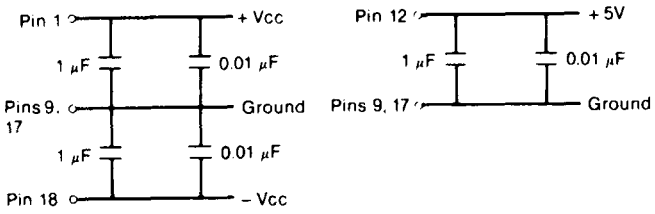
See the Converter Tutorial Section of the Micro Networks Applications Manual and Product Guide for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5120, MN5130, and MN5140 Series converters. The units' two GROUND pins (pins 9 and 17) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 9 and 17 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

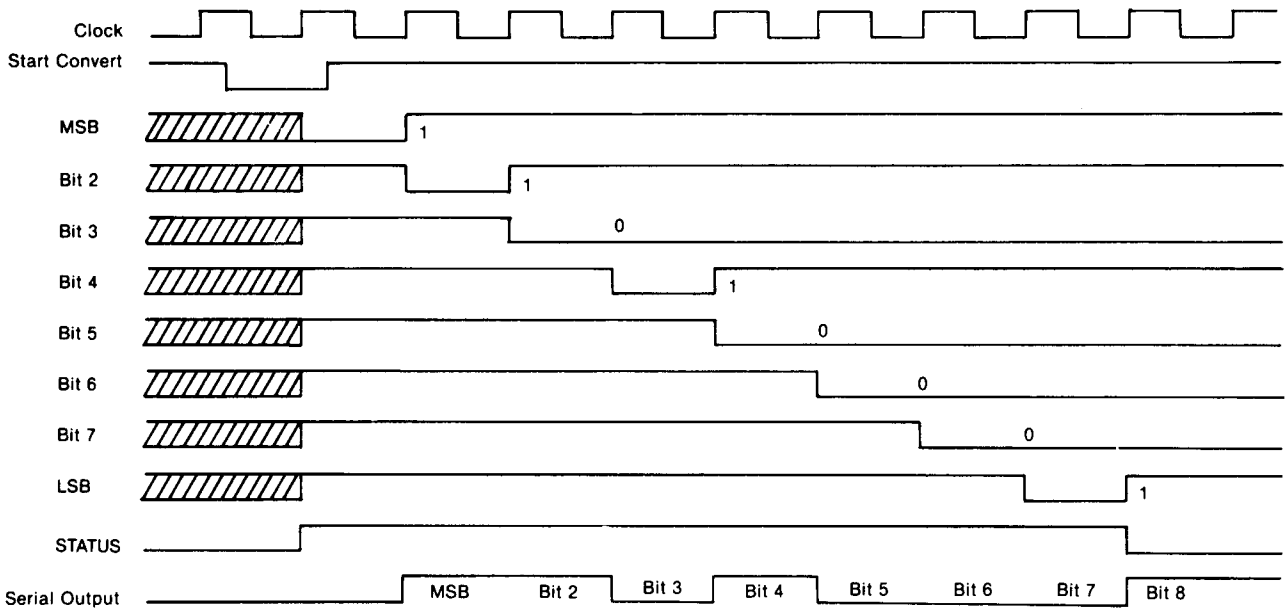
POWER SUPPLY DECOUPLING



DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's START CONVERT (Pin 8) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the STATUS output (Pin 7) is set to logic "1" (See Timing Diagram). The START CONVERT must now be brought high again for the conversion to continue. If the START is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the START has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the STATUS output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

TIMING DIAGRAM



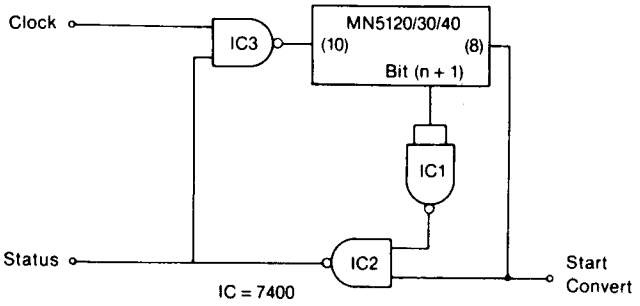
TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 1101 0001 which corresponds to 8.164V on the 0 to +10V (MN5123/33/43) input range. See Output Coding.
2. Conversion Time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", STATUS = "1") by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 20 nSec prior to the clock transition. Holding the START low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the START has returned high.
4. The delay between the resetting clock edge and STATUS actually rising to a "1" is 50 nSec maximum.
5. The START CONVERT may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 50 nSec (maximum) after the STATUS (E.O.C.) output has returned low. Parallel output data will remain valid and the STATUS output low until another conversion is initiated.
8. For continuous conversion, connect the STATUS output pin (Pin 7) to the START CONVERT input (Pin 8). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

CONTINUOUS CONVERTING—The MN5120/30/40 Series A/D converters can be made to continuously convert by tying the STATUS output (Pin 7) to the START CONVERT input (Pin 8). In this configuration, STATUS (START CONVERT) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing STATUS (START CONVERT) high again. The MSB will be set on the next rising clock edge. The result is that the STATUS will go low for approximately one clock period following each conversion. Please read the section describing the STATUS output. See page 7 for continuous conversions while short cycling.

SHORT CYCLING — For applications requiring less than 8 bits resolution, the MN5120/30/40 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.

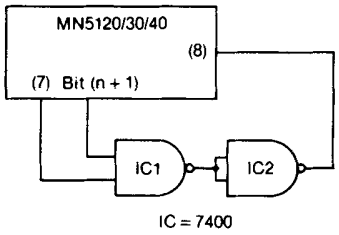
SHORT CYCLING SINGLE CONVERSION



Assuming a conversion is already in progess, bit (n + 1) will go low as bit n is being set (see Timing Diagram). Since the START CONVERT signal is high at this time, STATUS (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, START CONVERT is brought low driving STATUS high and gating on the clock. The first rising clock edge the converter sees with START CONVERT low will reset the converter bringing bit (n + 1) high again. Now STATUS will remain high as START CONVERT is brought back high allowing the conversion to continue. Therefore, in this configuration, STATUS and START CONVERT function normally, i.e., the same as STATUS and START CONVERT for a converter not being short cycled.

SHORT CYCLING AND CONTINUOUS CONVERTING — A previous section described how continuous converting for 8 bits could be accomplished by simply tying the STATUS output back to the START CONVERT input. To continuously convert at n bits, one simply has to tie the bit (n + 1) output back to the START CONVERT input. The bit (n + 1) output acts like a STATUS when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n + 1) comes on as a "1" and the conversion process comes on at bit (n + 2). This situation can be avoided by making the START CONVERT input the AND function of bit (n + 1) and the STATUS output.

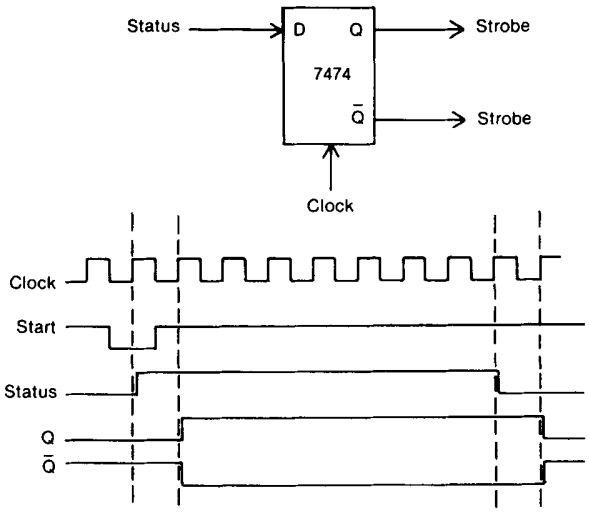
SHORT CYCLING CONTINUOUS CONVERTING



If one is already using the circuit described in the section labeled SHORT CYCLING, one can short cycle and continuously convert by making the START CONVERT input the AND function of STATUS (IC2) and STATUS (pin 7) outputs.

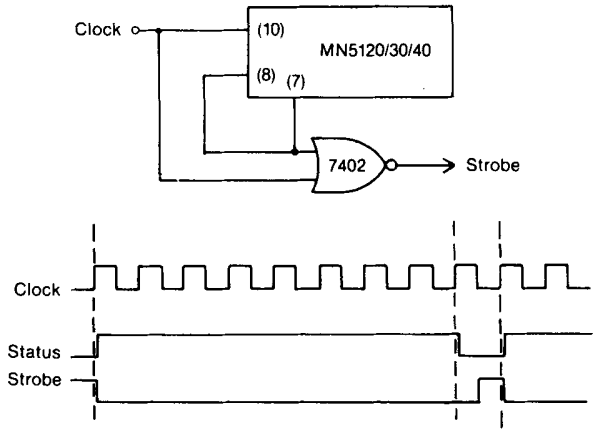
STATUS OUTPUT—The STATUS or END OF CONVERSION (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 50 nSec after STATUS has returned low. Therefore, an adequate delay must be provided if STATUS is to be used to strobe latches to hold output data. Simple gate delays can be employed or the STATUS can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after STATUS changes.

LATCHING OUTPUT DATA



If continuously converting, the STATUS (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse ½ period wide, ½ period after the STATUS output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

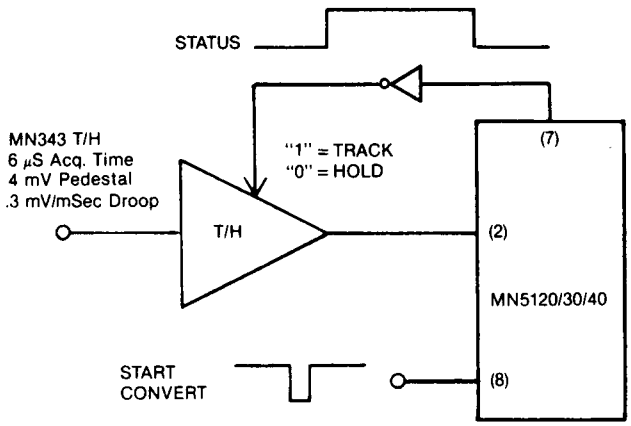
LATCHING DATA CONTINUOUS CONVERSIONS



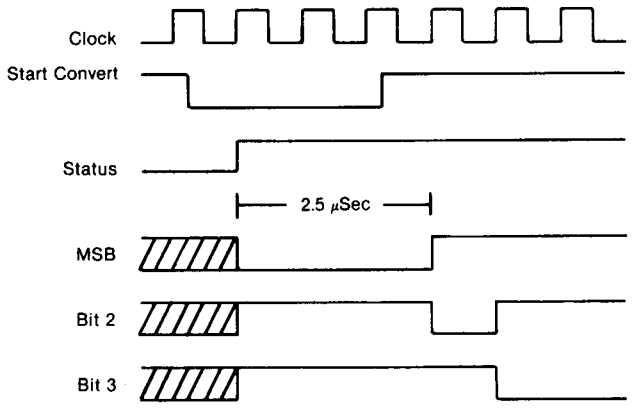
USING A TRACK AND HOLD AMP WITH MN5120/30/40 A/D's —The error that results when trying to convert moving analog signals with a successive approximation A/D can be as great as the amount the analog signal changes during a single A/D conversion time. If this error is unacceptable, a Track and Hold (T/H) or Sample and Hold (S/H) amplifier can be placed between the analog signal source and the A/D converter. A careful error analysis will be necessary to determine if the T/H is actually reducing and not increasing overall error. T/H parameters such as aperture uncertainty, gain accuracy, pedestal error and droop rate will have to be contended with (see the tutorial section of the Micro Networks' Applications Manual and Product Guide for a complete discussion of T/H parameters).

Normally, the T/H can be controlled directly by the A/D's STATUS output. Typical connections are shown on the next page. The STATUS output changes from a "0" to a "1" when the converter is reset. This drives the T/H from the track to the hold mode. At the end of conversion, STATUS returns to a "0" restoring the T/H to the track mode.

DRIVING A TRACK AND HOLD



Recall that if the START CONVERT pulse is brought high immediately after the converter has been reset, the MSB will be finalized one clock period later (see Timing Diagram). Care should be taken to ensure that aperture delay time and track-to-hold settling time do not contribute errors. If necessary, the width of the START CONVERT pulse can be increased to allow more time between the T/H being commanded into the hold mode (STATUS = "1") and the MSB being set. Recall that output bits do not begin to get set until after the START CONVERT has returned high. The example below shows a 2.25 μSec delay to allow for track to hold settling. Clock frequency = 1.33 MHz; 1 period = 0.75 μSec.



INPUT VOLTAGE AND OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT	
MN5120,30,40 0 to −10V	MN5121,31,41 ±5V	MN5122,32,42 ±10V	MN5123,33,43 0 to +10V	MSB	LSB
0.000	+5.000	+10.000	+10.000	1111	1111
−0.039	+4.961	+9.922	+9.961	1111	1110*
−4.961	+0.039	+0.078	+5.039	1000	0000*
−5.000	0.000	0.000	+5.000	0000	0000*
−5.039	−0.039	−0.078	+4.961	0111	1110*
−9.961	−4.961	−9.922	+0.039	0000	0000*
−10.000	−5.000	−10.000	0.000	0000	0000

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as 0 will change from "1" to a "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages.

EXAMPLE: For an MN5122 (±10V analog input range) the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.922 volts. Subsequently, any input voltage more negative than −9.922 volts will give a digital output of all "0's". The transition from digital output 0111 1111 to 1000 0000 will ideally occur at an input of zero volts, and the 1111 1110 to 1111 1111 transition should occur at +9.922 volts. An input greater than +9.922 volts will give all "1's".

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