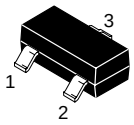
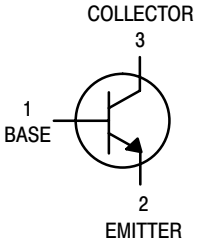
Low Noise Transistors
NPN Silicon

MMBT5088LT1
MMBT5089LT1

MMBT5089LT1 is a Preferred Device



CASE 318–08, STYLE 6
SOT–23 (TO–236AF)



MAXIMUM RATINGS

Rating	Symbol	5088LT1	5089LT1	Unit
Collector–Emitter Voltage	V_{CEO}	30	25	Vdc
Collector–Base Voltage	V_{CBO}	35	30	Vdc
Emitter–Base Voltage	V_{EBO}	4.5		Vdc
Collector Current — Continuous	I_C	50		mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board[1] T_A = 25°C	P_D	225	mW
Derate above 25°C		1.8	mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,[2] T_A = 25°C	P_D	300	mW
Derate above 25°C		2.4	mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

MMBT5088LT1 = 1Q; MMBT5089LT1 = 1R

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MMBT5088	$V_{(BR)CEO}$	30	—	Vdc
	MMBT5089		25	—	
Collector–Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MMBT5088	$V_{(BR)CBO}$	35	—	Vdc
	MMBT5089		30	—	
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	MMBT5088	I_{CBO}	—	50	nAdc
(V_{CB} = 15 Vdc, I_E = 0)	MMBT5089		—	50	
Emitter Cutoff Current ($V_{EB(off)}$ = 3.0 Vdc, I_C = 0)	MMBT5088	I_{EBO}	—	50	nAdc
($V_{EB(off)}$ = 4.5 Vdc, I_C = 0)	MMBT5089		—	100	

1. FR–5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 1
Publication Order Number:
MMBT5088LT1/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	MMBT5088		300	900	
	MMBT5089		400	1200	
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	MMBT5088		350	—	
	MMBT5089		450	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MMBT5088		300	—	
	MMBT5089		400	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			—	0.5	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			—	0.8	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T			MHz
(I_C = 500 μAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)			50	—	
Collector–Base Capacitance		C_{cb}			pF
(V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz emitter guarded)			—	4.0	
Emitter–Base Capacitance		C_{eb}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz collector guarded)			—	10	
Small Signal Current Gain		h_{fe}			—
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	MMBT5088		350	1400	
	MMBT5089		450	1800	
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 10 kΩ, f = 1.0 kHz)	MMBT5088		—	3.0	
	MMBT5089		—	2.0	

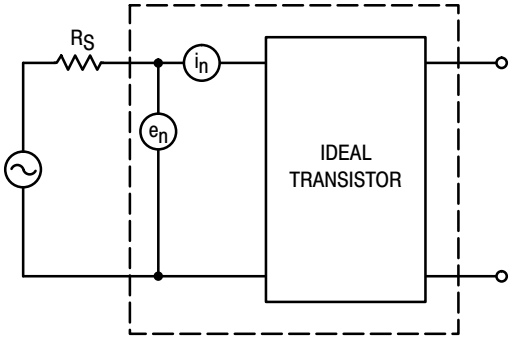


Figure 1. Transistor Noise Model

NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

NOISE VOLTAGE

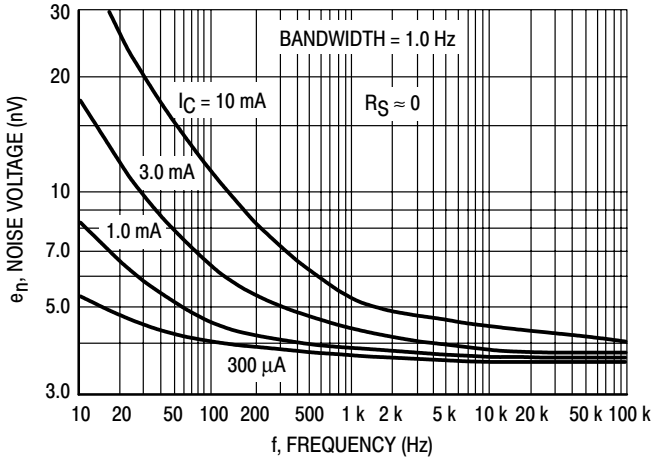


Figure 2. Effects of Frequency

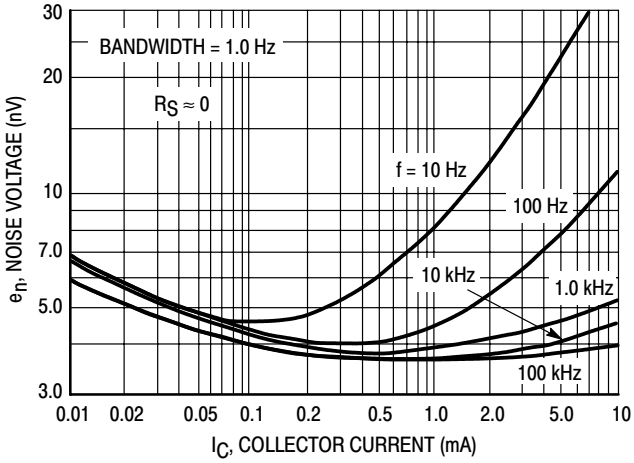


Figure 3. Effects of Collector Current

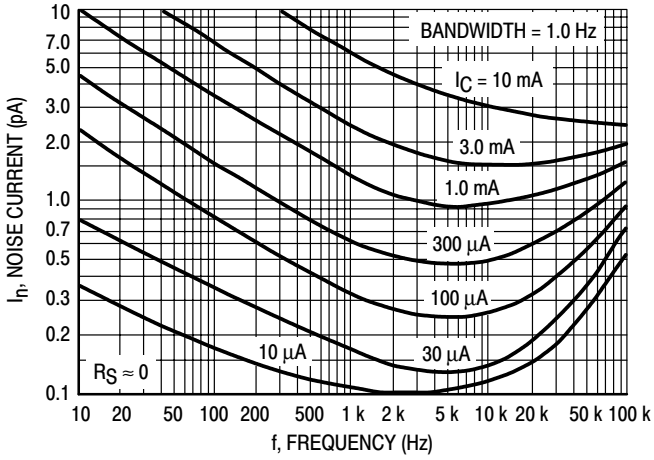


Figure 4. Noise Current

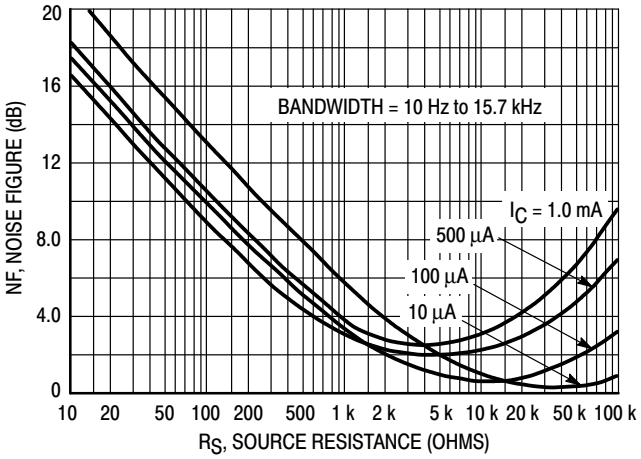


Figure 5. Wideband Noise Figure

100 Hz NOISE DATA

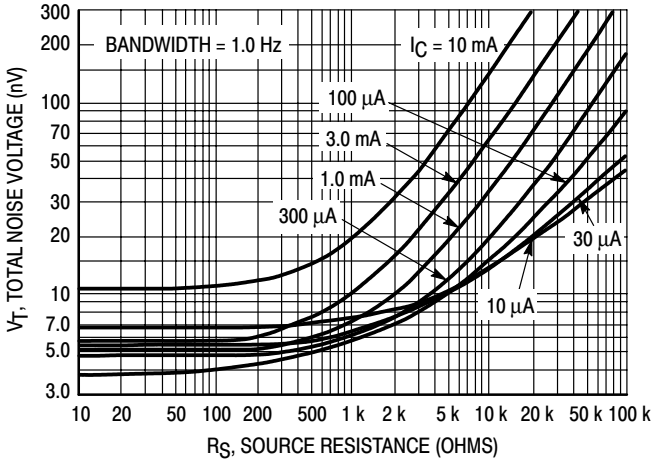


Figure 6. Total Noise Voltage

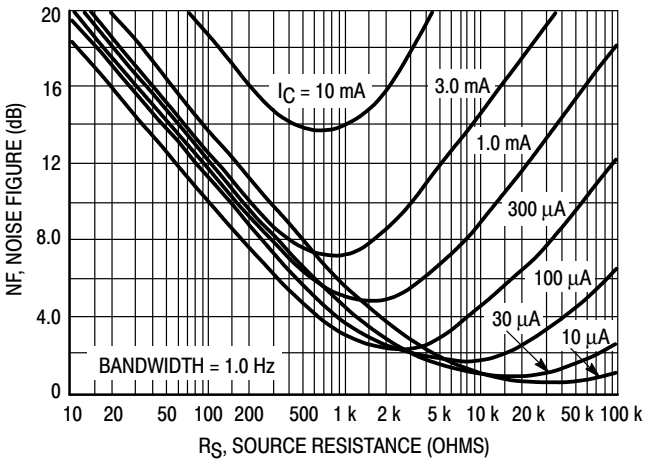


Figure 7. Noise Figure

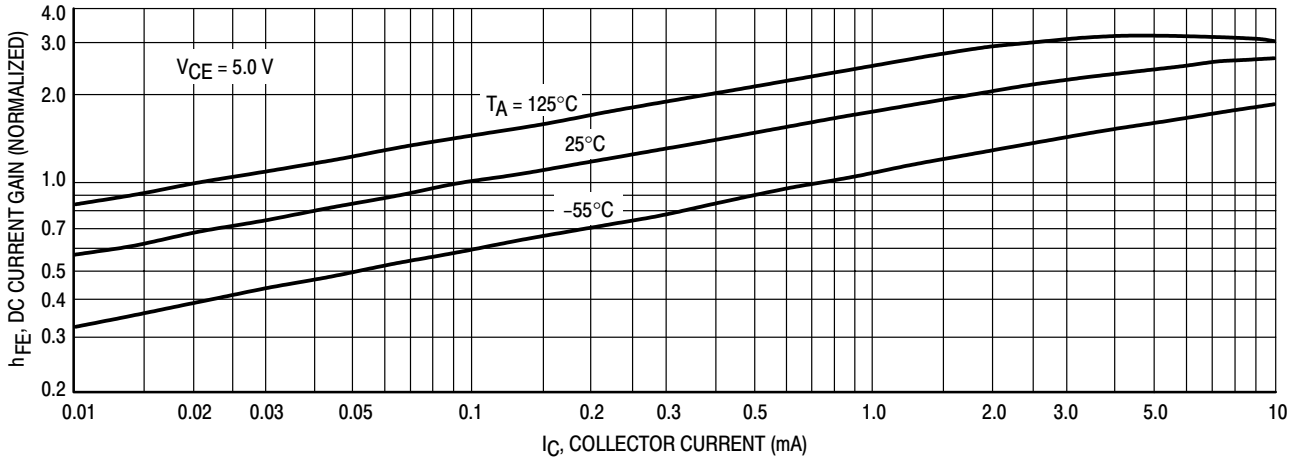


Figure 8. DC Current Gain

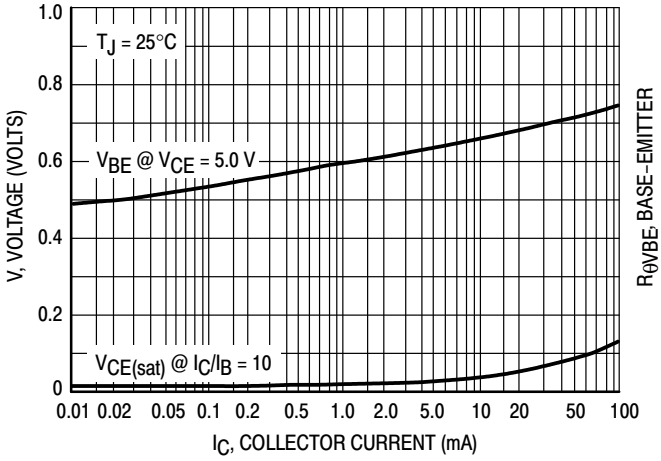


Figure 11. “On” Voltages

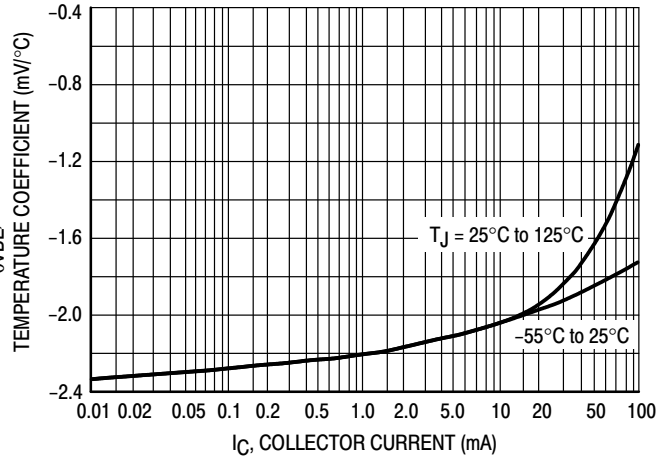


Figure 9. Temperature Coefficients

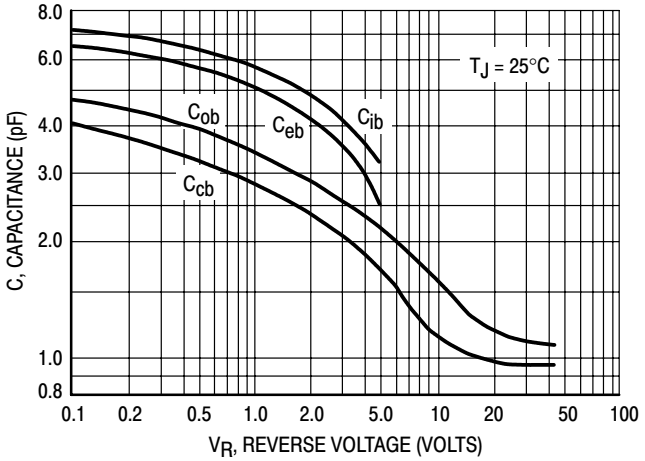


Figure 12. Capacitance

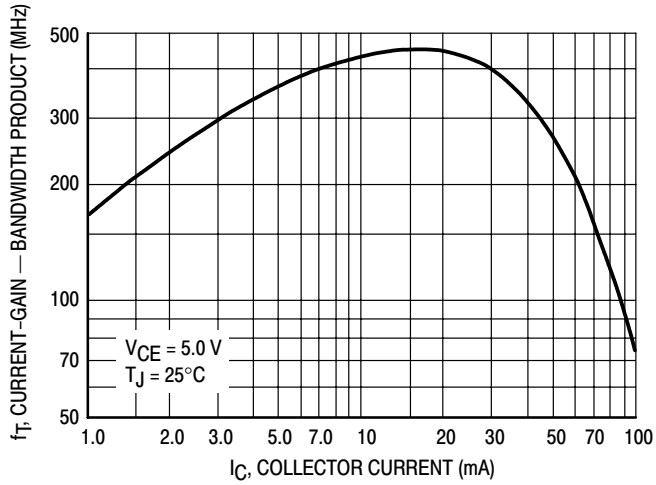
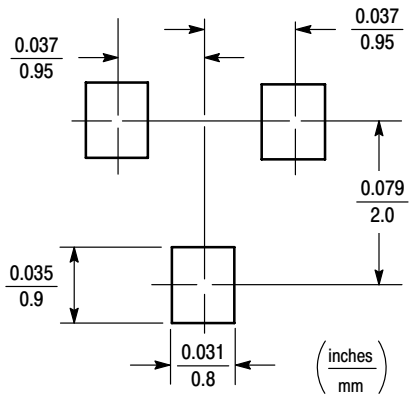


Figure 10. Current–Gain — Bandwidth Product

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

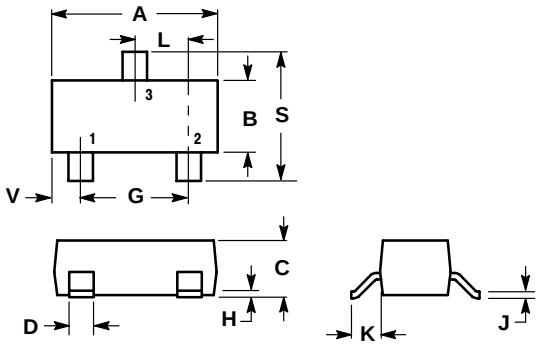
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AF



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

Notes

Thermal Clad is a trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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