54ACT11253, 74ACT11253
DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

SCAS040A – D3110, MARCH 1988 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **3-State Version of ′ACT11153**
- **Permits Multiplexing From N Lines to One Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-µm Process**

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

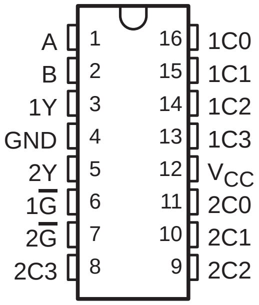
The 54ACT11253 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11253 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

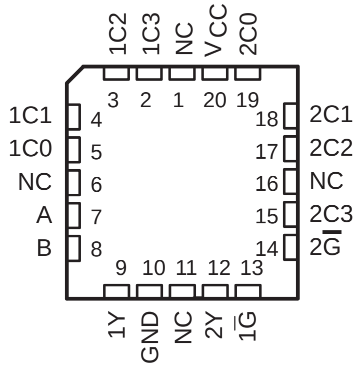
SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL $\overline{G}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

54ACT11253 . . . J PACKAGE
74ACT11253 . . . D OR N PACKAGE
(TOP VIEW)

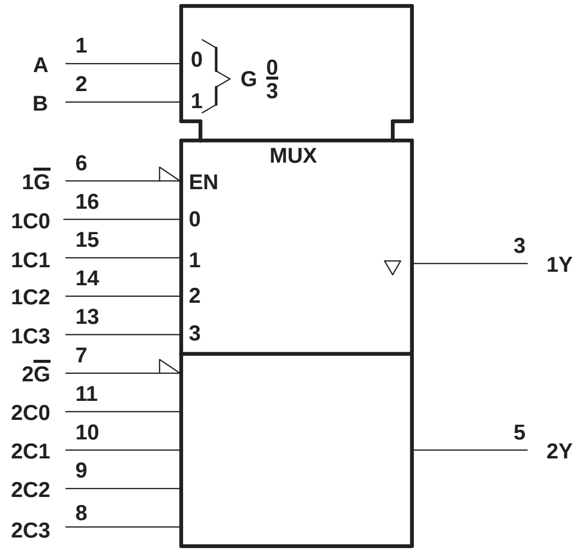


54ACT11253 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

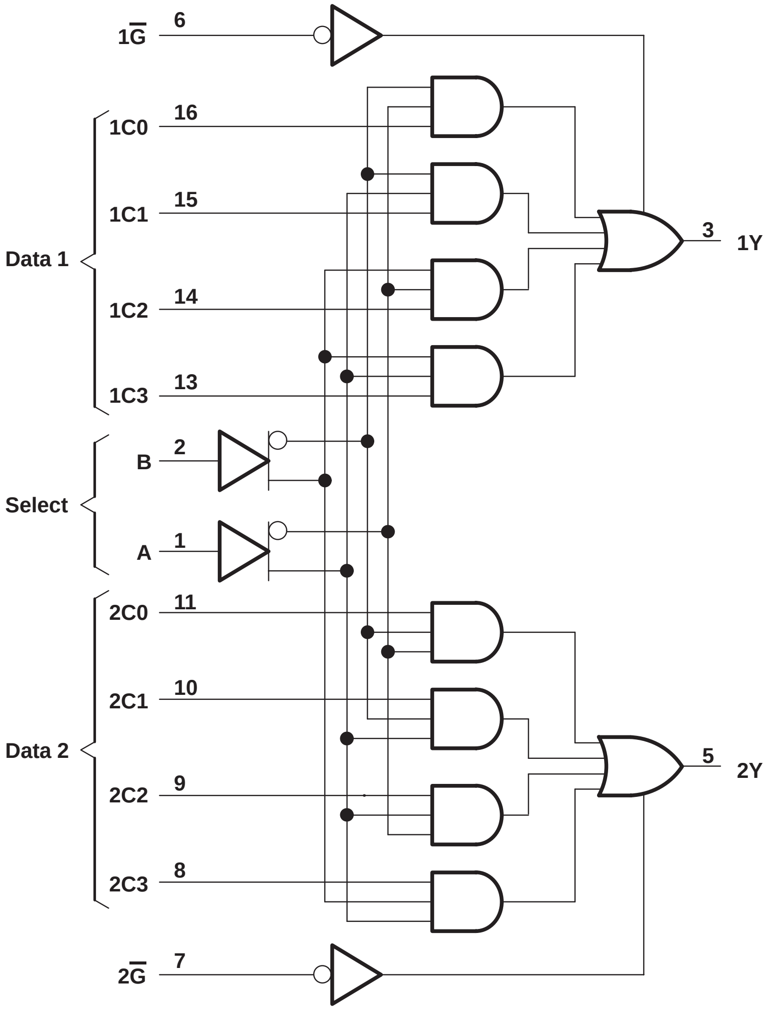
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		54ACT11253		74ACT11253		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT11253		74ACT11253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24$ mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50$ mA†	5.5 V				3.85				
	$I_{OH} = -75$ mA†	5.5 V						3.85		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50$ mA†	5.5 V					1.65			
	$I_{OL} = 75$ mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		8						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

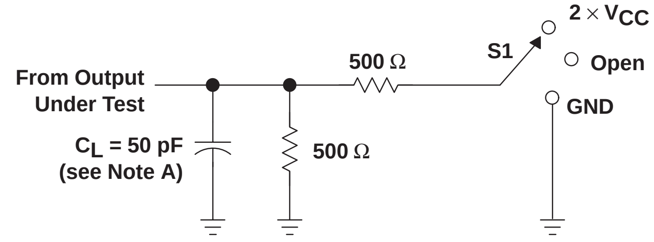
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11253		74ACT11253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1.5	6.8	9.8	1.5	11.8	1.5	11	ns
t_{PHL}			1.5	9.1	12.6	1.5	15.5	1.5	14.3	
t_{PLH}	Data (Any C)	Y	1.5	5.7	7.4	1.5	8.9	1.5	8.3	ns
t_{PHL}			1.5	7.2	10.5	1.5	12.5	1.5	11.7	
t_{PZH}	$\overline{G}$	Y	1.5	5	7.6	1.5	9	1.5	8.5	ns
t_{PZL}			1.5	4.8	7.3	1.5	8.6	1.5	8.1	
t_{PHZ}	$\overline{G}$	Y	1.5	6.4	8.6	1.5	9.5	1.5	9.2	ns
t_{PLZ}			1.5	5.9	7.4	1.5	8.1	1.5	7.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

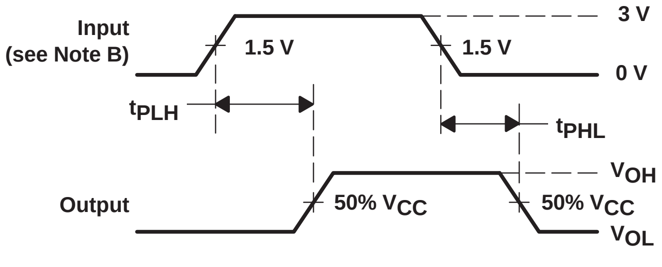
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		18	

PARAMETER MEASUREMENT INFORMATION

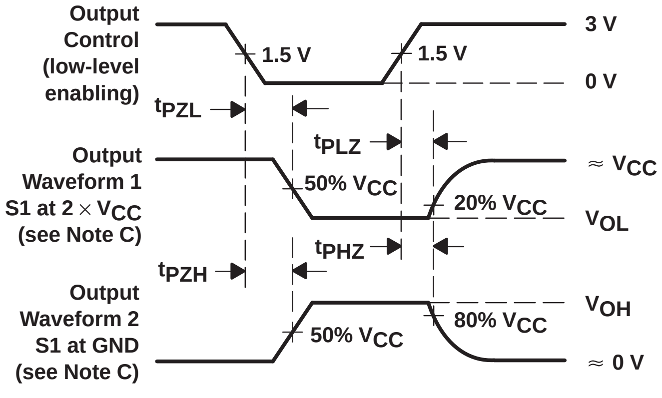


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.