MC14442

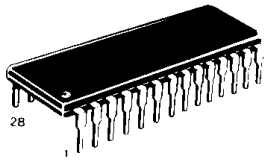
CMOS LSI
(LOW-POWER SILICON GATE COMPLEMENTARY MOS)

2

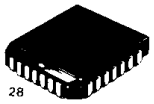
8-BIT A/D CONVERTER WITH PARALLEL INTERFACE

The MC14442 ADC is a 28-pin bus compatible 8-bit A/D converter with additional digital input capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles and allows up to 11 analog inputs. In addition, the part can accept up to 6 digital inputs. These inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control, and bus interface is included.

- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at $f_E = 1.0$ MHz
- Ratiometric Conversion
- Completely Programmable
- 5 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V ± 10%
- Monotonic Over Complete Input Range



P SUFFIX
PLASTIC DIP
CASE 710

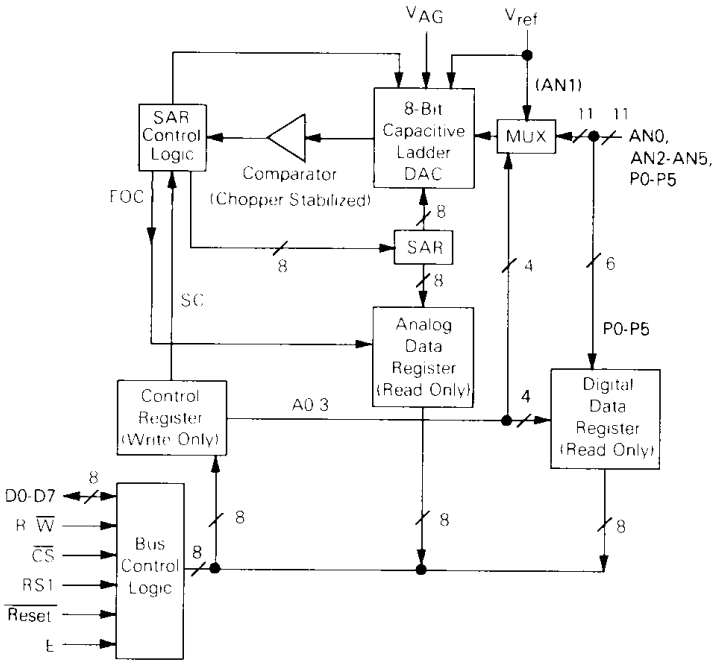


FN SUFFIX
PLCC
CASE 776

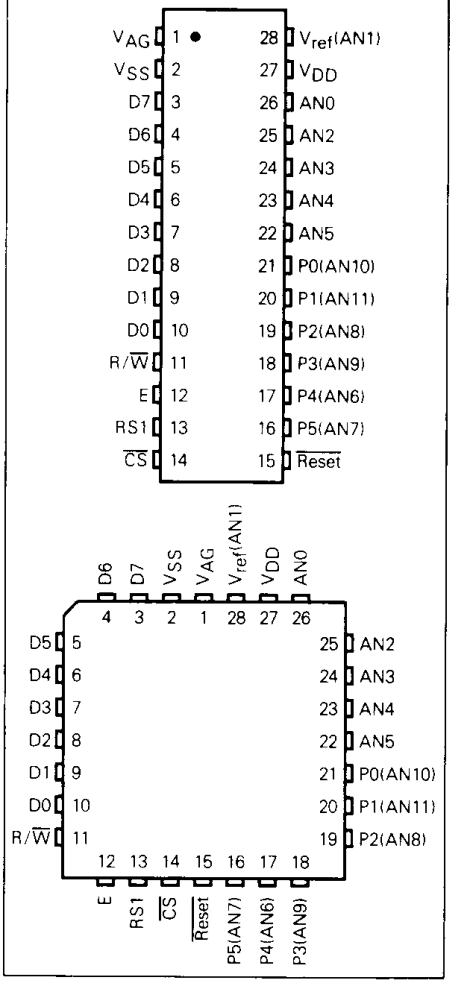
ORDERING INFORMATION

MC14442P	Plastic DIP
MC14442FN	PLCC

BLOCK DIAGRAM



PIN ASSIGNMENTS



2

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.5	V
V_{in}	DC Input Voltage (Referenced to V_{SS})	−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage (Referenced to V_{SS})	−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±20	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, T_A = −40°C to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS1, $\overline{CS}$)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{in} = 0 to 5.5 V	–	±1	μA
Data Bus (D0-D7)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Three-State (Off State) Input Leakage Current	I_{TSI}	V_{DD} = 5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±10	μA
Output High Voltage	V_{OH}	I_{OH} = −1.6 mA I_{OH} = −20 μA	2.4 V_{DD}−0.1	– –	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA I_{OL} = 20 μA	– –	0.4 0.1	V
Peripheral Inputs (P0-P5)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{DD} = 5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±1.0	μA
Current Requirements					
Supply Current	I_{DD}	V_{DD} = 5.5 V	–	10	mA
Input Current, V_{ref}	I_{ref}	V_{ref} = 4.5 to 5.5 V	–	800	μA

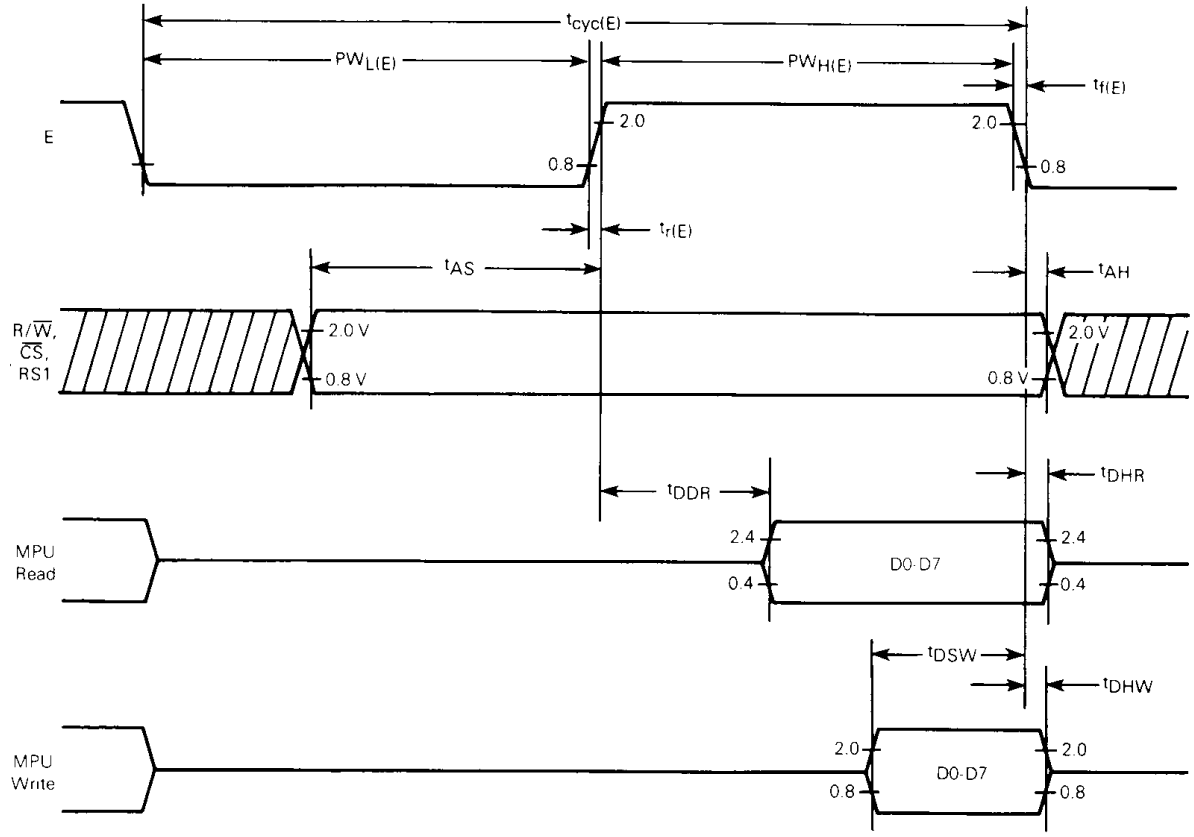
ANALOG CHARACTERISTICS (T_A = −40°C to 85°C)

Characteristic	Description	Min	Max	Unit
Analog Multiplexer				
Leakage Current	Leakage current between all deselected analog inputs and any selected analog input with all analog input voltages between V_{SS} and V_{DD}	–	±500	nA
A/D Converter (V_{SS} = 0 V, V_{AG} = 0 V, 4.5 V ≤ V_{ref} ≤ V_{DD} ≤ 5.5 V)				
Resolution	Number of bits resolved by the A/D	8	–	Bits
Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	–	± ½	LSB
Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	–	± ½	LSB
Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	–	± ½	LSB
Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	–	± ½	LSB
Quantization Error	Uncertainty due to converter resolution	–	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	–	±1.0	LSB
Conversion Time	Total time to perform a single analog-to-digital conversion	–	32	E cycles
Sample Acquisition Time	Time required to sample the analog input	–	12	E cycles

AC CHARACTERISTICS ($T_A = -40°$ to $85°C$) (See Figure 1)

Characteristic	Signal	Symbol	Min	Max	Unit
Enable Clock Cycle Time ($1/f_E$)	E	$t_{cyc(E)}$	943	–	ns
Enable Clock Pulse Width, High	E	$PW_{H(E)}$	440	–	ns
Enable Clock Pulse Width, Low	E	$PW_{L(E)}$	410	–	ns
Clock Rise Time	E	$t_{r(E)}$	–	25	ns
Clock Fall Time	E	$t_{f(E)}$	–	30	ns
Address Setup Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AS}	145	–	ns
Data Delay (Read)	D0-D7	t_{DDR}	–	335	ns
Data Setup (Write)	D0-D7	t_{DSW}	185	–	ns
Address Hold Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AH}	10	–	ns
Input Data Hold Time	D0-D7	t_{DHW}	10	–	ns
Output Data Hold Time	D0-D7	t_{DHR}	10	–	ns
Input Capacitance	P0-P5, AN0-AN10	C_{in}	–	55	pF
	R/$\overline{W}$, E, RS1, $\overline{CS}$, $\overline{RESET}$		–	15	
Three-State Output Capacitance	D0-D7	C_{out}	–	15	pF

FIGURE 1 – BUS TIMING



2

PIN FUNCTIONS

Pin No.	Pin Name	Function	Type
1	V_{AG}	A/D Converter Analog Ground	Supply
2	V_{SS}	Digital Ground	Supply
3	D7	Data Bus Bit 7 (MSB)	Input/Output
4	D6	Data Bus Bit 6	Input/Output
5	D5	Data Bus Bit 5	Input/Output
6	D4	Data Bus Bit 4	Input/Output
7	D3	Data Bus Bit 3	Input/Output
8	D2	Data Bus Bit 2	Input/Output
9	D1	Data Bus Bit 1	Input/Output
10	D0	Data Bus Bit 0 (LSB)	Input/Output
11	R/$\overline{W}$	Read/Write	Input
12	E	Enable Clock (ϕ2)	Input
13	RS1	Register Select	Input
14	$\overline{CS}$	Chip Select	Input
15	$\overline{Reset}$	Reset	Input
16	P5(AN7)	Digital Port or Analog Channel 7	Input
17	P4(AN6)	Digital Port or Analog Channel 6	Input
18	P3(AN9)	Digital Port or Analog Channel 9	Input
19	P2(AN8)	Digital Port or Analog Channel 8	Input
20	P1(AN11)	Digital Port or Analog Channel 11	Input
21	P0(AN10)	Digital Port or Analog Channel 10	Input
22	AN5	Analog Channel 5	Input
23	AN4	Analog Channel 4	Input
24	AN3	Analog Channel 3	Input
25	AN2	Analog Channel 2	Input
26	AN0	Analog Channel 0	Input
27	V_{DD}	Supply Voltage	Supply
28	V_{ref} (AN1)	A/D Converter Positive Reference Voltage (Analog Channel 1)	Input

MC14442 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) – The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) – The enable clock provides two functions for the MC14442. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/$\overline{W}$) – The R/$\overline{W}$ signal is provided to the MC14442 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/$\overline{W}$ to transfer data out of either of the ADC data registers.

Reset ($\overline{Reset}$) – The reset line supplies the means of externally forcing the MC14442 into a known state. When a low is applied to the $\overline{Reset}$ pin, the start conversion bit of the control register is cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the $\overline{Reset}$ pin must be low for at least one complete enable clock cycle.

Chip Select ($\overline{CS}$) – Chip select is an active low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless $\overline{CS}$ is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14442.

MC14442 ANALOG INPUTS AND DIGITAL INPUTS

(Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN5) – These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 12-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN6-AN11) – These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

Shared Digital Inputs (P0-P5) – P0-P5 comprise a 6-bit digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is not programmed, but instead is simply assigned by the system designer on a pin-by-pin basis.

CAUTION: Digital values read from the P0-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

MC14442 SUPPLY VOLTAGE PINS

Positive Supply Voltage (V_{DD}) – V_{DD} is used internally to supply power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14442 were designed with high V_{DD} supply rejection; however, it is recommended that a filtering capacitance be used externally between V_{DD} and V_{SS} to filter noise caused by transient current spikes.

Ground Supply Voltage (V_{SS}) – V_{SS} should be tied to system digital ground or the negative terminal of the V_{DD} power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high V_{SS} rejection.

Positive A/D Reference Voltage (V_{ref}) – This is the voltage used internally to provide reference to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{ref} - V_{AG}$ (full scale). Hence V_{ref} should be a very noise-free supply. Ideally V_{ref} should be single-point connected to the voltage supply driving the system's transducers. V_{ref} may be connected to V_{DD}, but degradation of absolute A/D accuracy may result due to switching noise on V_{DD}.

V_{ref} can be accessed via Analog Channel 1 (AN1).

A/D Ground Reference Voltage (V_{AG}) – This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy may be degraded if V_{AG} is wired to V_{SS} at the ADC package unless V_{SS} has been sufficiently filtered to remove switching noise. Ideally V_{AG} should be single-point grounded to the system analog ground supply.

MC14442 INTERNAL REGISTERS

The MC14442 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

CAUTION: RS1 should **not** be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

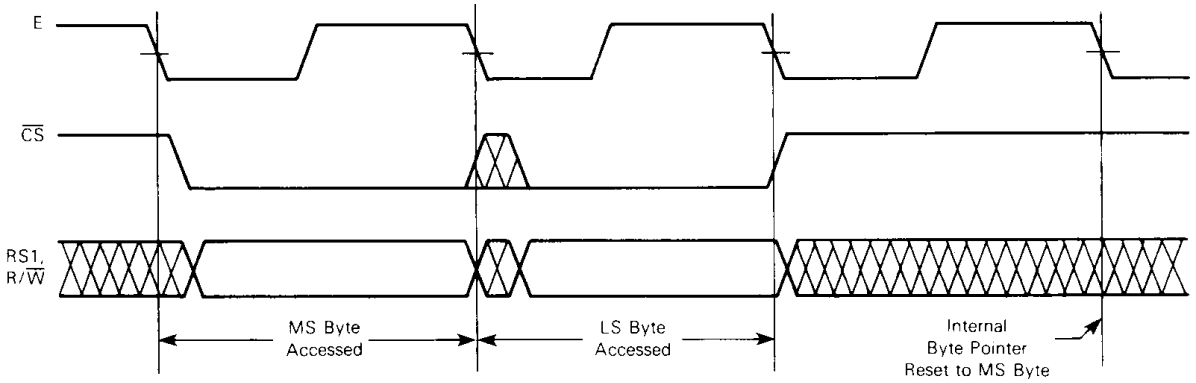
INTERNAL REGISTER ADDRESSING

Addressing Signals				ADC Response
$\overline{Reset}$	$\overline{CS}$	R/$\overline{W}$	RS1	
0	X	X	X	Reset
1	0	0	0	No Response
1	0	0	1	MPU Write to Control Register
1	0	1	0	MPU Read from Analog Data Register
1	0	1	1	MPU Read from Digital Data Register
1	1	X	X	Chip Deselected (No Response)

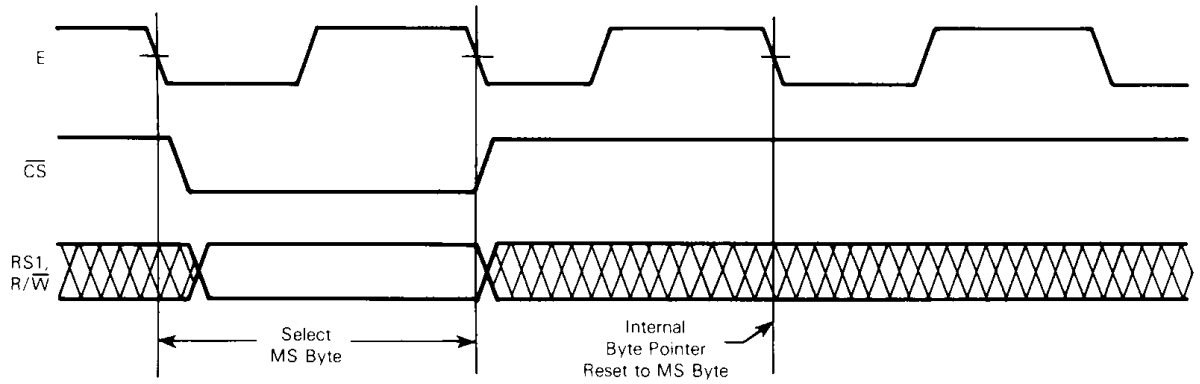
FIGURE 2 — ADC ACCESS TIMING

2

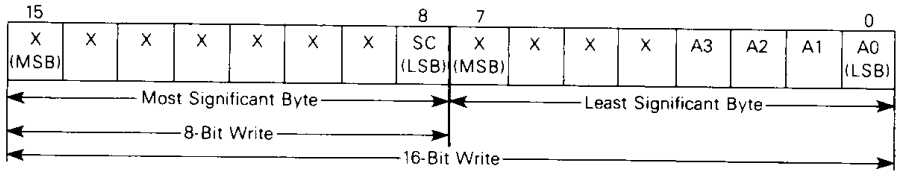
a — Typical 16-Bit ADC Access



b — Typical 8-Bit ADC Access



MC14442 CONTROL REGISTER
(Write Only)



Analog Multiplexer Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

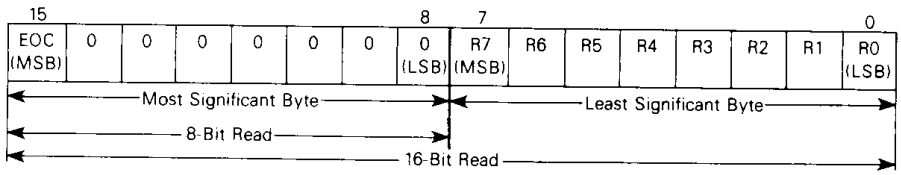
Hexadecimal Address (A3 = MSB)	Select
0	AN0
1	V_{ref}(AN1)
2-5	A2-AN5
6 or E	AN6
7 or F	AN7
8 or C	AN8
9 or D	AN9
A	AN10
B	AN11

Start A/D Conversion (SC) – When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel will begin immediately after the completion of the control register write.

Unused Bits (X) – Bits 4-7 and 9-15 of the ADC Control Register are not used internally.

NOTE: A 16-bit control register write is required to change the analog multiplexer address. However, 8-bit writes to the MC14442 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

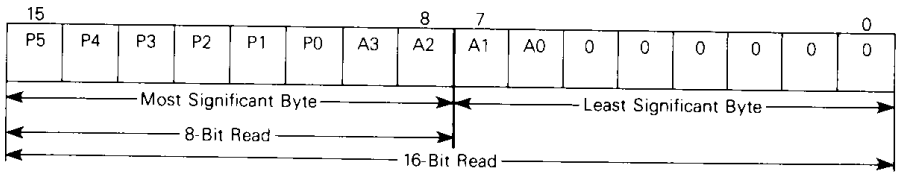
MC14442 ANALOG DATA REGISTER
(Read Only)



A/D Result (R0-R7) – The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of $FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) – The A/D status bit is set whenever a conversion is successfully completed by the ADC. The status bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14442 DIGITAL DATA REGISTER
(Read Only)



Logical Zero (0) – These bits are always read as logical zero.

Analog Multiplexer Address (A0-A3) – The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) – The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

ANALOG SUBSYSTEM
(See Block Diagram)

2

General Description

The analog subsystem of the MC14442 is composed of a 12-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of twelve channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as V_{DD} and V_{SS} power supply rejection.

Device Operation

An A/D conversion is initiated by writing a logical 1 into the SC bit of the ADC control register. The MC14442 allows 2 enable clock cycles for the write into the control register even if only one byte is written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 KΩ or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logic 0) if an A/D conversion is in progress.

FIGURE 3 – A/D TIMING SEQUENCE

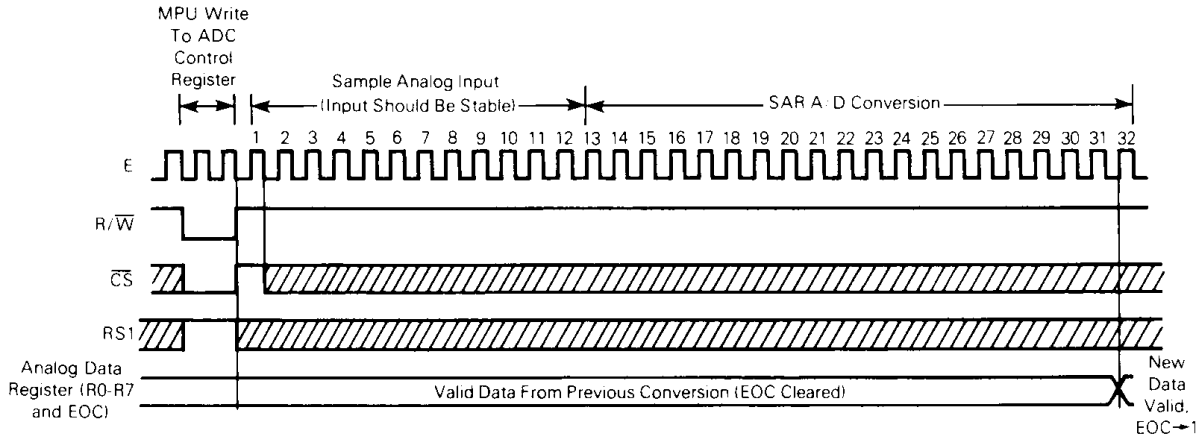
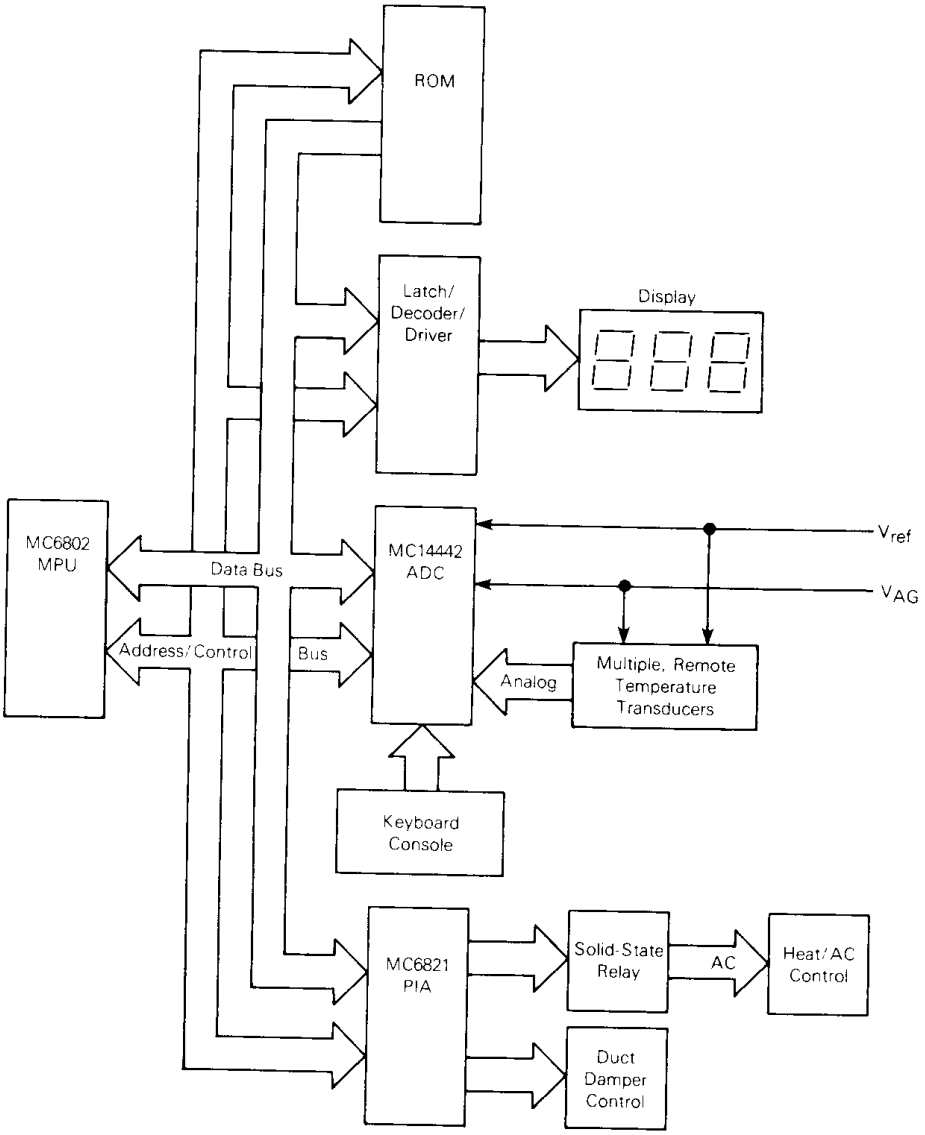


FIGURE 4 – TYPICAL MC14442 APPLICATION IN A CLIMATE CONTROLLER



ADCs/DACs

2

SELECTOR GUIDE

Function	I/O Format	Resolution	Number of Analog Channels	On-Chip Oscillator	Other Features	Device Number
ADC	Serial	8 Bits	11	—	Successive Approximation	**MC145040**
		10 Bits	11			**MC145050**
		8 Bits	11	√	Successive Approximation	**MC145041**
		10 Bits	11			**MC145051**
		10 Bits	5			**MC145053**
	Parallel	3 1/2 Digit BCD	1	√	Dual Slope	**MC14433**
		8 Bits	11	—	Successive Approximation	**MC14442**
ADC Linear Subsystem	Parallel	8 to 10 Bits	6	—	Single Slope w/ Auto Zeroing	**MC14443**
		8 to 10 Bits	6	—	Single Slope w/ Auto Zeroing	**MC14447**
DAC	Serial	6 Bits	6	—	Emitter-Follower Outputs	**MC144110**
		6 Bits	4	—	Emitter-Follower Outputs	**MC144111**