To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M5M5Y416CWG -55HI, -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

Those are summarized in the part name table below.

DESCRIPTION

The M5M5Y416C is a family of low voltage 4-Mbit static RAMs organized as 262144-words by 16-bit, fabricated by Mitsubishi's high-performance 0.18µm CMOS technology.

The M5M5Y416C is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

M5M5Y416CWG is packaged in a CSP (chip scale package), with the outline of 7.0mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

FEATURES

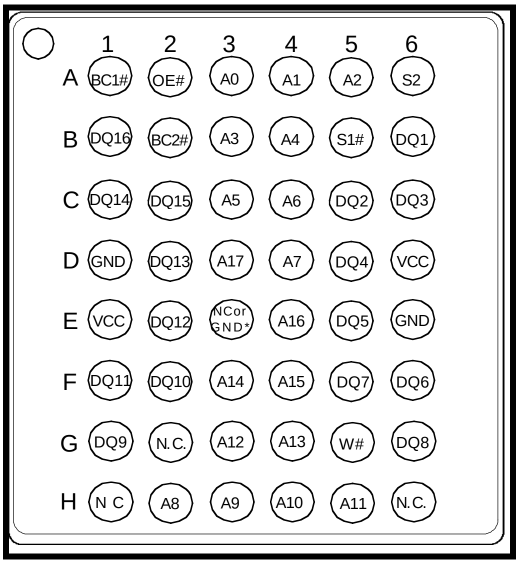
- Single 1.65~2.3V power supply
- Small stand-by current: 0.1µA (2.3V, typ.)
- No clocks, No refresh
- Data retention supply voltage =1.3V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S1#, S2, BC1# and BC2#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Process technology: 0.18µm CMOS
- Package: 48ball 7.0mm x 8.5mm CSP

Version, Operating temperature	Part name	Power Supply	Access time max.	Stand-by current (µA)						Active current Icc1 (2.3V, max)
				* Typical		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
I-version -40 ~ +85°C	M5M5Y416CWG -55HI	1.65 ~ 2.3V	55ns	0.1	0.2	1	2	8	15	30mA (10MHz) 3mA (1MHz)
	M5M5Y416CWG -70HI	1.65 ~ 2.3V	70ns							

* Typical parameter indicates the value for the center of distribution at 2.3V, and not 100% tested.

PIN CONFIGURATION

(TOP VIEW)



	1	2	3	4	5	6
A	BC1#	OE#	A0	A1	A2	S2
B	DQ16	BC2#	A3	A4	S1#	DQ1
C	DQ14	DQ15	A5	A6	DQ2	DQ3
D	GND	DQ13	A17	A7	DQ4	VCC
E	VCC	DQ12	NCor GND*	A16	DQ5	GND
F	DQ11	DQ10	A14	A15	DQ7	DQ6
G	DQ9	N.C.	A12	A13	W#	DQ8
H	NC	A8	A9	A10	A11	N.C.

Outline: 48FJA

NC: No Connection

*Don't connect E3 ball to voltage level more than 0V

Pin	Function
A0 ~ A17	Address input
DQ1 ~ DQ16	Data input / output
S1#	Chip select input 1
S2	Chip select input 2
W#	Write control input
OE	Output enable input
BC1#	Lower Byte (DQ1 ~ 8)
BC2#	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply

M5M5Y416CWG -55HI, -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

FUNCTION

The M5M5Y416CWG is organized as 262144-words by 16-bit. These devices operate on a single +1.65~2.3V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs BC1# , BC2# , S1# , S2 , W# and OE#. Each mode is summarized in the function table.

A write operation is executed whenever the low level W# overlaps with the low level BC1# and/or BC2# and the low level S1# and the high level S2. The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting W at a high level and OE# at a low level while BC1# and/or BC2# and S1# and S2 are in an active state(S1=L,S2=H).

When setting BC1# at the high level and other pins are in an active stage , upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting BC2# at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

When setting BC1# and BC2# at a high level or S1# at a high level or S2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by BC1#, BC2# and S1#, S2.

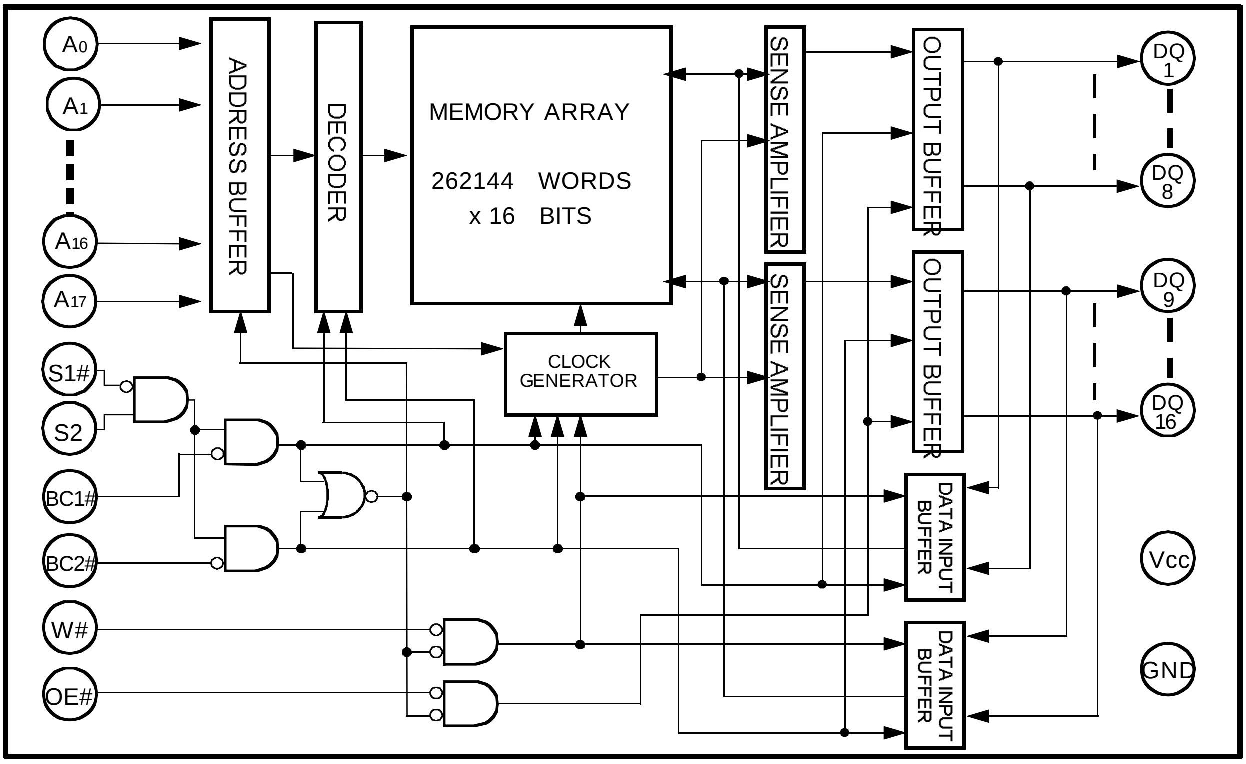
The power supply current is reduced as low as 0.1µA(25°C, Vcc=1.65V, typical), and the memory data can be held at +1.3V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

S1#	S2	BC1#	BC2#	W#	OE#	Mode	DQ1~8	DQ9~16	Icc
H	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
L	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	———	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	———	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	———	High-Z	High-Z	Active

note1: "H" and "L" in this table mean V_{IH} and V_{IL}, respectively.
note2: "X" in this table should be "H" or "L".

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.3* ~ +2.7	V
V_I	Input voltage	With respect to GND	-0.3* ~ Vcc + 0.3 (max. 2.7V)	
V_O	Output voltage	With respect to GND	0 ~ Vcc	
P_d	Power dissipation	Ta=25°C	700	mW
T_a	Operating temperature	I-version	- 40 ~ +85	°C
T_{stg}	Storage temperature		- 65 ~ +150	°C

* -0.7V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS

(Vcc=1.65~ 2.3V, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Units
				Min	Typ	Max	
V_{IH}	High-level input voltage			0.7xVcc		Vcc+0.2	V
V_{IL}	Low-level input voltage			-0.2 *		0.4	
V_{OH}	High-level output voltage	I_{OH}= -0.1mA		1.3			
V_{OL}	Low-level output voltage	I_{OL}=0.1mA				0.2	
I_I	Input leakage current	V_I =0 ~ Vcc				±1	µA
I_O	Output leakage current	BC1# and BC2#=VIH or S1#=VIH or S2=VIL or OE#=VIH, VI/O=0 ~ Vcc				±1	
Icc1	Active supply current (AC,MOS level)	BC1# and BC2#≦ 0.2V, S1#≦ 0.2V, S2≧ Vcc-0.2V other inputs ≦0.2V or ≧ Vcc-0.2V Output - open (duty 100%)	f= 10MHz	-	18	30	mA
			f= 1MHz	-	1.5	3	
Icc2	Active supply current (AC,TTL level)	BC1# and BC2#=V_{IL} , S1#=V_{IL} ,S2=V_{IH} other pins =V_{IH} or V_{IL} Output - open (duty 100%)	f= 10MHz	-	18	30	
			f= 1MHz	-	1.5	3	
Icc3	Stand by supply current (AC,MOS level)	(1) S1# ≧ Vcc - 0.2V, S2 ≧ Vcc - 0.2V, other inputs = 0 ~ Vcc (2) S2 ≦ 0.2V, other inputs = 0 ~ Vcc (3) BC1# and BC2#≧ Vcc - 0.2V S1#≦0.2V, S2≧Vcc - 0.2V other inputs = 0 ~ Vcc	~ +25°C	-	0.1	1	µA
			~ +40°C	-	0.2	2	
			~ +70°C	-	-	8	
			~ +85°C	-	-	15	
Icc4	Stand by supply current (AC,TTL level)	BC1# and BC2#=V_{IH} or S1#=V_{IH} or S2=V_{IL} Other inputs= 0 ~ Vcc		-	-	0.5	mA

* -0.7V in case of AC (Pulse width ≦ 30ns)

Note 3: Direction for current flowing into IC is indicated as positive (no mark)

Note 4: Typical parameter indicates the value for the center of distribution at 2.3V, and not 100% tested.

CAPACITANCE

(Vcc=1.65 ~ 2.3V, unless otherwise noted)

Symbo	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			10	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			10	

AC ELECTRICAL CHARACTERISTICS (Vcc=1.65 ~ 2.3V, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	1.65~2.3V	
Input pulse	V_{IH}=0.7 x Vcc+0.2V, V_{IL}=0.2V	
Input rise time and fall time	5ns	
Reference level	V_{OH}=V_{OL}=0.9V	Transition is measured ±200mV from steady state voltage.(for ten,tdis)
Output loads	Fig.1,CL=30pF CL=5pF (for ten,tdis)	

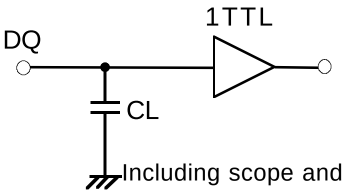


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits				Units
		55HI		70HI		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
$t_{a}(A)$	Address access time		55		70	ns
$t_{a}(S1)$	Chip select 1 access time		55		70	ns
$t_{a}(S2)$	Chip select 2 access time		55		70	ns
$t_{a}(BC1)$	Byte control 1 access time		55		70	ns
$t_{a}(BC2)$	Byte control 2 access time		55		70	ns
$t_{a}(OE)$	Output enable access time		30		35	ns
$t_{dis}(S1)$	Output disable time after S1# high		20		25	ns
$t_{dis}(S2)$	Output disable time after S2 low		20		25	ns
$t_{dis}(BC1)$	Output disable time after BC1# high		20		25	ns
$t_{dis}(BC2)$	Output disable time after BC2# high		20		25	ns
$t_{dis}(OE)$	Output disable time after OE# high		20		25	ns
$t_{en}(S1)$	Output enable time after S1# low	5		10		ns
$t_{en}(S2)$	Output enable time after S2 high	5		10		ns
$t_{en}(BC1)$	Output enable time after BC#1 low	5		5		ns
$t_{en}(BC2)$	Output enable time after BC2# low	5		5		ns
$t_{en}(OE)$	Output enable time after OE# low	5		5		ns
$t_{V}(A)$	Data valid time after address	5		10		ns

(3) WRITE CYCLE

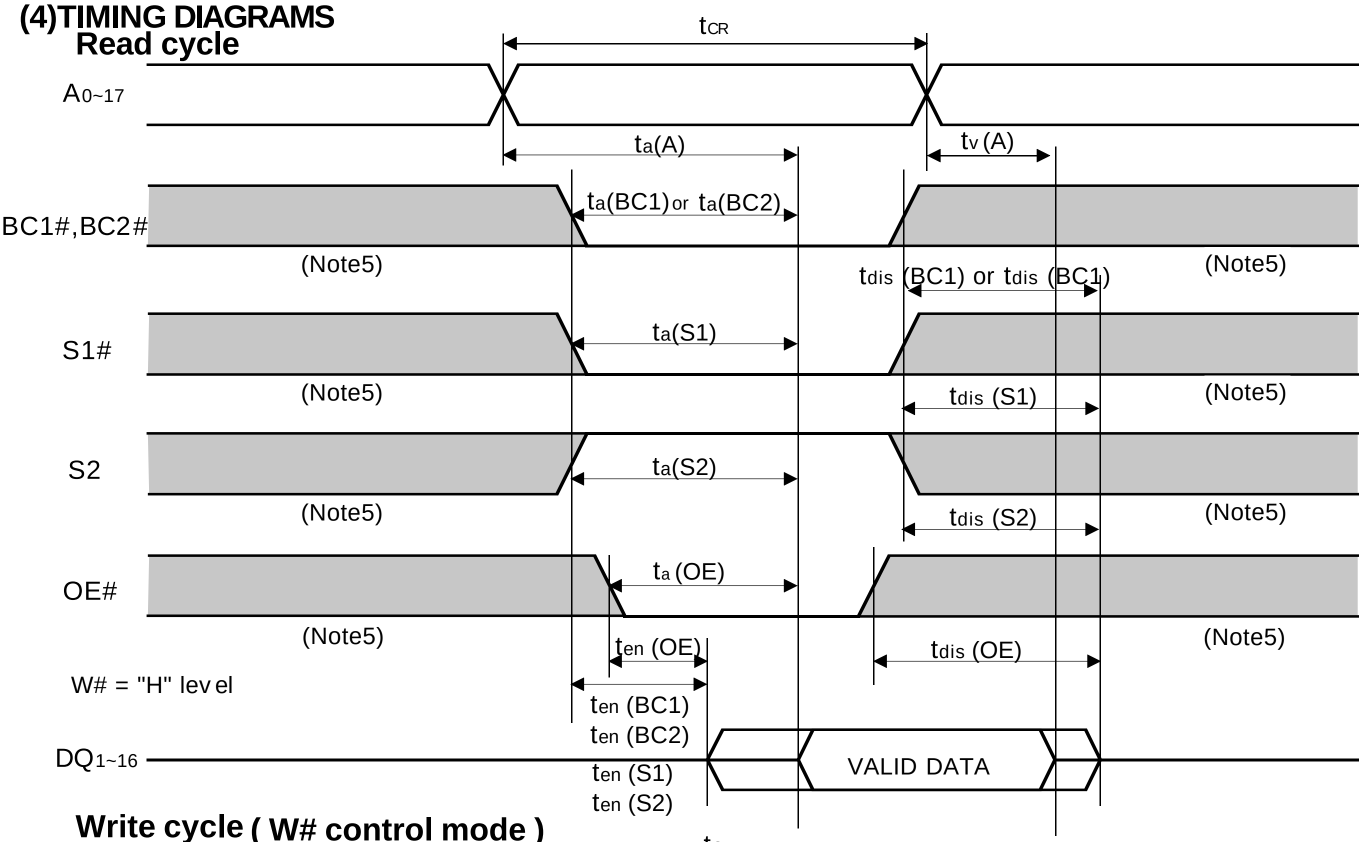
Symbol	Parameter	Limits				Units
		55HI		70HI		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
$t_{w}(W)$	Write pulse width	45		55		ns
$t_{su}(A)$	Address setup time	0		0		ns
$t_{su}(A-WH)$	Address setup time with respect to W#	50		65		ns
$t_{su}(BC1)$	Byte control 1 setup time	50		65		ns
$t_{su}(BC2)$	Byte control 2 setup time	50		65		ns
$t_{su}(S1)$	Chip select 1 setup time	50		65		ns
$t_{su}(S2)$	Chip select 2 setup time	50		65		ns
$t_{su}(D)$	Data setup time	25		30		ns
$t_{h}(D)$	Data hold time	0		0		ns
$t_{rec}(W)$	Write recovery time	0		0		ns
$t_{dis}(W)$	Output disable time from W# low		20		25	ns
$t_{dis}(OE)$	Output disable time from OE# high		20		25	ns
$t_{en}(W)$	Output enable time from W# high	5		5		ns
$t_{en}(OE)$	Output enable time from OE# low	5		5		ns

M5M5Y416CWG -55HI, -70HI

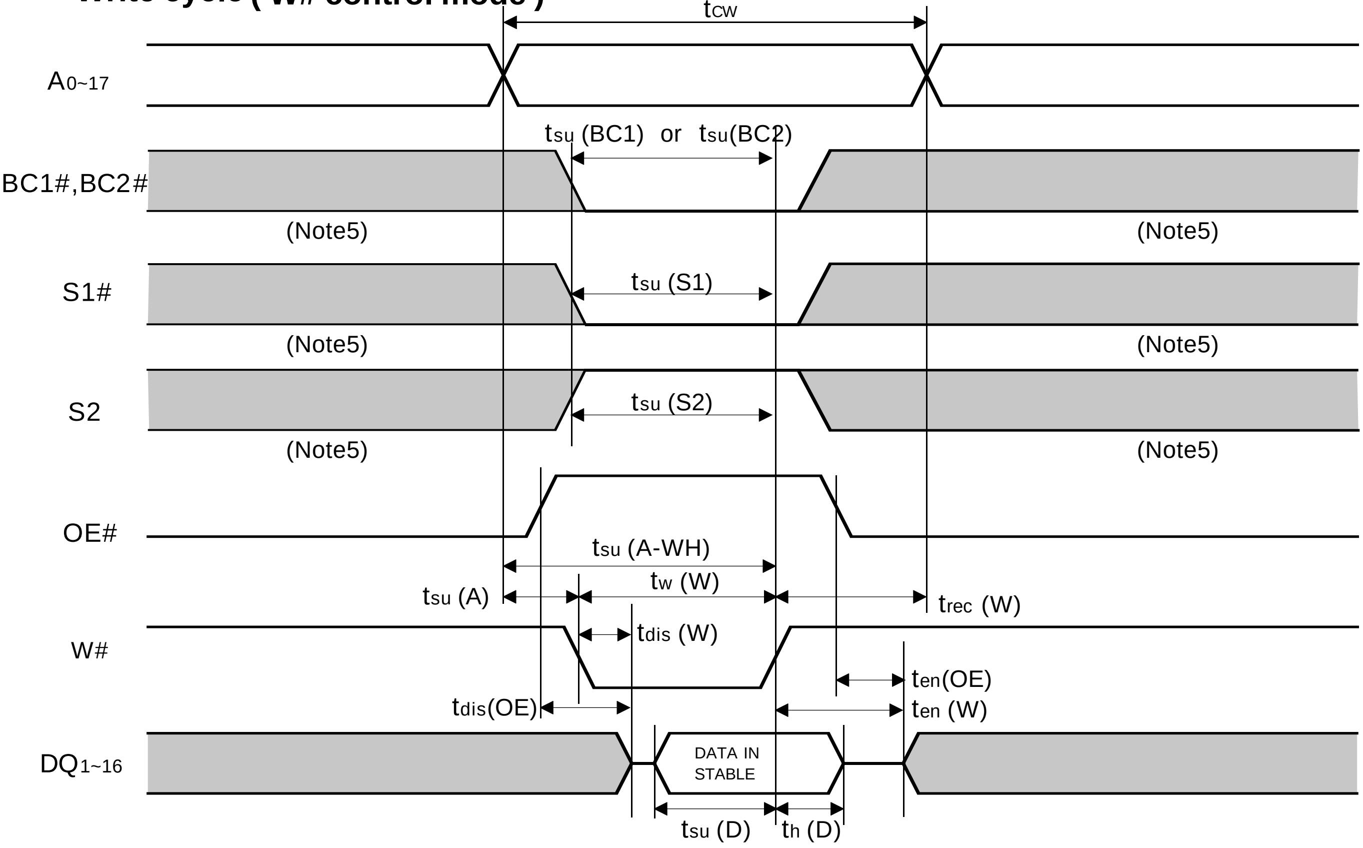
4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

(4)TIMING DIAGRAMS

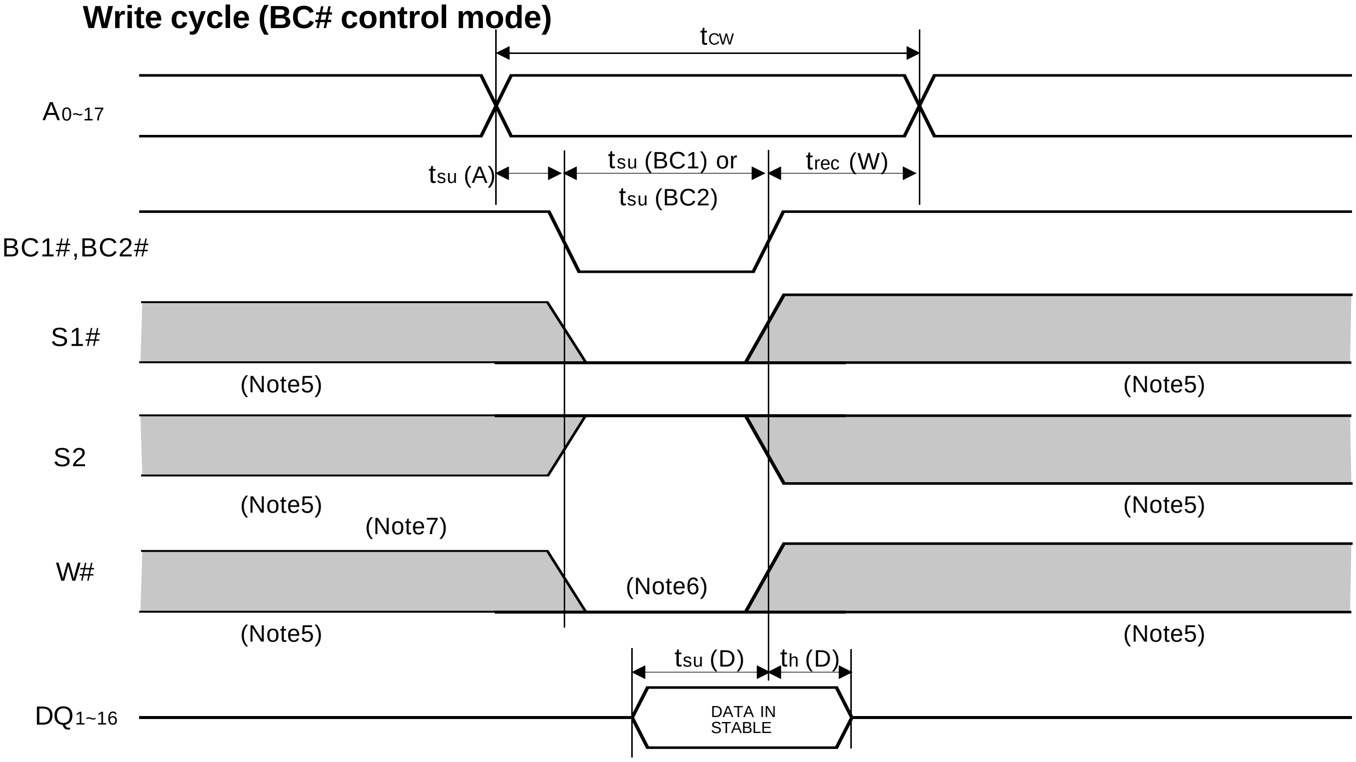
Read cycle



Write cycle (W# control mode)



Write cycle (BC# control mode)



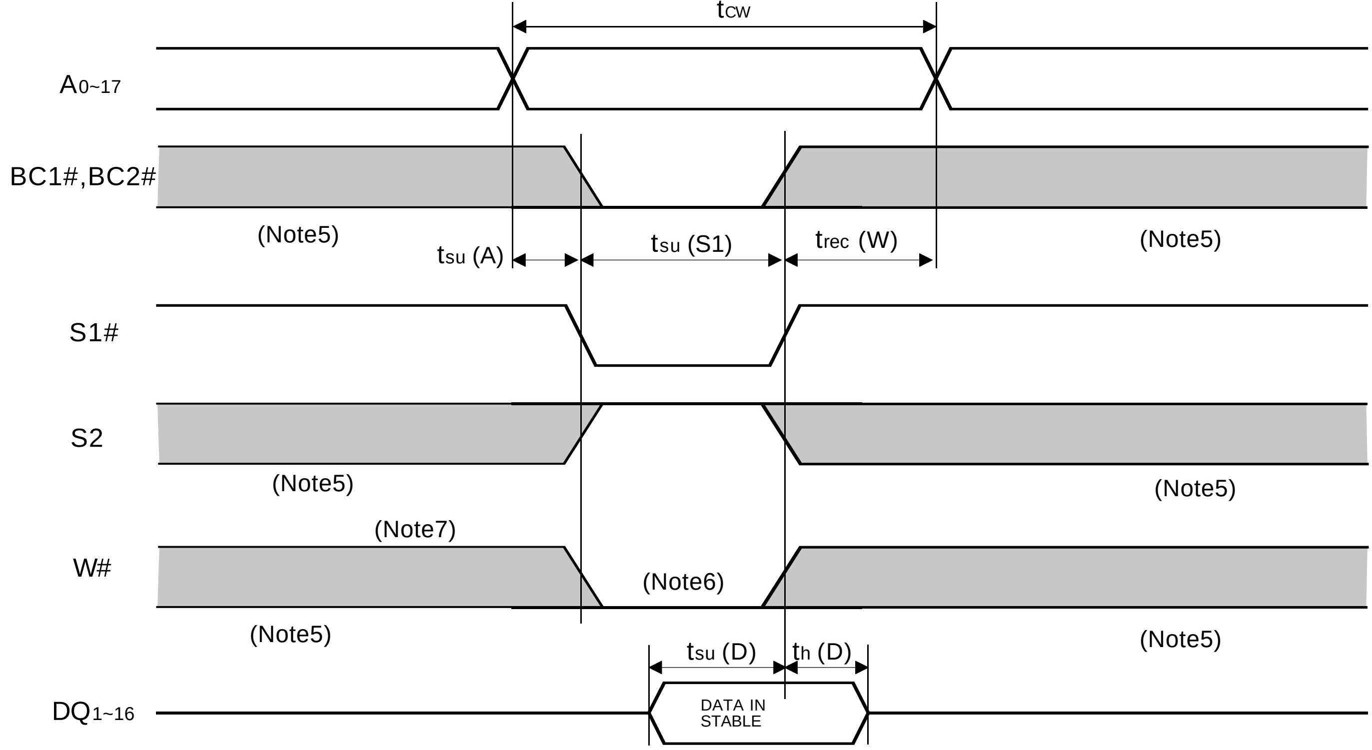
Note 5: Hatching indicates the state is "don't care".

Note 6: A Write occurs during S1# low, S2 high overlaps BC1# and/or BC2# low and W# low.

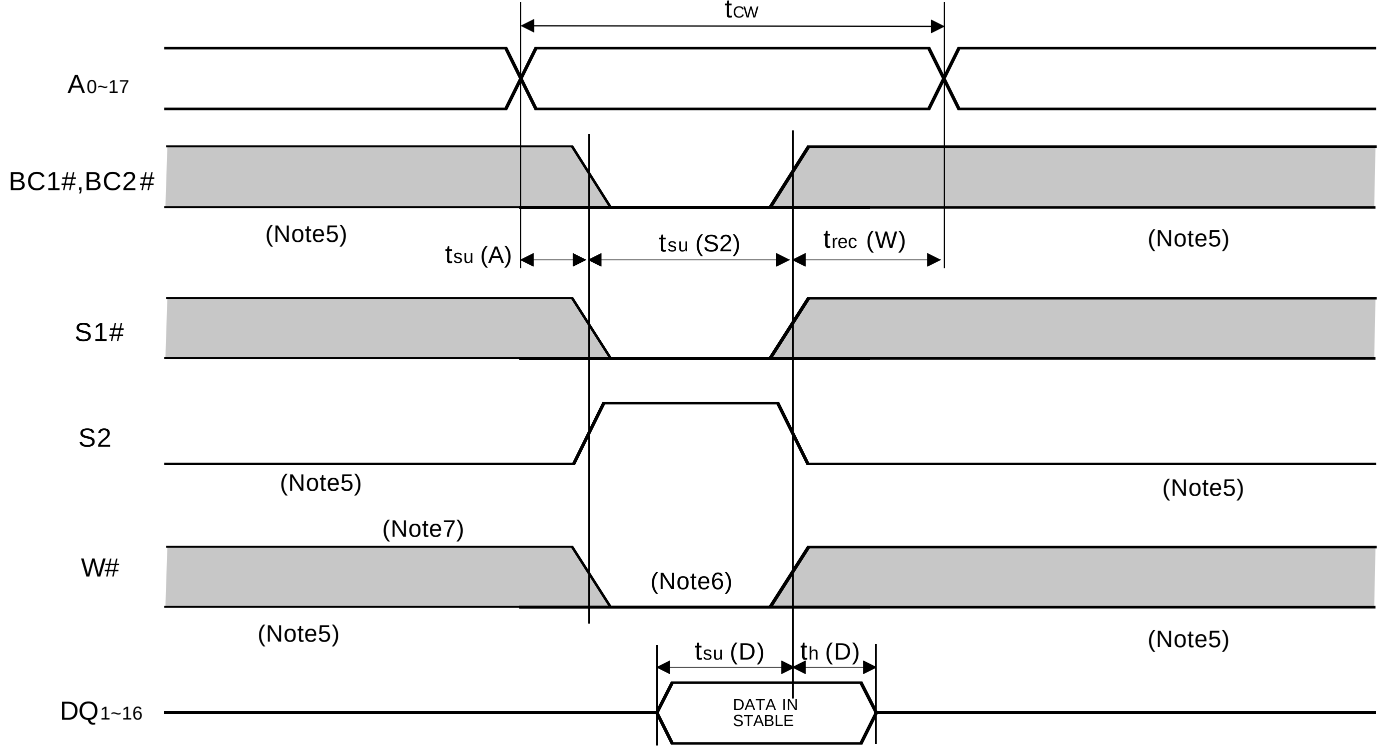
Note 7: When the falling edge of W# is simultaneously or prior to the falling edge of BC1# and/or BC2# or the falling edge of S1# or rising edge of S2, the outputs are maintained in the high impedance state.

Note 8: Don't apply inverted phase signal externally when DQ pin is in output mode.

Write cycle (S1# control mode)



Write cycle (S2 control mode)



POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits			Units
				Min	Typ	Max	
Vcc (PD)	Power down supply voltage			1.3			V
V_I (BC)	Byte control input BC1# & BC2#	1.65V≦ Vcc(PD)		0.7xVcc			V
		1.3V ≦ Vcc(PD) ≦1.65V			Vcc(PD)		
V_I (S1)	Chip select input S1#	1.65V≦ Vcc(PD)		0.7xVcc			V
		1.3V ≦ Vcc(PD) ≦1.65V			Vcc(PD)		
V_I (S2)	Chip select input S2					0.2	V
Icc (PD)	Power down supply current	Vcc=1.65V (1) S1# ≧ Vcc - 0.2V, other inputs = 0 ~ Vcc (2) S2 ≦ 0.2V, other inputs = 0 ~ Vcc (3) BC1# and BC2# ≧ Vcc - 0.2V S1# ≦ 0.2V, S2 ≧ Vcc - 0.2V other inputs = 0 ~ Vcc	~ +25°C	-	0.1	0.7	µA
			~ +40°C	-	0.2	1.5	
			~ +70°C	-	-	5	
			~ +85°C	-	-	10	

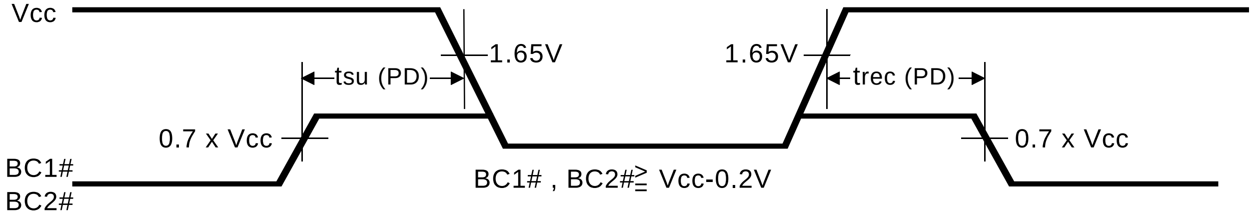
Note 9: Typical parameter of Icc(PD) indicates the value for the center of distribution at 1.65V, and not 100% tested.

(2) TIMING REQUIREMENTS

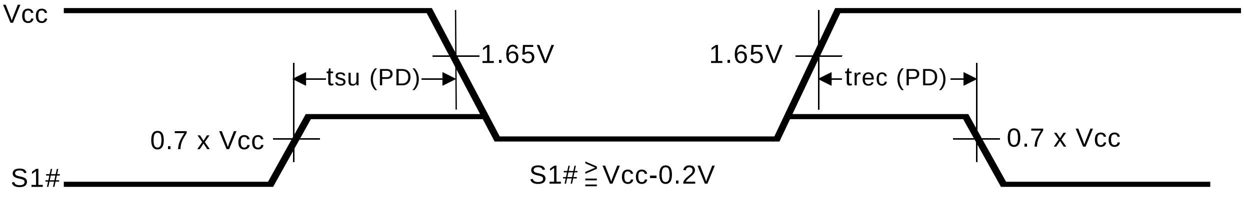
Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t_{su} (PD)	Power down set up time		0			ns
t_{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

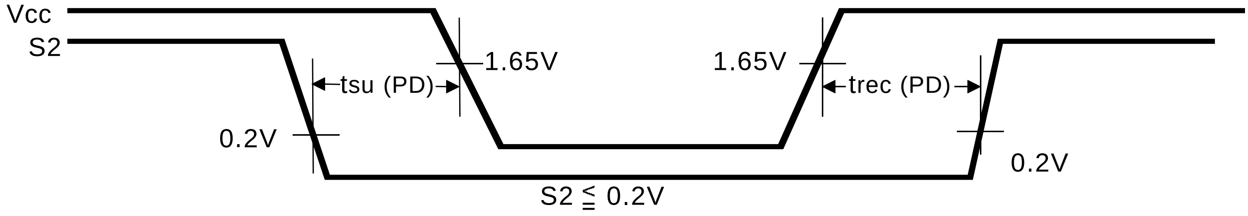
BC# control mode On the BC# control mode, the level of S1# and S2 must be fixed at S1#, S2≧Vcc-0.2V or S2≦0.2V



S1# control mode On the S1# mode, the level of S2 must be fixed at S2 ≧ Vcc-0.2V or S2≦ 0.2V.



S2 control mode



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