

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to
 change.

MITSUBISHI MICROCOMPUTERS
38C8 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 38C8 group is the 8-bit microcomputer based on the 740 family core technology.

The 38C8 group has a LCD drive control circuit (bias control, time sharing control), a 10-bit A-D converter, and a Serial I/O as additional functions.

The various microcomputers in the 38C8 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

FEATURES

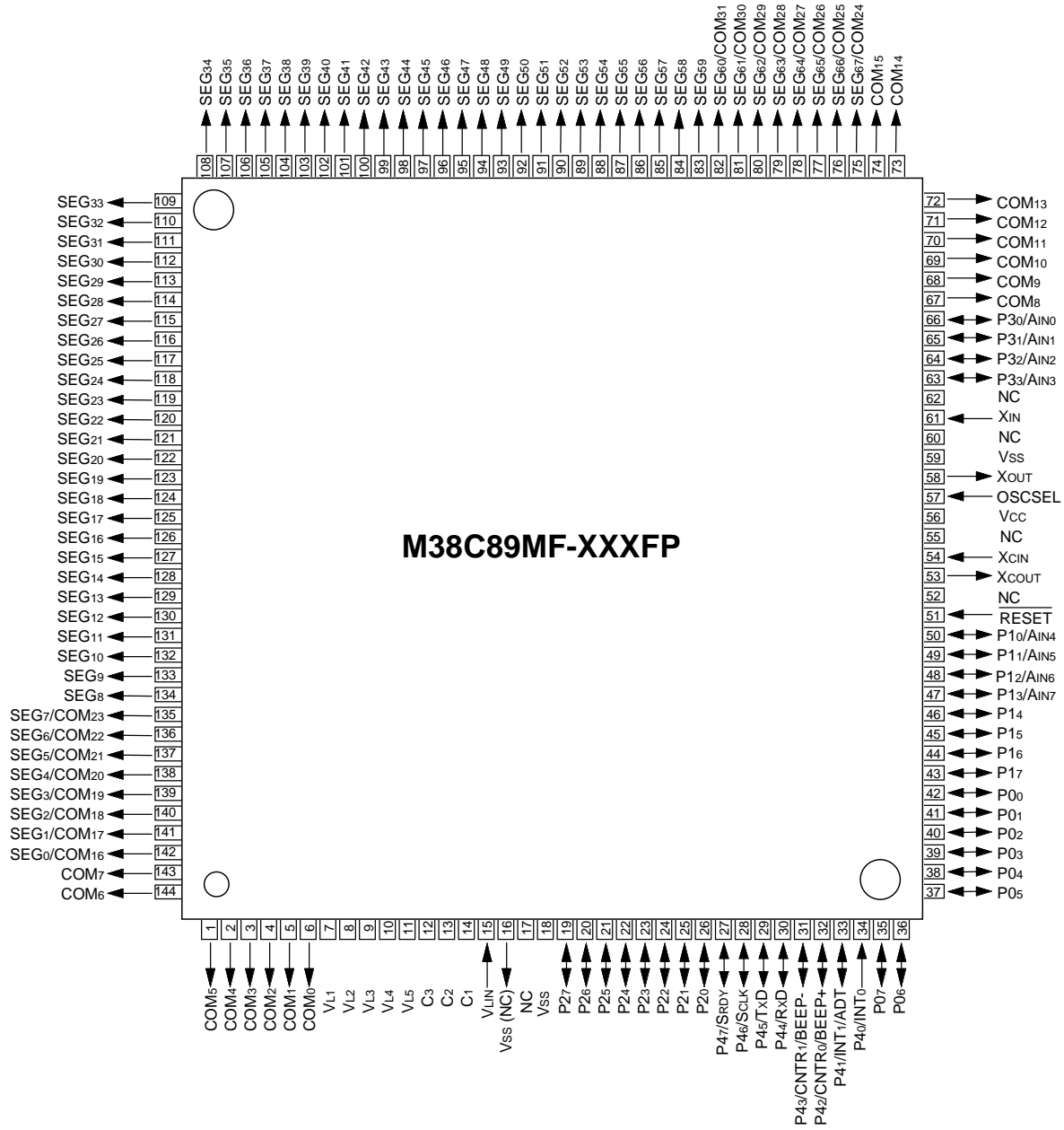
- Basic machine-language instructions 71
- The minimum instruction execution time 0.5 μs
 (at 8 MHz oscillation frequency)
- Memory size
 - ROM 60 K bytes
 - RAM 2048 bytes
- Programmable input/output ports 35
- Software pull-up resistors
 - Ports P0–P3, P41–P47
- Interrupts 15 sources, 15 vectors
 (includes key input interrupt)
- Timers 8-bit X 3, 16-bit X 2
- Serial I/O 8-bit X 1 (UART or Clock-synchronized)
- A-D converter (32 kHz operating available) ... 10-bit X 8 channels

- LCD drive control circuit
 - Bias 1/5, 1/7
 - Duty 1/16, 1/32
 - Common output 16 or 32
 - Segment output 52 or 68
- Main clock generating circuit (RC oscillation selectable)
 - (connect to external ceramic resonator or resistor)
- Sub-clock generating circuit
 - (connect to quartz-crystal oscillator)
- Power source voltage
 - In high-speed mode 4.0 to 5.5 V
 - In middle-speed mode 2.2 to 5.5 V
 - In low-speed mode 2.2 to 5.5 V
- Power dissipation
 - In high-speed mode 30 mW
 (at 8 MHz oscillation frequency, at 5 V power source voltage)
 - In low-speed mode 60 μW
 (at 32 kHz oscillation frequency, at 3 V power source voltage, at WIT state, at voltage multiplier operating, LCD drive waveform generating state)
- Operating temperature range – 20 to 85°C

APPLICATIONS

Dot-matrix-type displays

PIN CONFIGURATION (TOP VIEW)



M38C89MF-XXXXP

Package type : 144P6Q-A

Fig. 1 M38C89MF-XXXXP pin configuration

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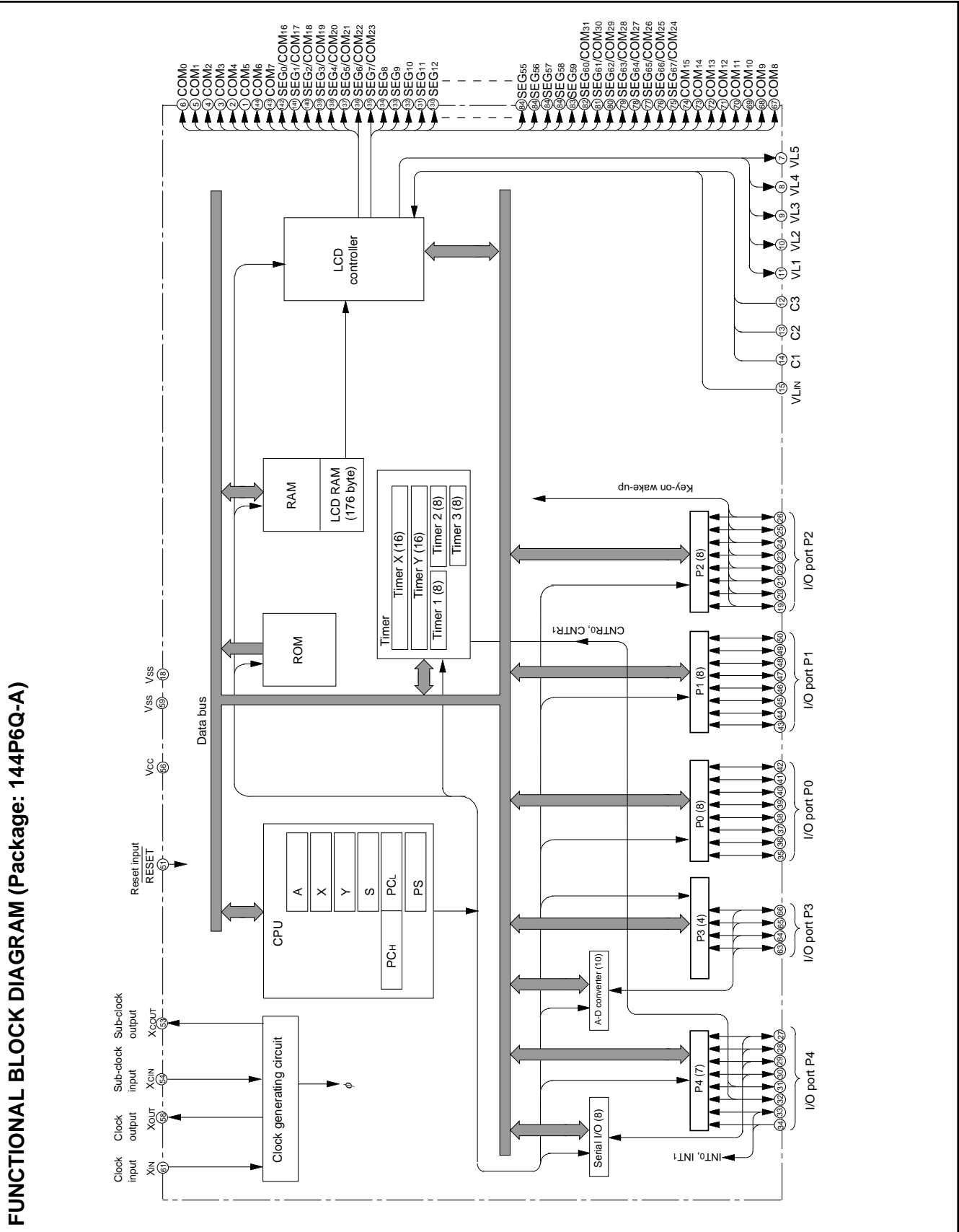


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	
			Function except a port function
Vcc, Vss	Power source	• Apply voltage of 4.0–5.5 V to Vcc, and 0 V to Vss. (at high-speed mode)	
RESET	Reset input	• Reset input pin for active "L."	
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between XIN pin and XOUT pin.	
XOUT	Clock output	• Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
OSCSEL	RC oscillation select	• This pin determines the oscillation between XIN and XOUT. The oscillation method can be selected from either by an oscillator or by a resistor.	
XCIN	Sub-clock input	• Input and output pins for sub-clock generating circuit. (Connect a quartz-crystal oscillator between the XCIN and XCOU pins to set the oscillation frequency. The clock generated the externals cannot be input directly.)	
XCOU	Sub-clock output		
VLIN	Power source input for LCD	• Reference voltage input pin for LCD. • The input voltage to this pin is boosted threefold by voltage multiplier.	
VL1 – VL5	LCD power source	• LCD drive power source pins.	
COM0 – COM32	Common output	• LCD common output pins.	
SEG0/COM16–SEG7/COM23, SEG60/COM31–SEG67/COM24	Segment output/ Common output	• LCD segment/common output pins.	
SEG8–SEG59	Segment output	• LCD segment output pins.	
P00–P07	I/O port P0	• 8-bit I/O port.	
P14–P17	I/O port P1	• CMOS compatible input level.	
P10/AIN4–P13/AIN7	I/O port P1	• CMOS 3-state output structure.	
P20–P27		I/O port P2	• A-D converter analog input pin • Key-on wake-up interrupt input pin
P30/AIN0 – P33/AIN3	I/O port P3	• 4-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure.	
P40/INT0	Input port P4	• 1-bit input port. • CMOS compatible input level.	
P41/INT1/ADT	I/O port P4	• 7-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output.	
P42/CNTR0/ BEEP+, P43/CNTR1/ BEEP-		• External interrupt pin • A-D trigger input pin • Timer function I/O pin	
P44/RxD, P45/TxD, P46/SCLK, P47/SRDY		• Serial I/O I/O pin	
C1, C2, C3	Voltage multiplier	• External capacitor connect pins for a voltage multiplier of LCD.	
Vss (NC), NC		• Non-function pins. • Leave the Vss (NC) pin open.	

PART NUMBERING

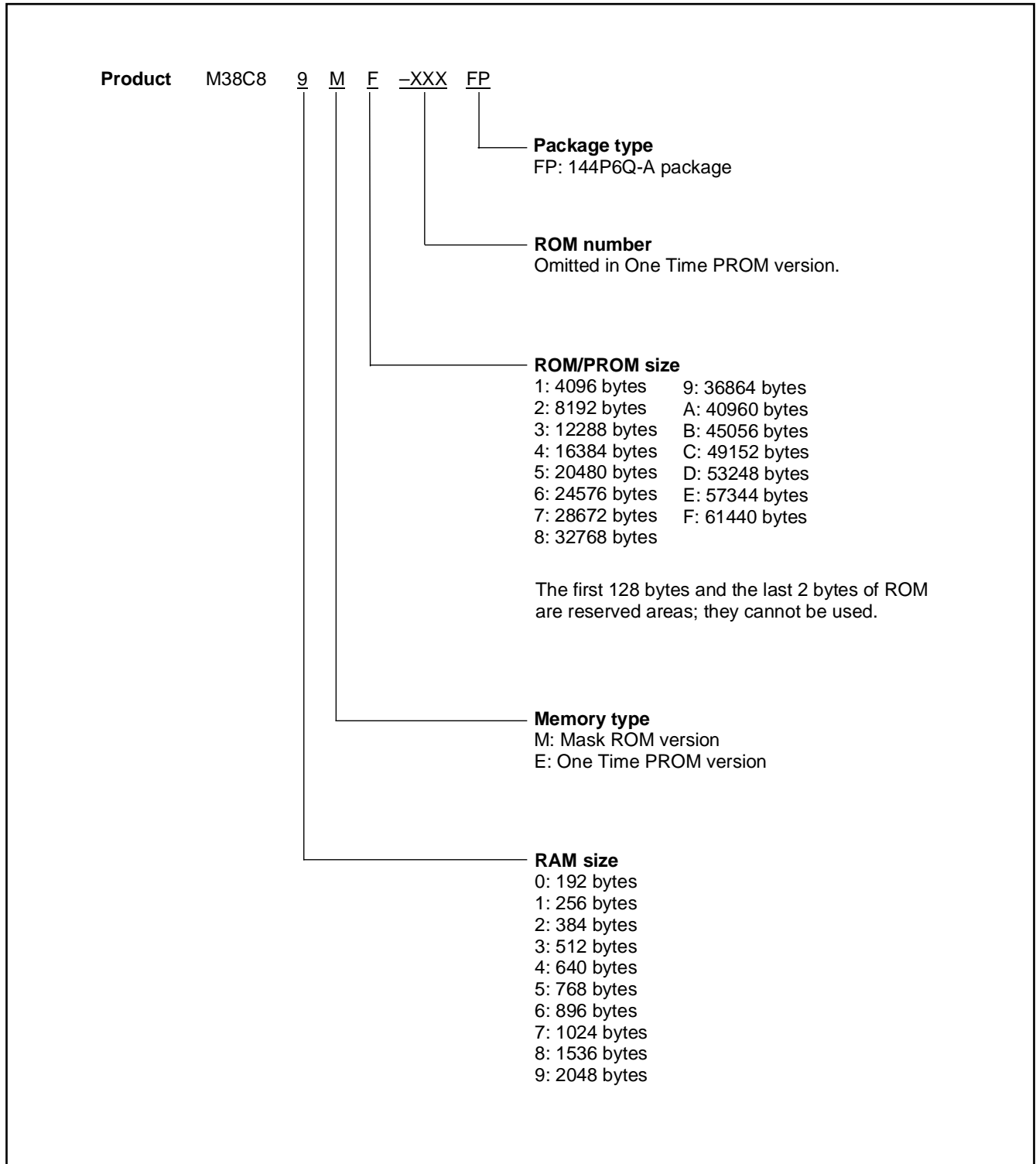


Fig. 3 Part numbering

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GROUP EXPANSION

Mitsubishi plans to expand the 38C8 group as follows.

Packages

144P6Q-A 0.5 mm-pitch plastic molded QFP

Memory Type

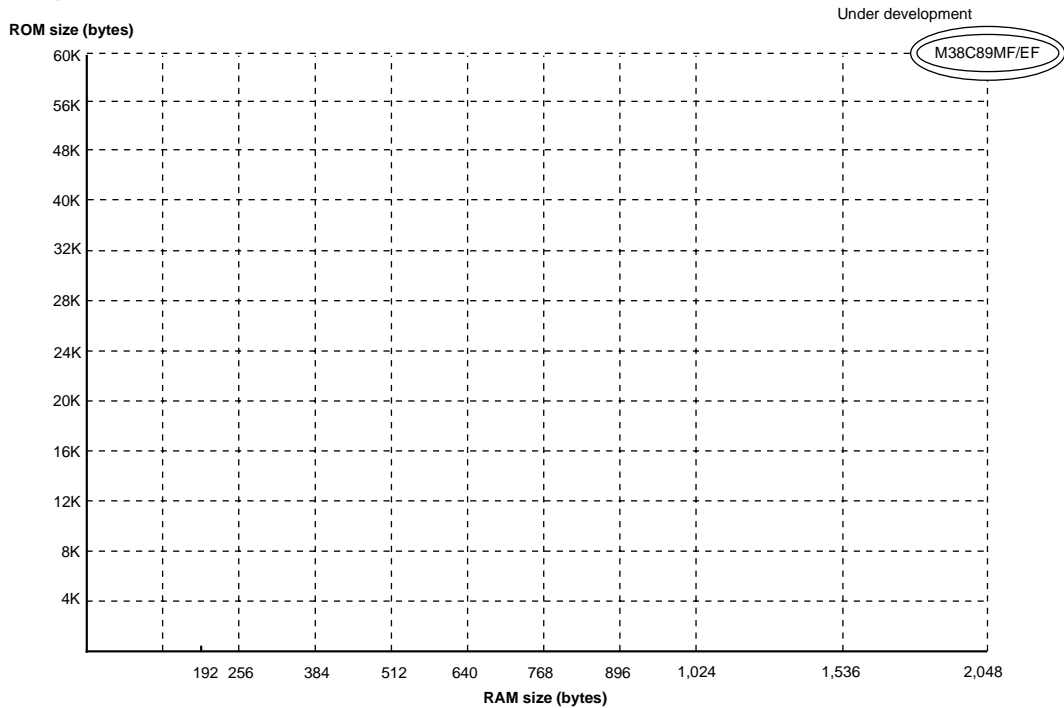
Support for mask ROM and One Time PROM versions

Memory Size

ROM/PROM size 60 K bytes

RAM size 2048 bytes

Memory Expansion Plan



Products under development or planning; the development schedule and specification may be revised without notice. The development of planning products may be stopped.

Fig. 4 Memory expansion plan

Currently planning products are listed below.

Table 2 Support products

As of Dec. 2000

Product name	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38C89MF-XXXXFP	61440 (61310)	2048	144P6Q-A	Mask ROM version
M38C89EFFP	61440 (61310)	2048	144P6Q-A	One Time PROM version

**FUNCTIONAL DESCRIPTION
 CENTRAL PROCESSING UNIT (CPU)**

The 38C8 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

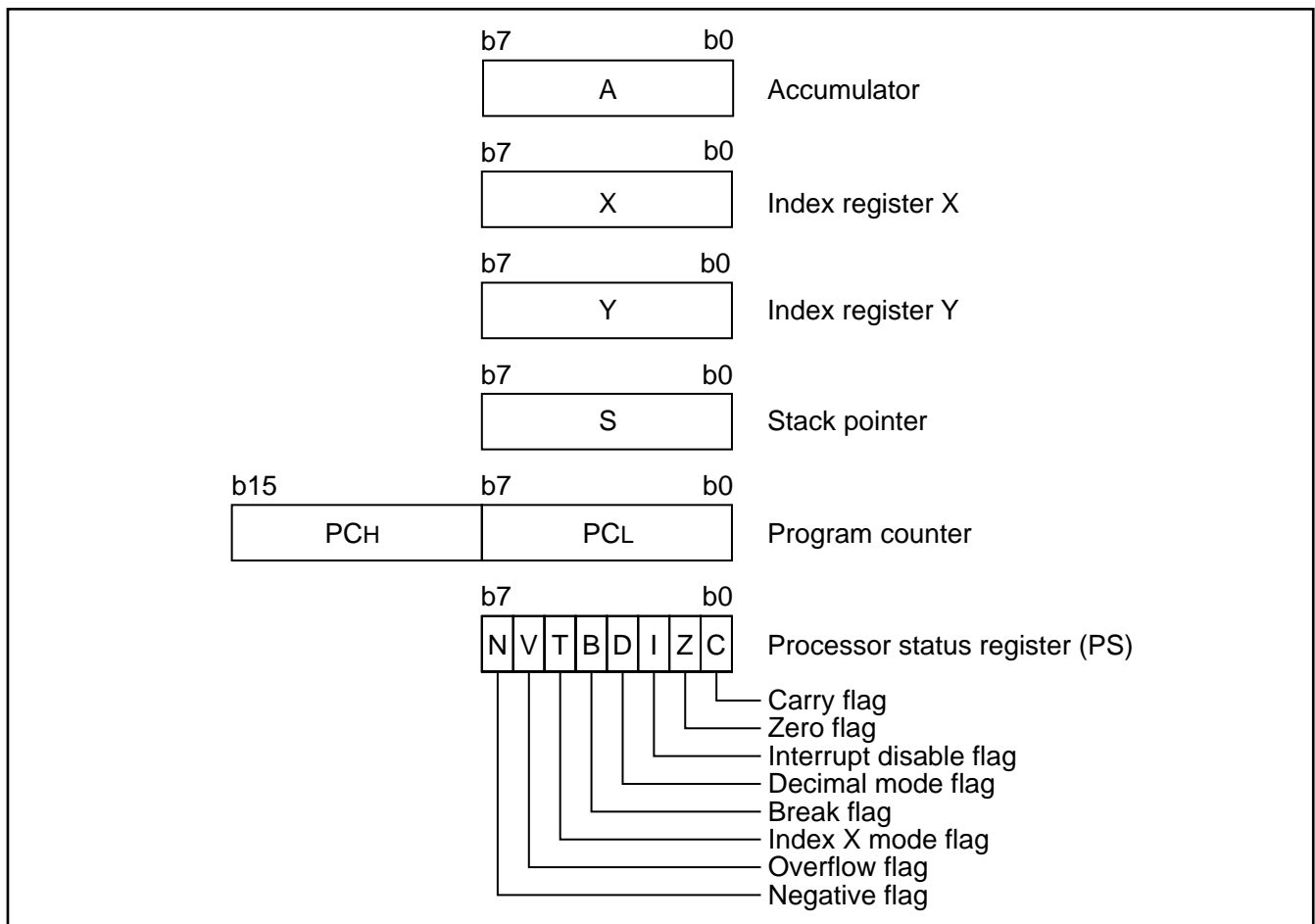
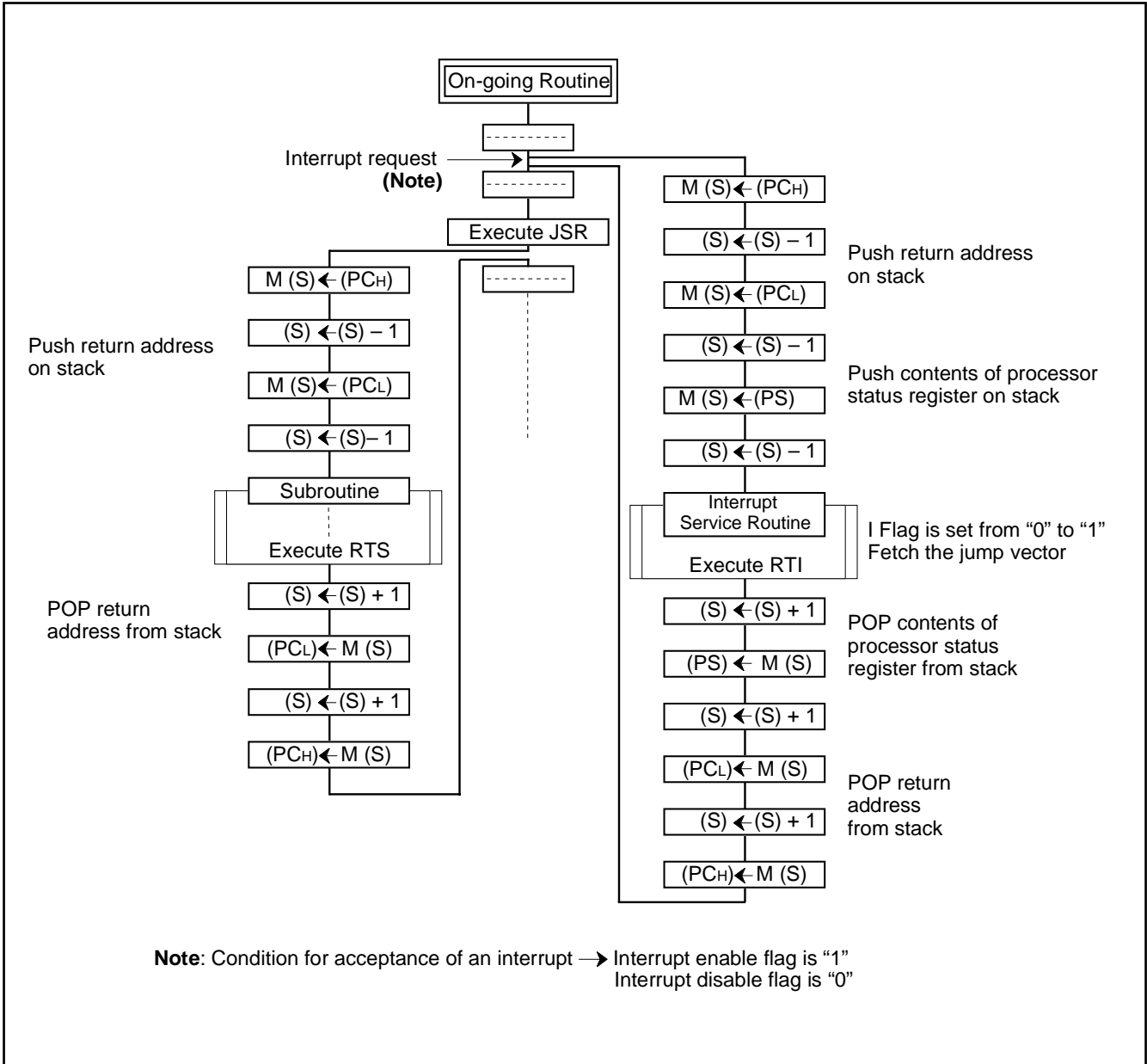


Fig. 5 740 Family CPU register structure



Note: Condition for acceptance of an interrupt → Interrupt enable flag is "1"
 Interrupt disable flag is "0"

Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)
 The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
- Bit 1: Zero flag (Z)
 The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".
- Bit 2: Interrupt disable flag (I)
 The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".
- Bit 3: Decimal mode flag (D)
 The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC

- Bit 4: Break flag (B)
 The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".
- Bit 5: Index X mode flag (T)
 When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.
- Bit 6: Overflow flag (V)
 The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.
- Bit 7: Negative flag (N)
 The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	-	SEI	SED	-	SET	-	-
Clear instruction	CLC	-	CLI	CLD	-	CLT	CLV	-

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address 003B16.

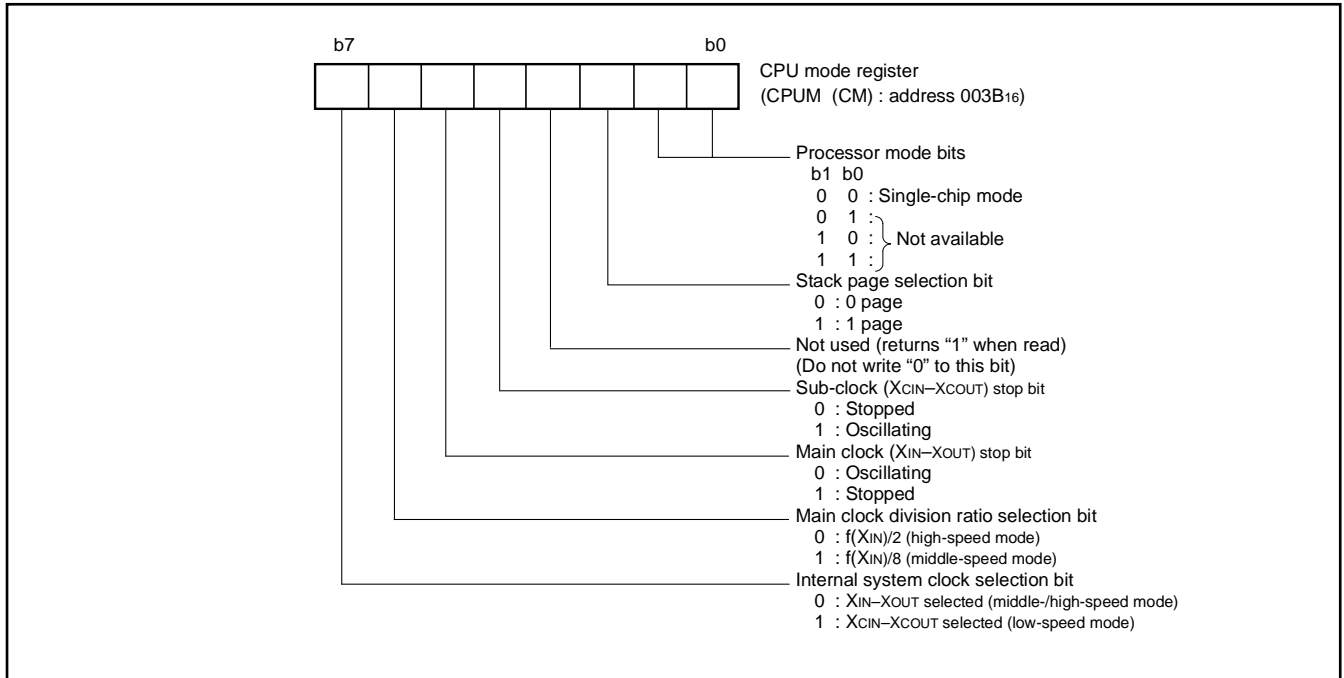


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

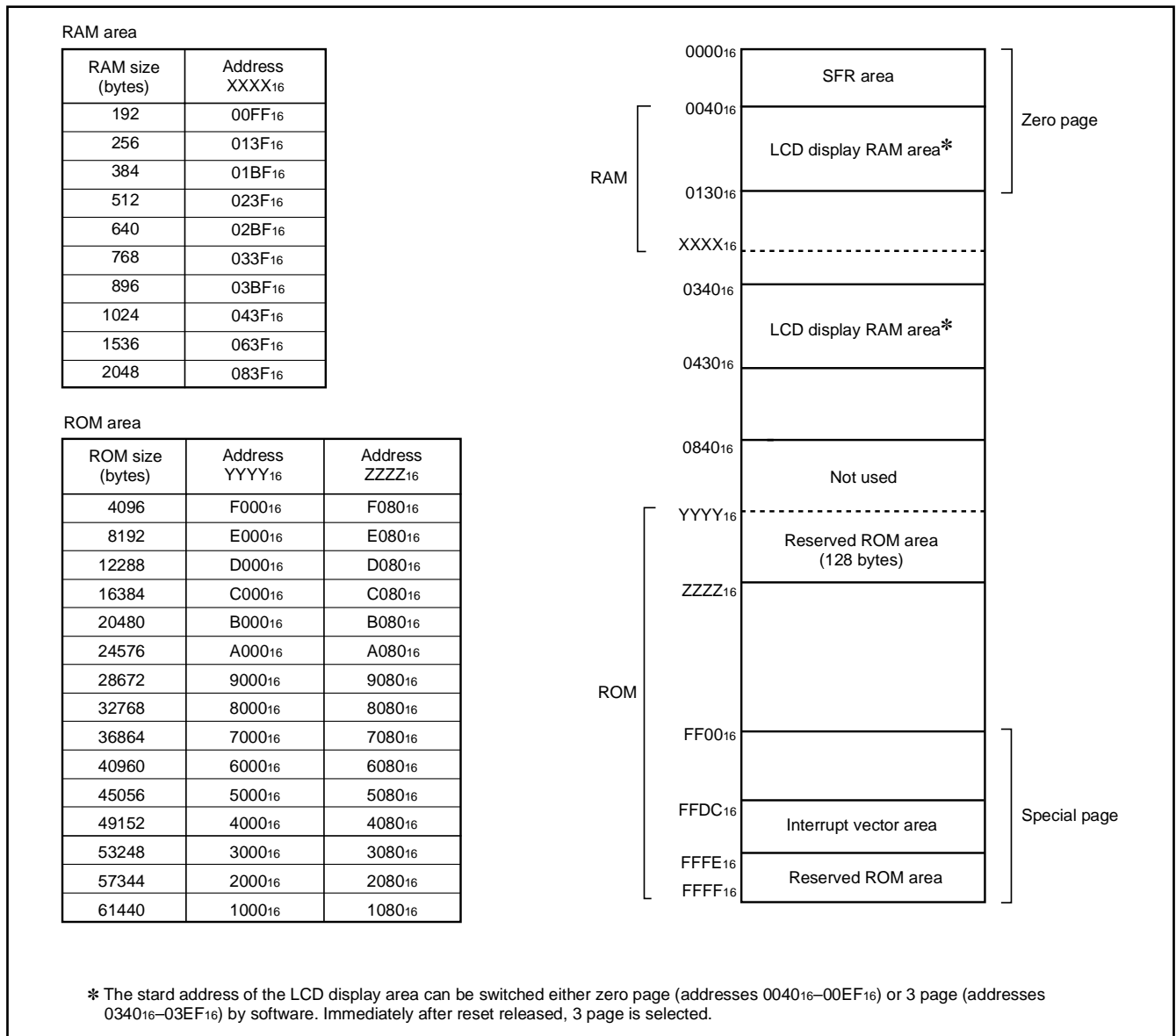


Fig. 8 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer X (low-order) (TXL)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer X (high-order) (TXH)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer Y (low-order) (TYL)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer Y (high-order) (TYH)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 1 (T1)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 2 (T2)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Timer 3 (T3)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Timer X mode register (TXM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer Y mode register (TYM)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 123 mode register (T123M)
000A ₁₆		002A ₁₆	
000B ₁₆		002B ₁₆	
000C ₁₆		002C ₁₆	
000D ₁₆		002D ₁₆	
000E ₁₆		002E ₁₆	
000F ₁₆		002F ₁₆	
0010 ₁₆		0030 ₁₆	
0011 ₁₆		0031 ₁₆	A-D control register (ADCON)
0012 ₁₆		0032 ₁₆	A-D conversion register (low-order) (ADL)
0013 ₁₆		0033 ₁₆	A-D conversion register (high-order) (ADH)
0014 ₁₆		0034 ₁₆	
0015 ₁₆		0035 ₁₆	
0016 ₁₆	PULL register A (PULLA)	0036 ₁₆	
0017 ₁₆	PULL register B (PULLB)	0037 ₁₆	LCD control register 1 (LC1)
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	0038 ₁₆	LCD control register 2 (LC2)
0019 ₁₆	Serial I/O status register (SIOSTS)	0039 ₁₆	LCD mode register (LM)
001A ₁₆	Serial I/O control register (SIOCON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆		003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆		003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆		003F ₁₆	Interrupt control register 2 (ICON2)

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

[Direction Registers]

The I/O ports P0–P3 and P41–P47 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pull-up Control

By setting the PULL register A (address 001616) or the PULL register B (address 001716), ports P0 to P4 except for port P40 can control pull-up with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.

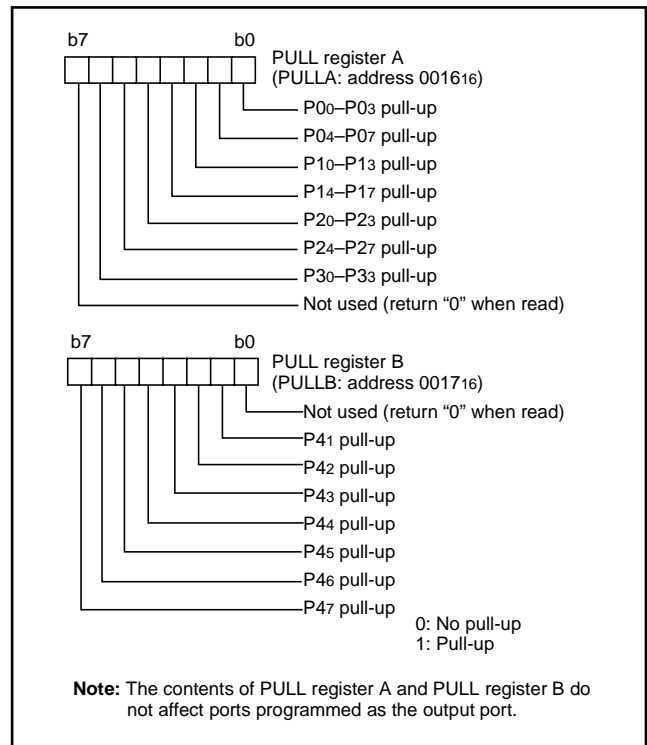


Fig. 10 Structure of PULL register A and PULL register B

Table 5 List of I/O port function

Pin	Name	Input/Output	I/O format	Non-port function	Related SFRs	Ref. No.		
P00–P07	Port P0	Input/Output, individual bits	CMOS 3-state output		PULL register A	(1)		
P10/AN4– P13/AN7	Port P1				PULL register A A-D control register	(2)		
P14–P17					PULL register A	(1)		
P20–P27	Port P2	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt in- put	PULL register A Interrupt control register 2	(1)		
P30/AN0– P33/AN3	Port P3	Input/Output, individual bits	CMOS 3-state output	A-D converter input	PULL register A A-D control register	(2)		
P40/INT0	Port P4	Input	CMOS compatible input level	External interrupt in- put	PULL register B Interrupt edge select register	(3)		
P41/INT1		Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Timer X function I/O	PULL register B Timer X mode register	(4)		
P42/CNTR0/ BEEP+				Timer Y function input	PULL register B Timer Y mode register	(5)		
P43/CNTR1/ BEEP-				Serial I/O funtion I/O	PULL register B Serial I/O control register Serial I/O status register UART control register			(6)
P44/RxD								(7)
P45/TxD								(8)
P46/SCLK								(9)
P47/SRDY								
COM0–COM7, COM8–COM15				Common	Output	LCD common output		LCD mode register
SEG0/COM16– SEG7/COM23, SEG60/COM31– SEG67/COM24	Segment/ Common	LCD segment output LCD common output						
SEG8–SEG59	Segment	LCD segment output						

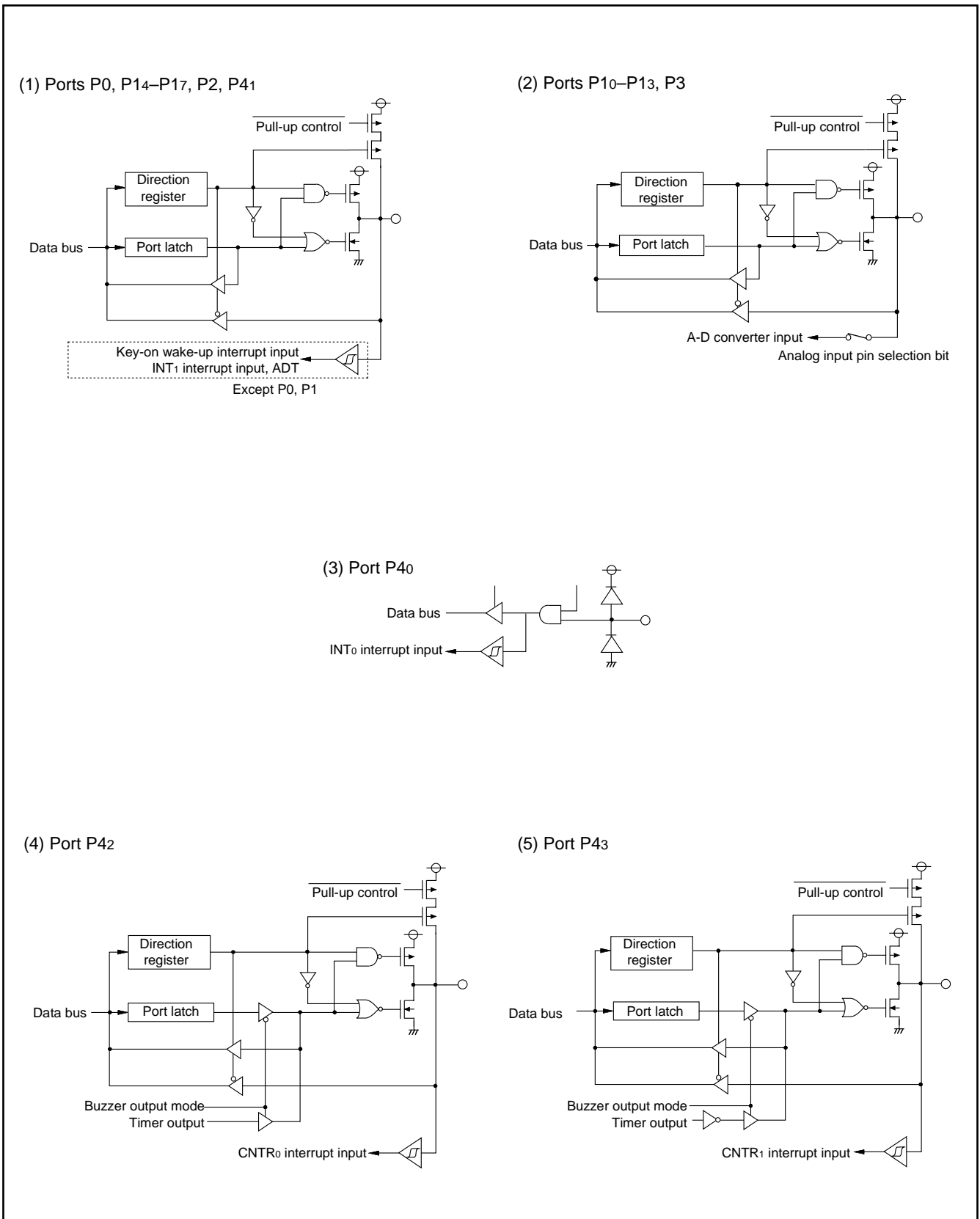
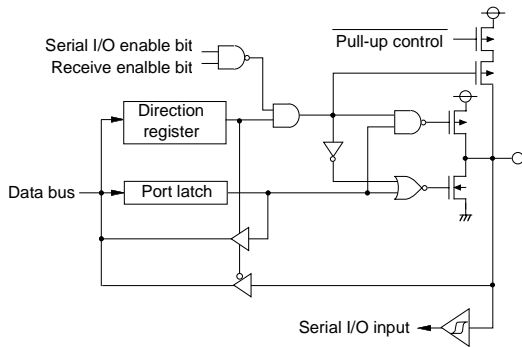
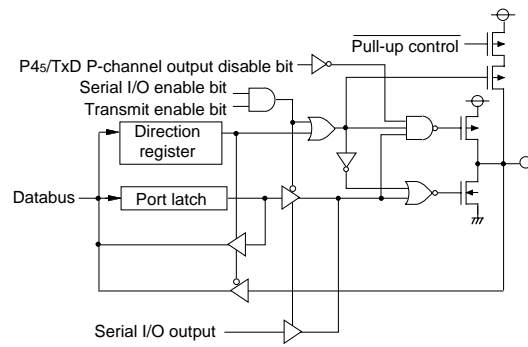


Fig. 11 Port block diagram (1)

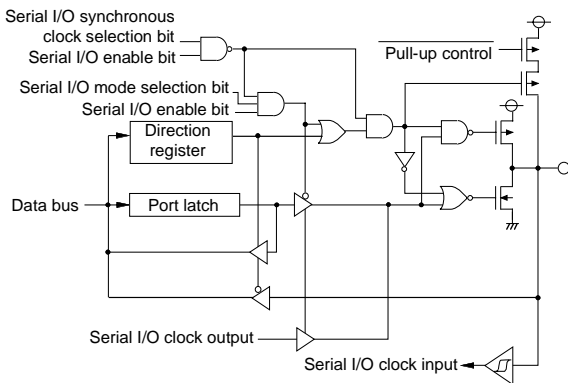
(6) Port P44



(7) Port P45



(8) Port P46



(9) Port P47

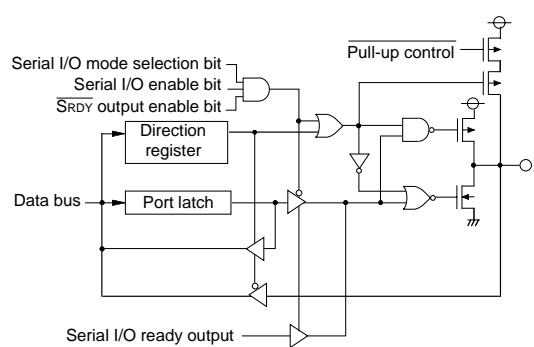


Fig. 12 Port block diagram (2)

INTERRUPTS

Interrupts occur by fifteen sources: six external, eight internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge
 Related register: Interrupt edge selection register (address 3A16)
 Timer X mode register (address 2716)
 Timer Y mode register (address 2816)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
 Related register: AD control register (address 3116)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

- ①Set the corresponding interrupt enable bit to "0" (disabled).
- ②Set the interrupt edge select bit (active edge switch bit) or the interrupt source select bit to "1".
- ③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the corresponding interrupt enable bit to "1" (enabled).

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Serial I/O reception	4	FFF716	FFF616	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O transmission	5	FFF516	FFF416	At completion of serial I/O transmission shift or when transmission buffer is empty	Valid when serial I/O is selected
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
Timer 2	8	FFEF16	FFEE16	At timer 2 underflow	
Timer 3	9	FFED16	FFEC16	At timer 3 underflow	
CNTR0	10	FFE816	FFE716	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	11	FFE616	FFE516	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Timer 1	12	FFE316	FFE216	At timer 1 underflow	
Key input (Key-on wake-up)	13	FFE116	FFE016	At falling of port P2 (at input) input logical level AND	External interrupt (falling valid)
A-D conversion	14	FFDF16	FFDE16	At completion of A-D conversion	Valid when A-D conversion interrupt is selected
BRK instruction	15	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

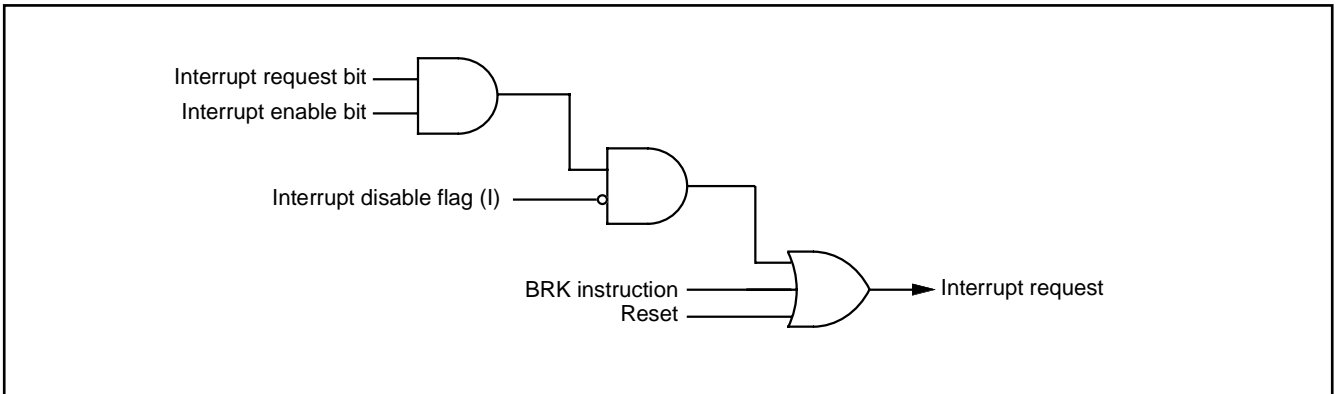


Fig. 13 Interrupt control

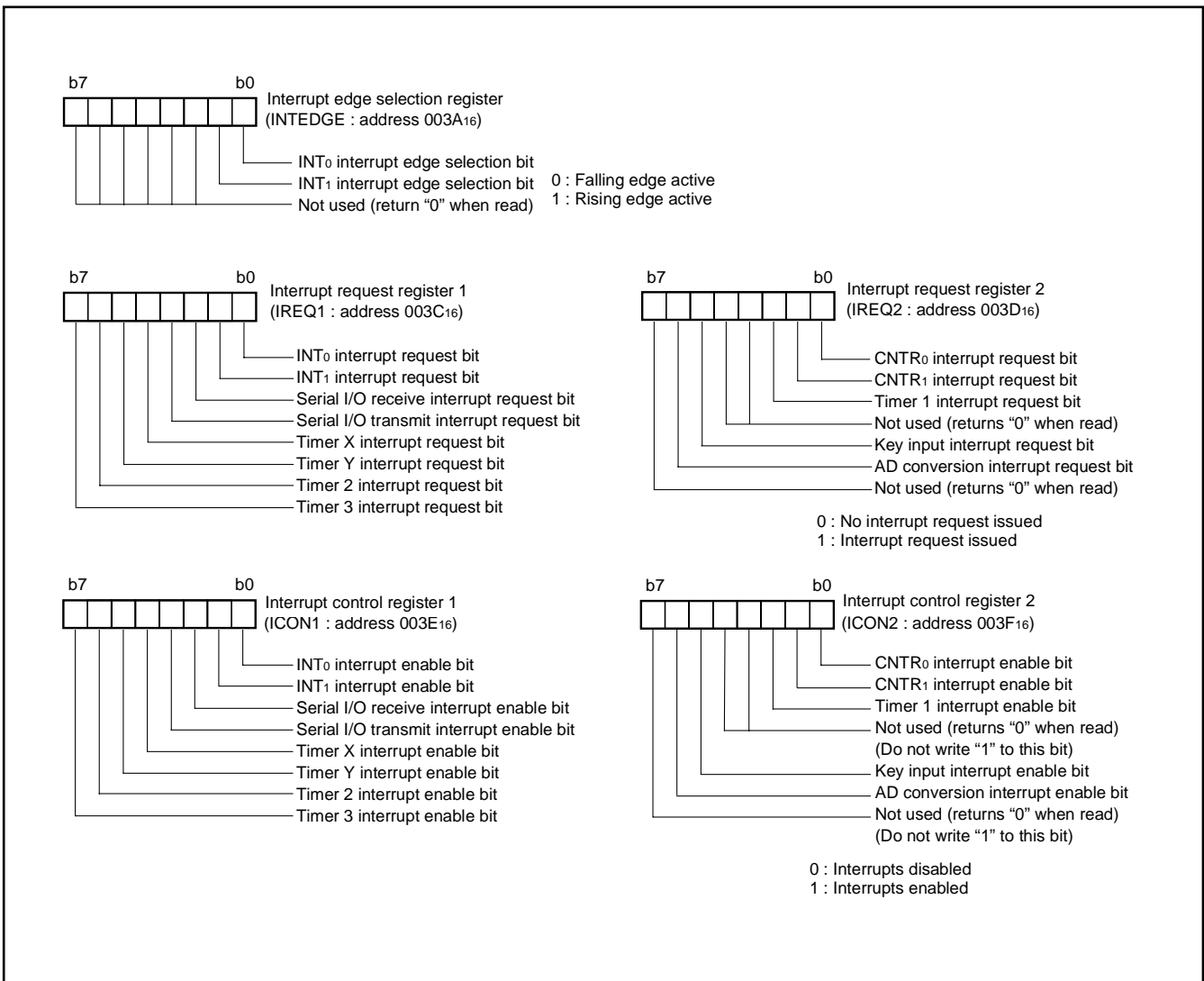


Fig. 14 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by applying "L" level to any pin of port P2 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example

of using a key input interrupt is shown in Figure 15, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P20-P23.

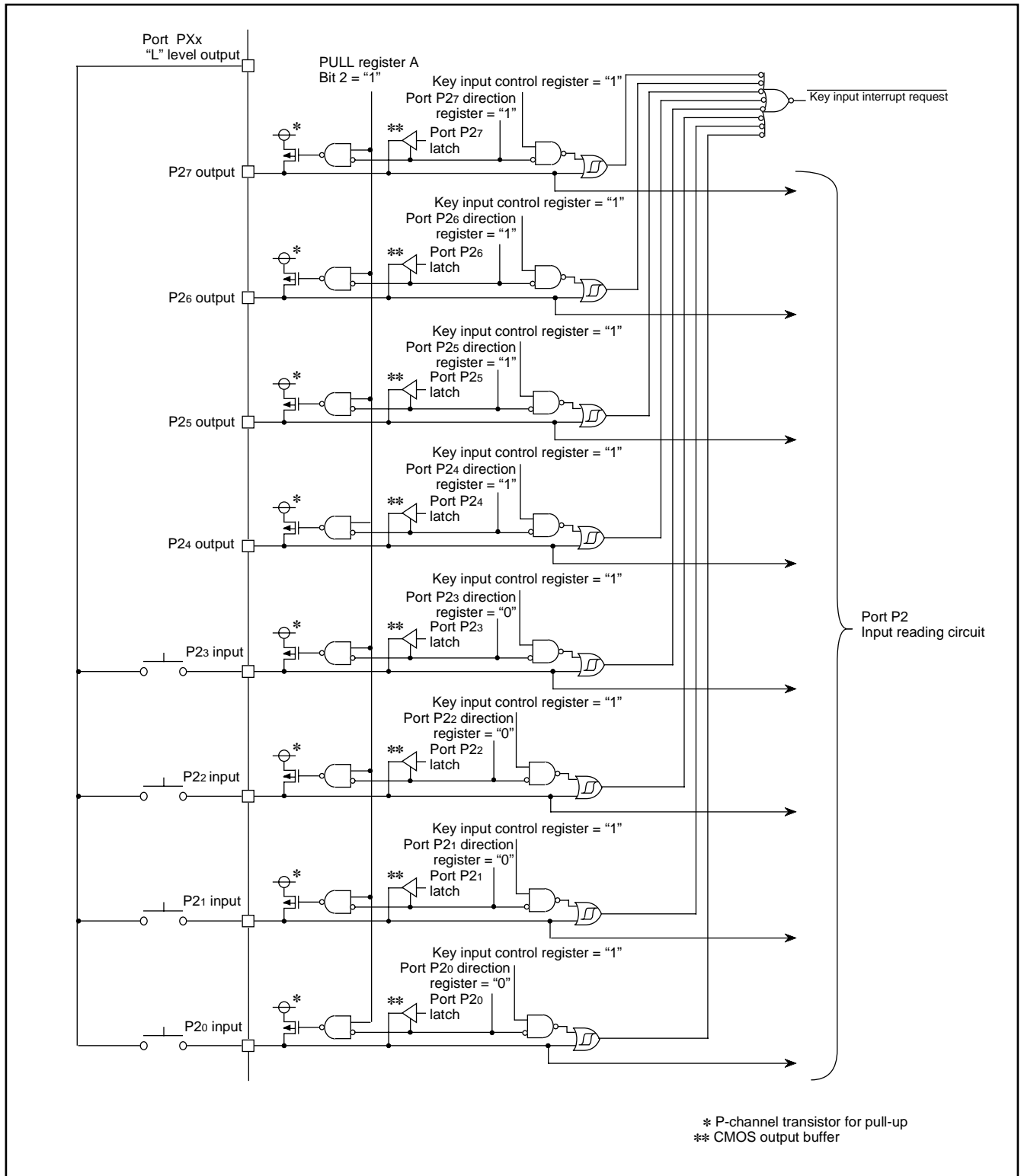


Fig. 15 Connection example when using key input interrupt and port P2 block diagram

TIMERS

The 38C8 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer

is set to "1".

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

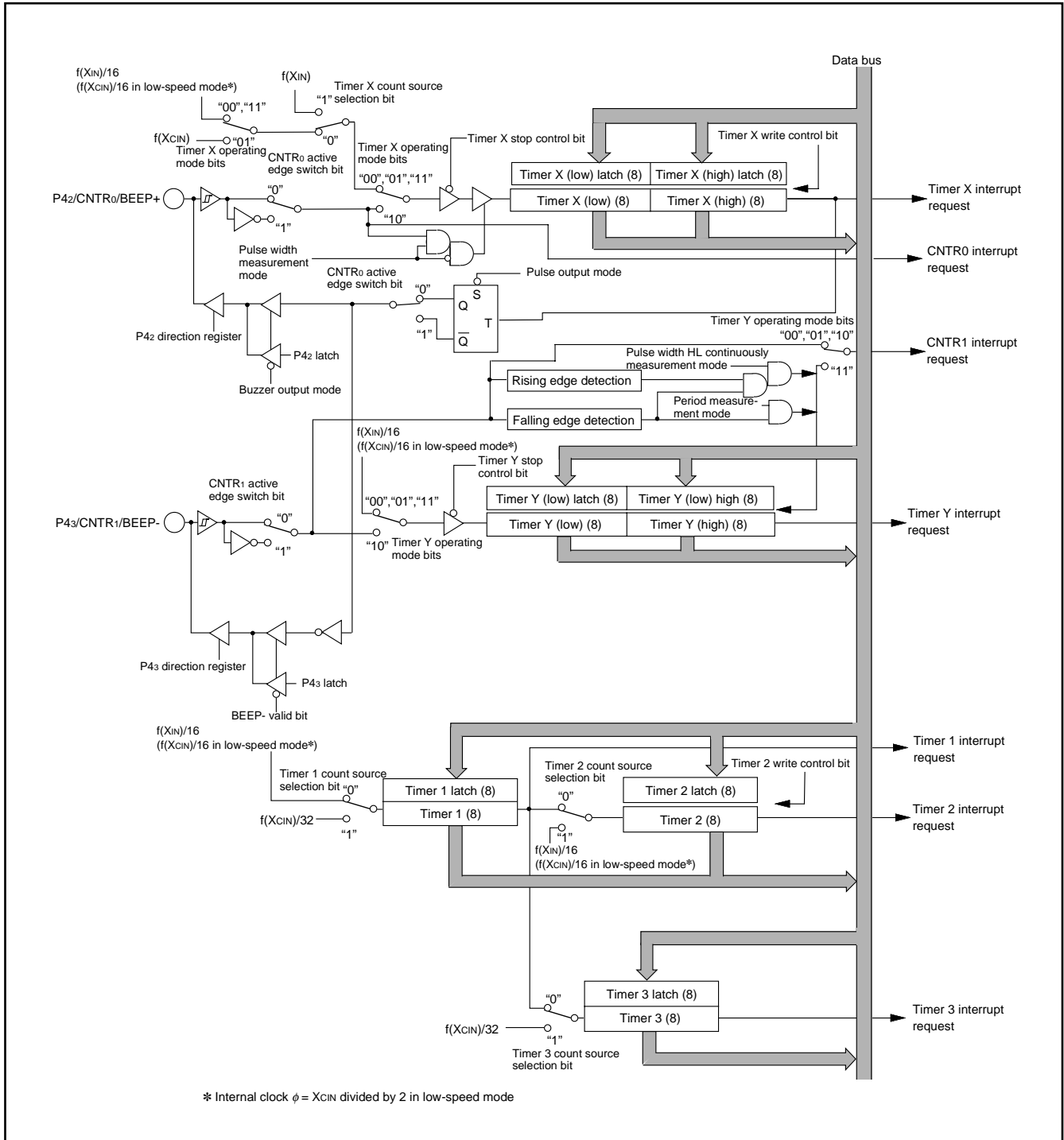


Fig. 16 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write by setting the timer X mode register.

(1) Timer Mode

When the timer X count source selection bit is "0", the timer counts $f(XIN)/16$ (or $f(XCIN)/16$ in low-speed mode). When it is "1", the timer counts $f(XIN)$.

(2) Buzzer Output Mode

Each time the timer underflows, a signal output from the BEEP+ pin is inverted. When the BEEP- valid bit is "1", the opposite phase of BEEP+ signal is output from the BEEP- pin. When using the BEEP+ pin and the BEEP- pin, set ports shared with these pins to output.

(3) Event Counter Mode

The timer counts signals input through the CNTR0 pin. Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the port shared with the CNTR0 pin to input.

(4) Pulse Width Measurement Mode

When the timer X count source selection bit is "0", the count source is $f(XIN)/16$ (or $f(XCIN)/16$ in low-speed mode). When it is "1", the count source is $f(XIN)$.

If CNTR0 active edge switch bit is "0", the timer counts while the input signal of CNTR0 pin is at "H". If it is "1", the timer counts while the input signal of CNTR0 pin is at "L". When using a timer in this mode, set the port shared with the CNTR0 pin to input.

●Timer X write control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.

If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.

If the value is written in latch only, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

■Notes on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

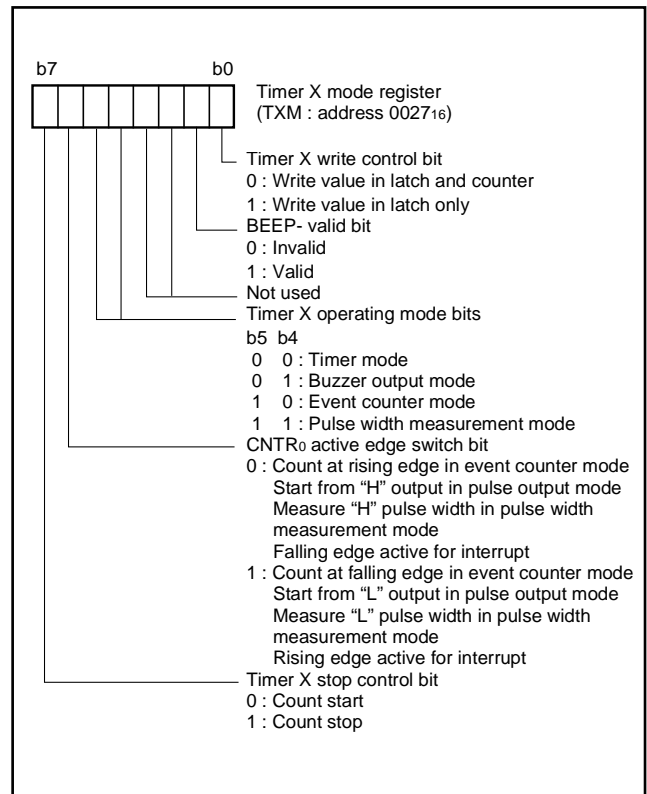


Fig. 17 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer Mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Period Measurement Mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the port shared with the CNTR1 pin to input.

(3) Event Counter Mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the port shared with the CNTR1 pin to input.

(4) Pulse Width HL Continuously Measurement Mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the port shared with the CNTR1 pin to input.

■Notes on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in the pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

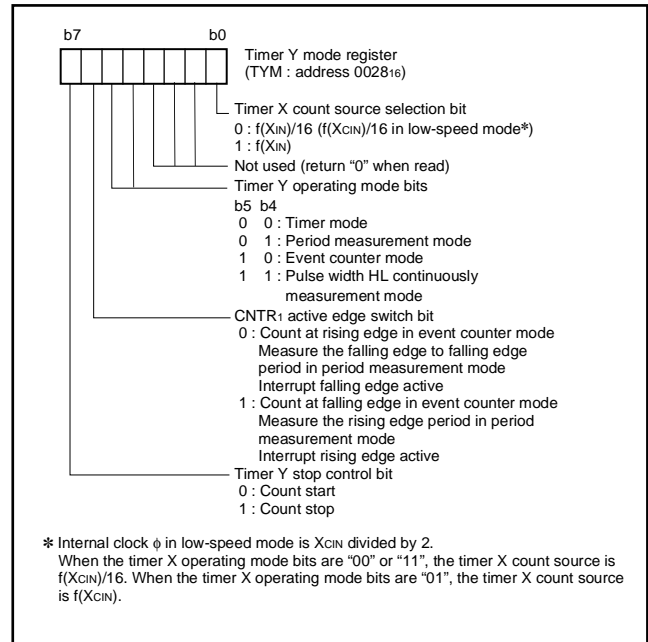


Fig. 18 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by the timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

● **Timer 2 write control**

If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

■ **Notes on timer 1 to timer 3**

When the count source of timer 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

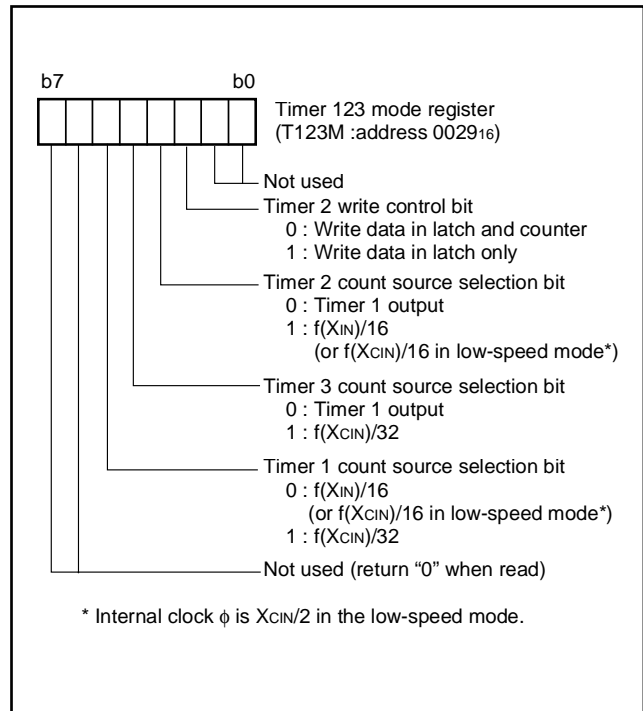


Fig. 19 Structure of timer 123 mode register

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O can be selected by setting the mode selection bit of the serial I/O control register to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer registers.

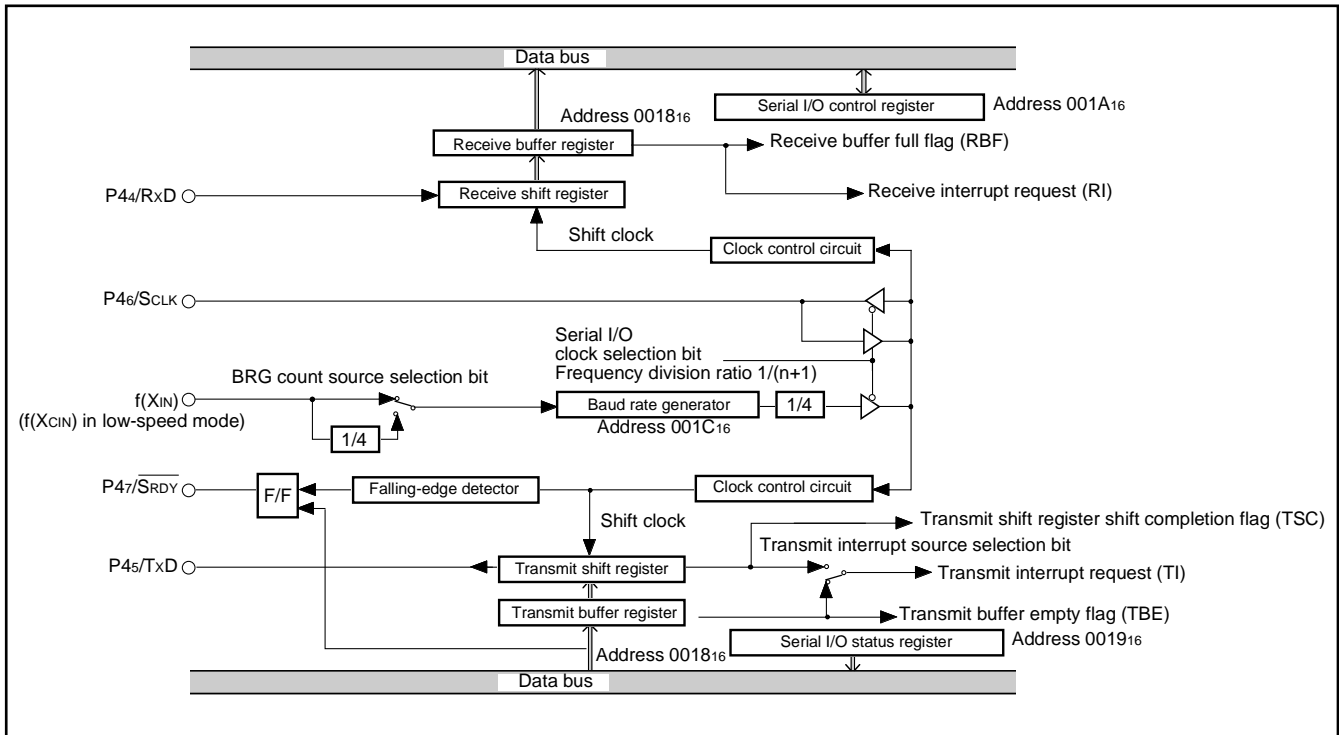


Fig. 20 Block diagram of clock synchronous serial I/O

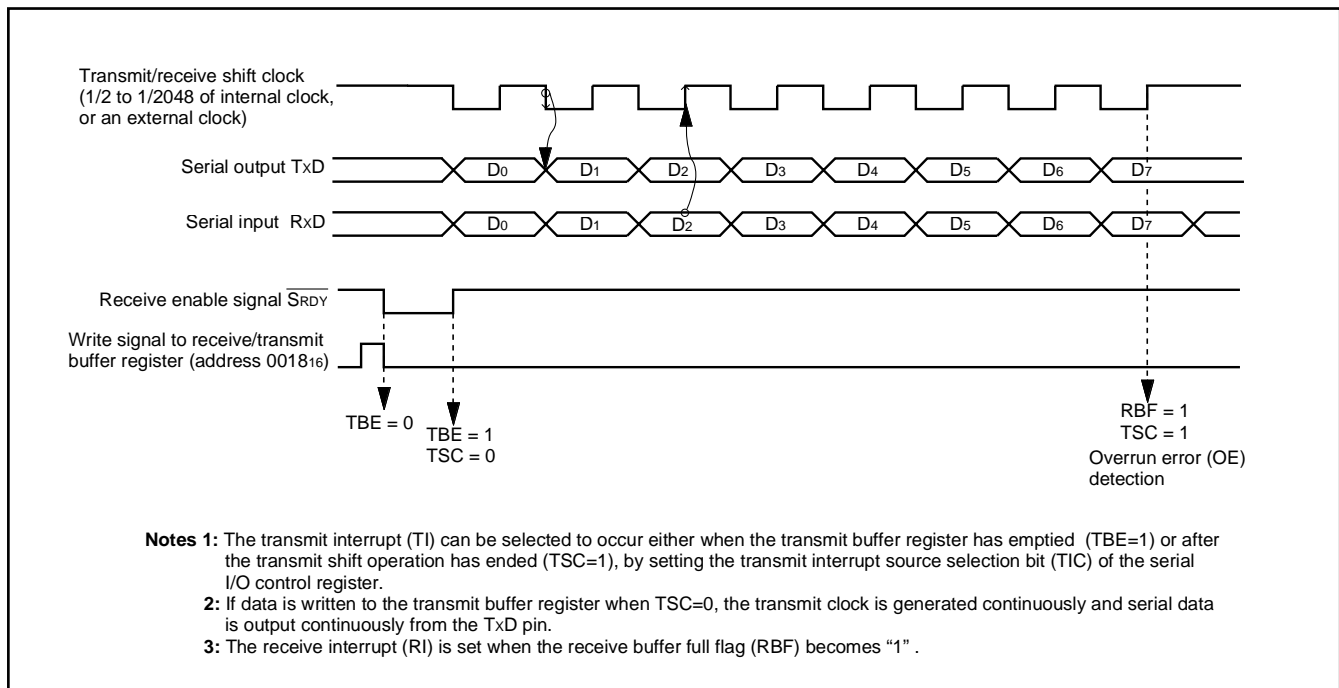


Fig. 21 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer register,

but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

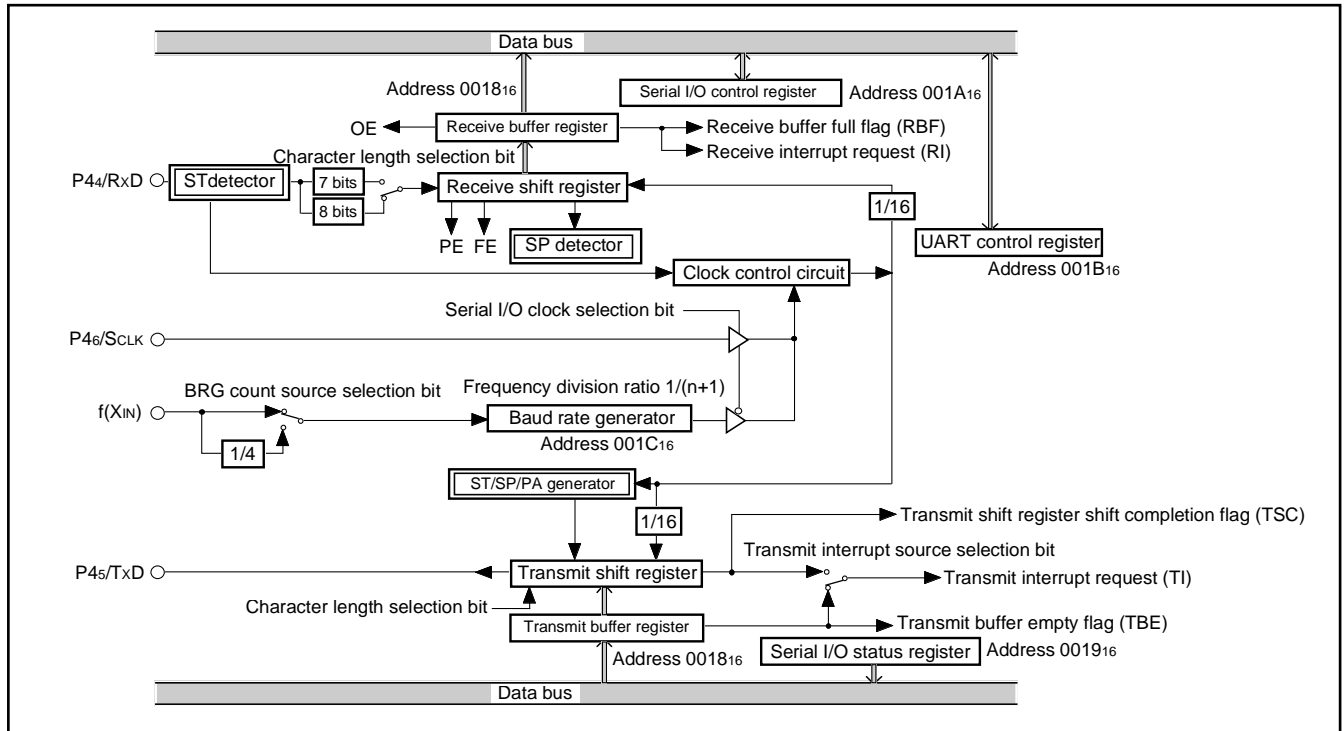


Fig. 22 Block diagram of UART serial I/O

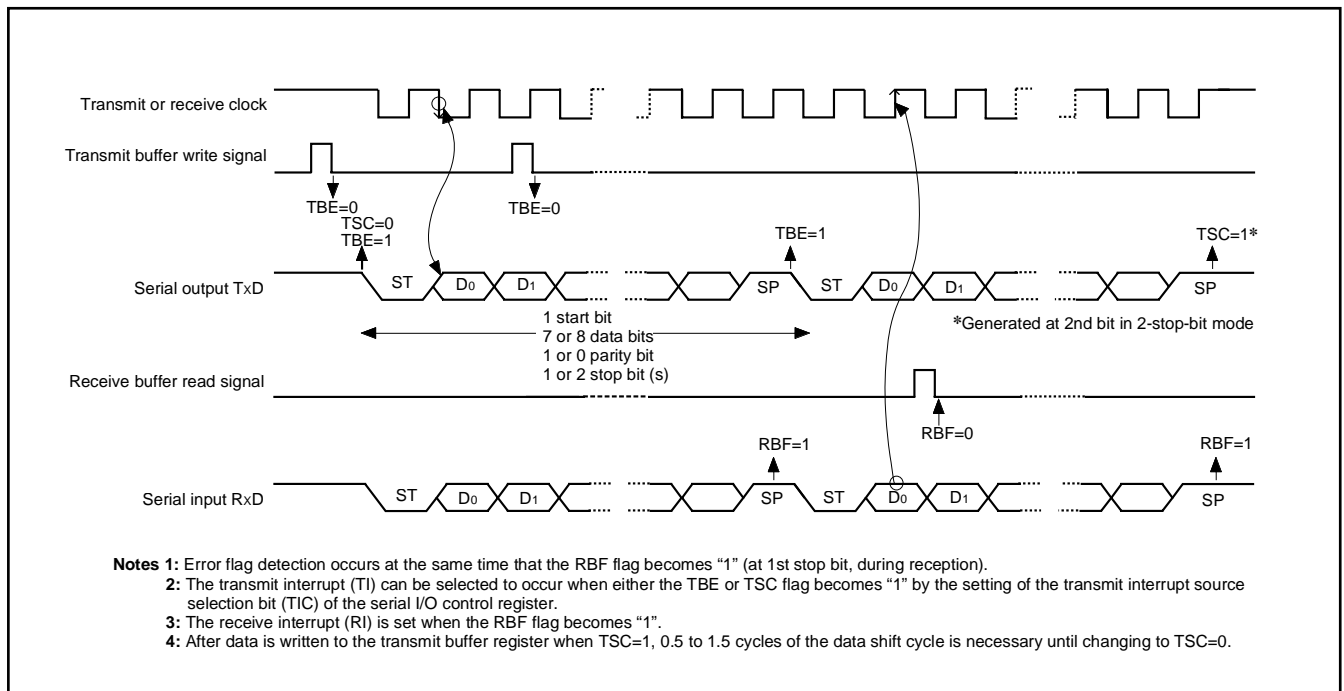


Fig. 23 Operation of UART serial I/O function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 001816

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is "0".

[Serial I/O Status Register (SIOSTS)] 001916

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE. Writing "0" to the serial I/O enable bit (SIOE) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O Control Register (SIOCON)] 001A16

The serial I/O control register contains eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] 001B16

This is a 5 bit register containing four control bits, which are valid when UART is selected and set the data format of an data receiver/transfer, and one control bit, which is always valid and sets the output structure of the P45/TxD pin.

[Baud Rate Generator(BRG)] 001616

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

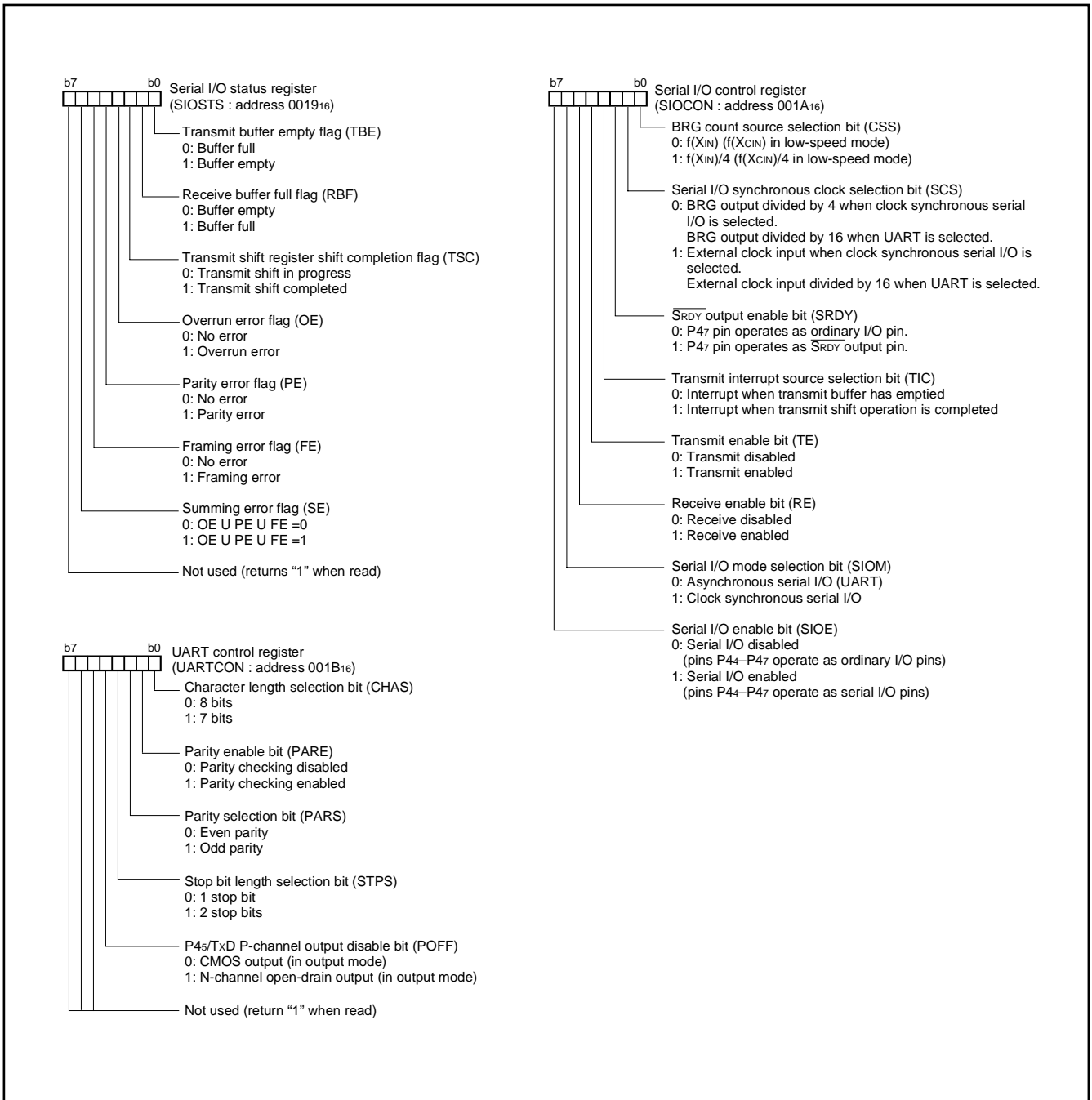


Fig. 24 Structure of serial I/O control registers

A-D CONVERTER

[A-D Conversion Registers (ADL, ADH)] 003216, 003316

The A-D conversion registers are read-only registers that contain the result of an A-D conversion. During A-D conversion, do not read these registers.

[A-D Control Register (ADCON)] 003116

The A-D control register controls the A-D conversion process. Bits 0 to 2 are analog input pin selection bits. Bit 3 is an A-D conversion completion bit and "0" during A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. When bit 5, which is the AD external trigger valid bit, is set to "1", A-D conversion is started even by a rising edge or falling edge of an ADT input.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Because the comparator consists of a capacitor coupling, a deficient conversion speed may cause lack of electric charge and make the conversion accuracy worse. When A-D conversion is performed in the middle-speed mode or the high-speed mode, set $f(XIN)$ to at least 500 kHz.

In the low-speed mode, A-D conversion is performed by using the built-in self-oscillation circuit. Therefore, there is no limitation in the lower bound frequency of $f(XIN)$.

Trigger Start

When using the A-D external trigger, set the port shared with the ADT pin to input. The polarity of INT1 interrupt edge also applies to the A-D external trigger. When the INT1 interrupt edge polarity is switched after an external trigger is validated, an A-D conversion may be started.

Resistor ladder

The resistor ladder outputs the comparison voltage by dividing the voltage between VDD and VSS by resistance.

Channel Selector

The channel selector selects one of the ports P33/AIN3–P30/AIN0 and ports P10/AIN4–P13/AIN7, and inputs it to the comparator.

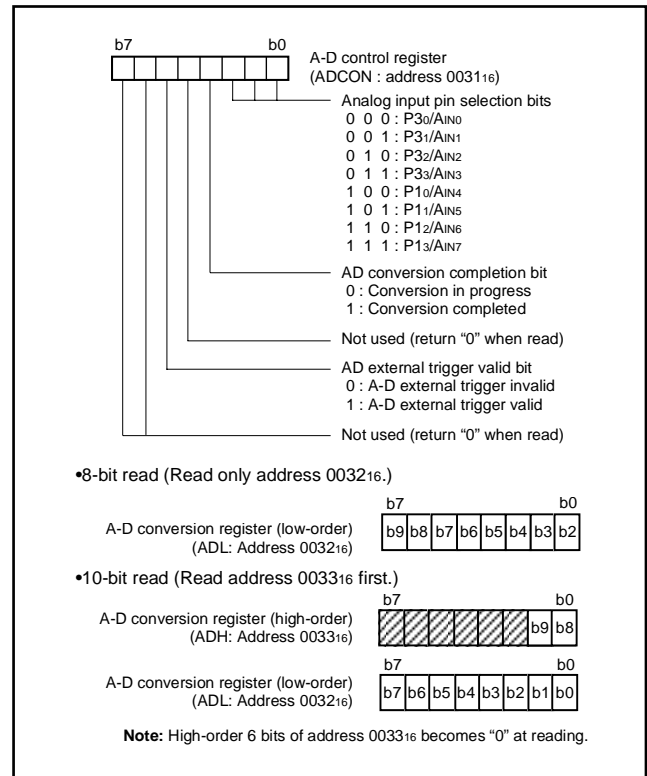


Fig. 25 Structure of A-D control register

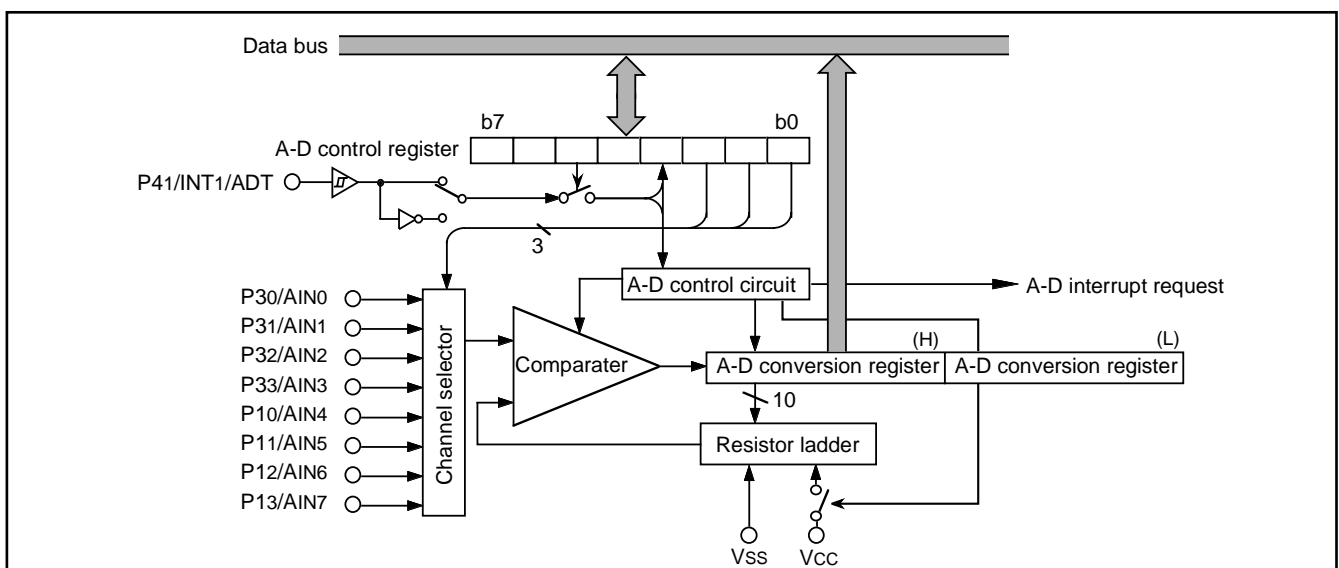


Fig. 26 A-D converter block diagram

LCD CONTROLLER/DRIVER

The 38C8 group has the built-in Liquid Crystal Display (LCD) controller/driver consisting of the following.

- 240-byte LCD display RAM
- 52 or 68 segment driver
- 16 or 32 common driver
- LCD clock generator
- Timing controller

- Bias controller
- Voltage multiplier
- LCD mode register
- LCD control registers 1, 2

A maximum of 68 segment output pins and 32 common output pins can be used for control of external LCD display.

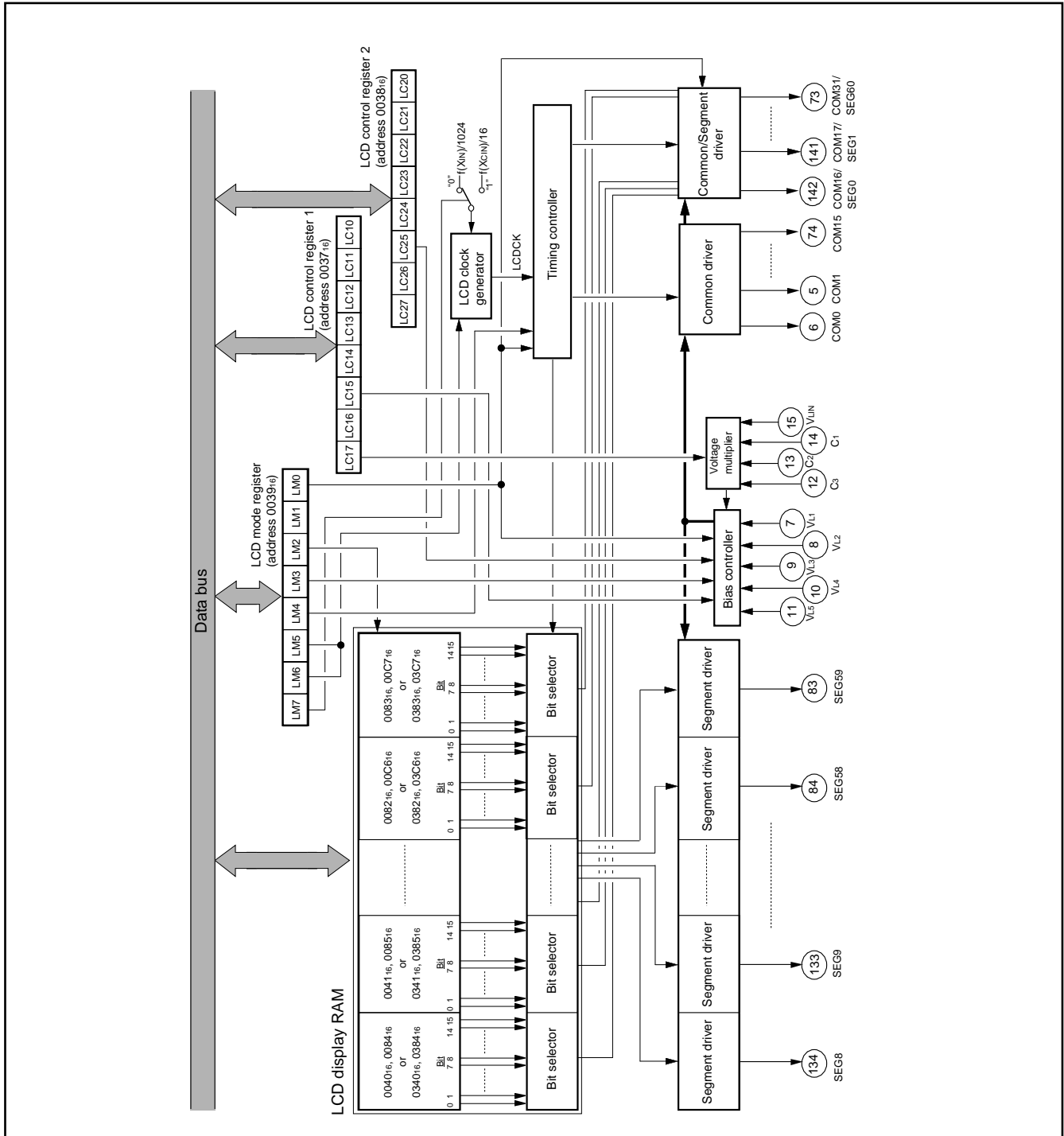


Fig. 27 Block diagram of LCD controller/driver

LCD Controller/Driver Function

The controller/driver performs the bias control and the time sharing control by the LCD control registers 1, 2 (LC1, LC2), and the LCD mode register (LM). The data of corresponding LCDRAM is output from the segment pins according to the output timing of the common pins.

The 38C8 group has the voltage multiplier only for LCD in addition to LCD controller/driver .

[LCD mode register (LM)] 003916

The LCD mode register is used for setting the LCD controller/driver according to the LCD panel used.

[LCD control register 1 (LC1)] 003716

The LCD control register 1 controls the voltage multiplier and built-in resistance.

[LCD control register 2 (LC2)] 003816

The LCD control register 2 is read-only. Setting "1" to bit 5 makes built-in resistance low resistance, and can raise drivability of the segment pins and the common pins.

Table 7 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
16	16 X 68 dots (5 X 7 dots + cursor 2 lines)
32	32 X 52 dots (5 X 7 dots + cursor 4 lines)

Note: When executing the STP instruction while operating LCD, execute the STP instruction after prohibiting LCD (set "0" to bit 3 of the LCD mode register).

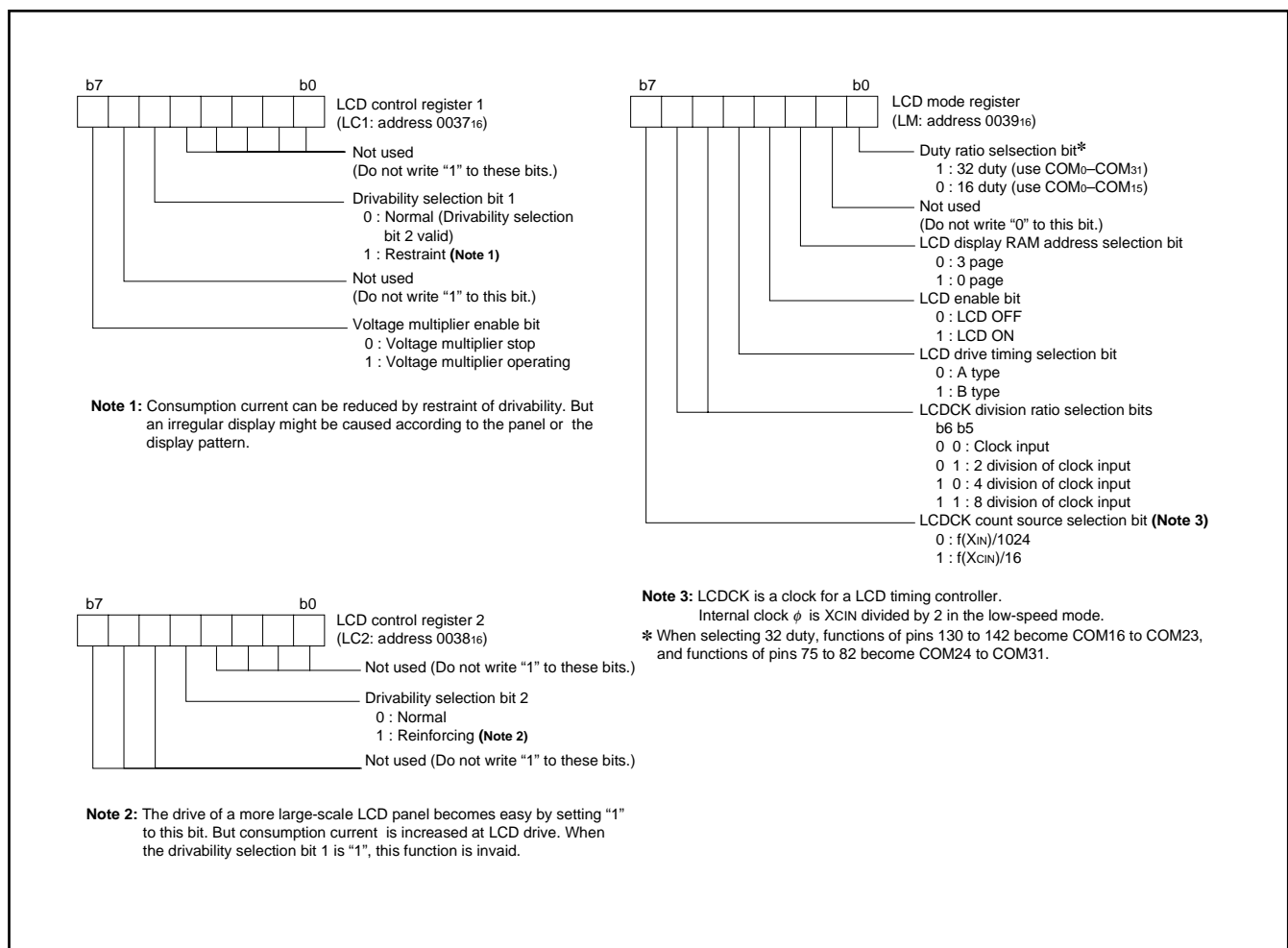


Fig. 28 Structure of LCD control register

Voltage Multiplier

When the voltage multiplier is operated after a reference voltage for boosting is applied to LCD power supply VLIN, a voltage that is three times as large as VLIN pin occurs at the VL5 pin. Operate the voltage multiplier after applying a reference voltage for boosting to VLIN.

Bias Control

In the LCD power source pins (VL1–VL5), a proper level is automatically generated in 1/32 and 1/16 duty ratio. The quality of the LCD display can be stabilized by connecting the capacitor for smoothness between Vss and these pins.

Table 8 Bias control and applied voltage to VL1–VL5

Bias value	Voltage value
1/7 bias	VL5 = VLCD
	VL4 = 6/7 VLCD
	VL3 = 5/7 VLCD
	VL2 = 2/7 VLCD
	VL1 = 1/7 VLCD
1/5 bias	VL5 = VLCD
	VL4 = 4/5 VLCD
	VL3 = 3/5 VLCD
	VL2 = 2/5 VLCD
	VL1 = 1/5 VLCD

Note: VLCD is a value which can be supplied to the LCD panel. Set value which is less than maximum ratings to VLCD.

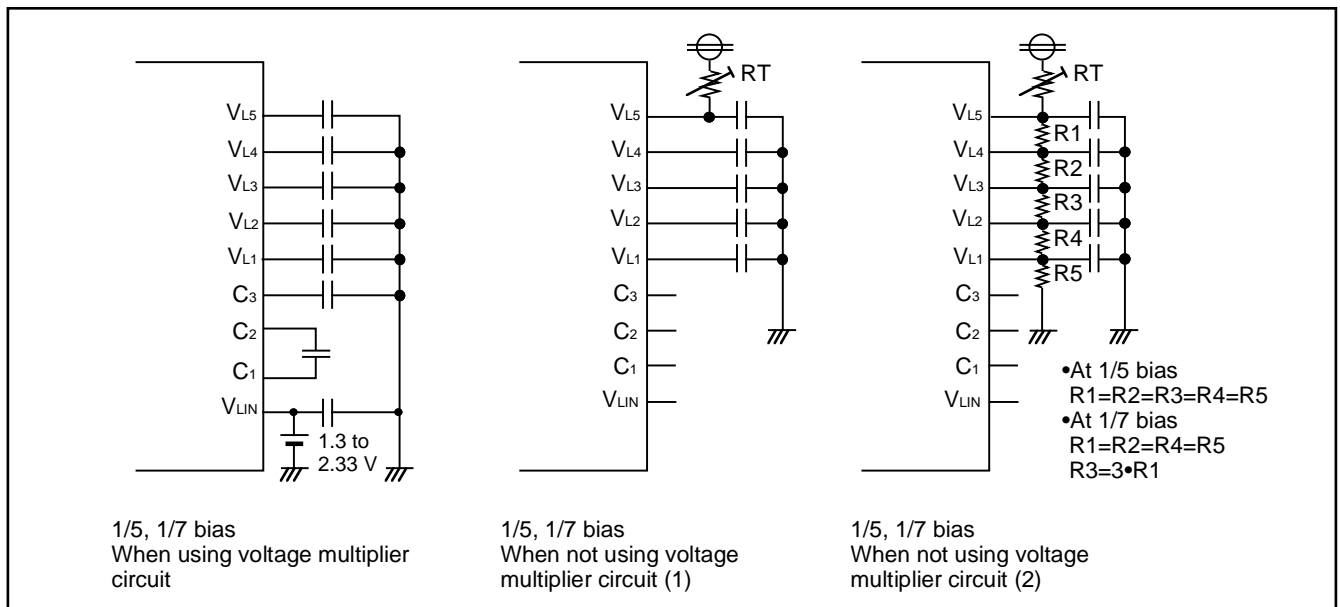


Fig. 29 Example of circuit at each bias

Common Pin and Duty Ratio Control

The common pins (COM0–COM31) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bit (bit 0 of the LCD mode register).

Table 9 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit	Common pins used
16	0	COM0–COM15 (Note)
32	1	COM0–COM31

Note: The SEG0/COM16–SEG7/COM23 pins are used as the SEG0–SEG7.
 The SEG67/COM24–SEG60/COM31 pins are used as the SEG67–SEG60.

LCD Display RAM

Addresses 004016 to 012F16 is the designated RAM for the LCD display. When “1” are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{(duty ratio)}}$$

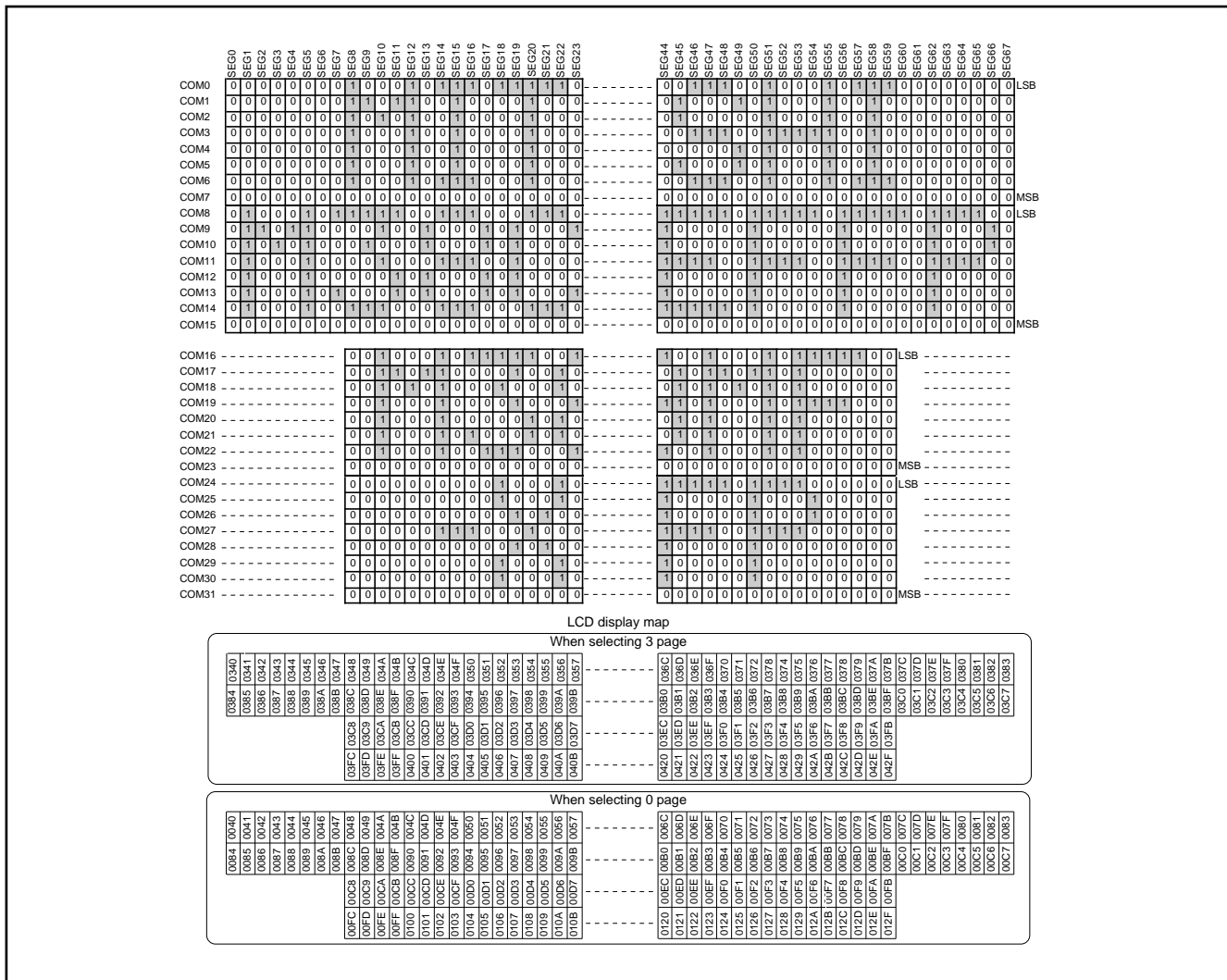


Fig. 30 LCD display RAM map

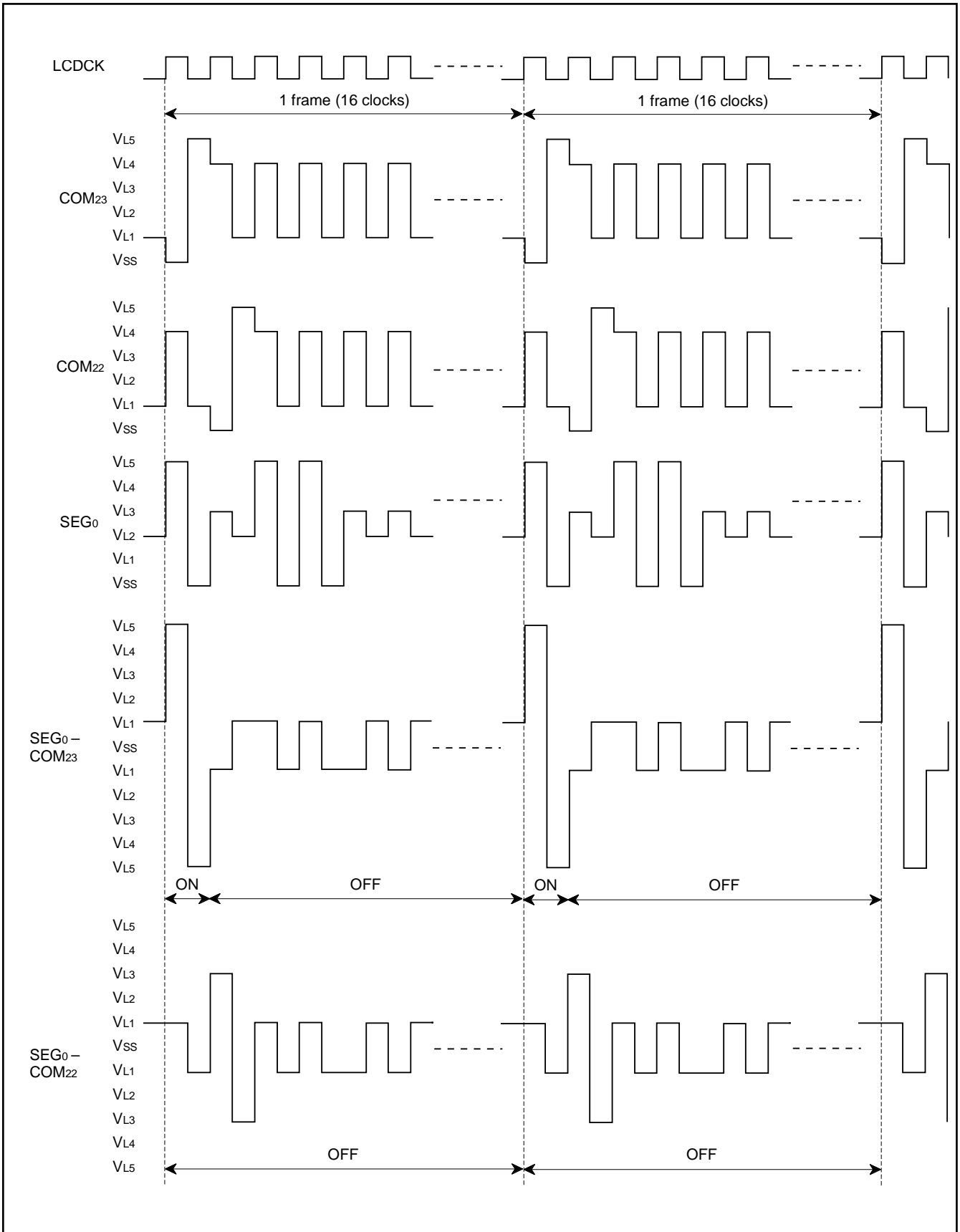


Fig. 31 LCD drive waveform (1/16 duty ratio, 1/5 bias, A type)

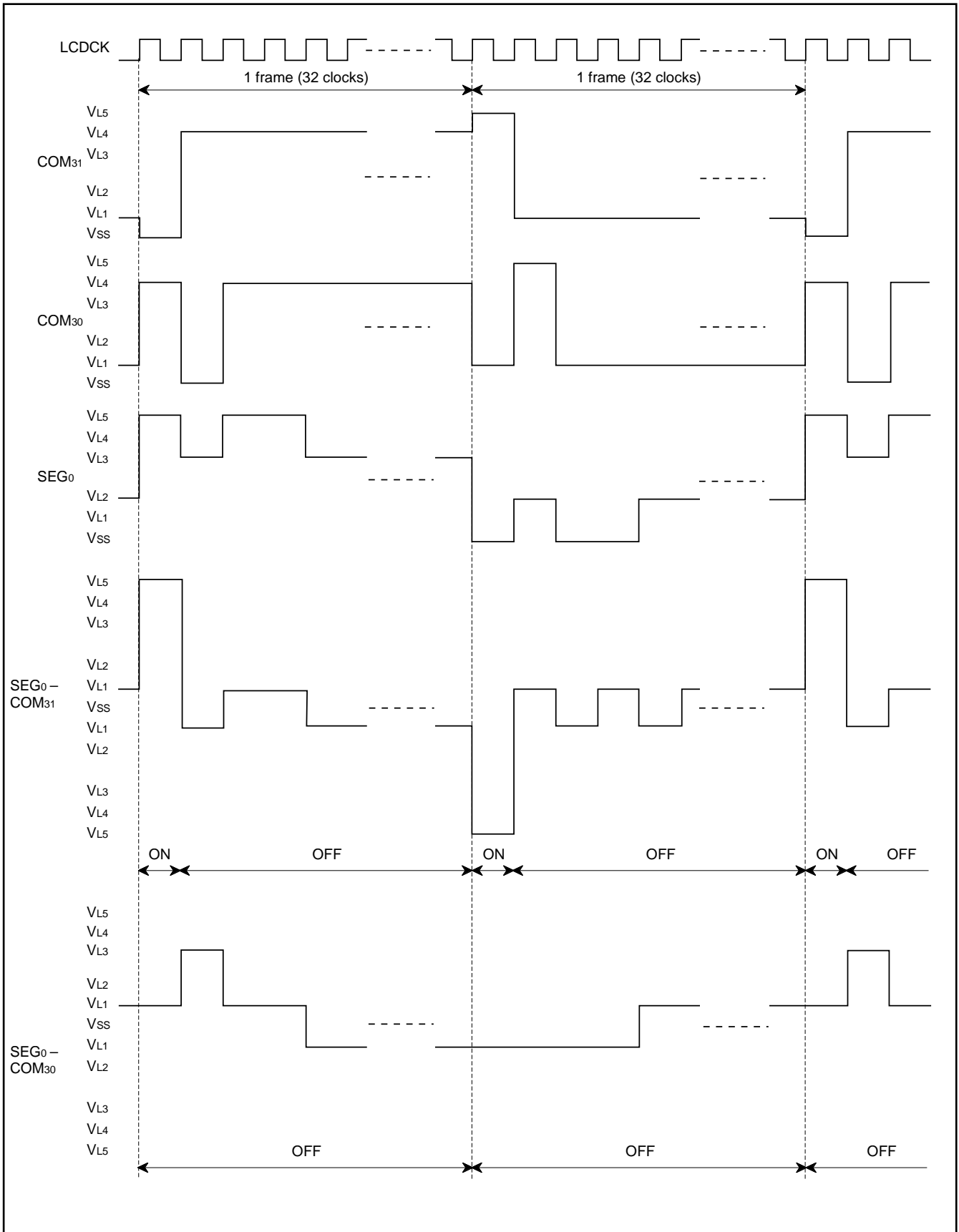


Fig. 32 LCD drive waveform (1/32 duty ratio, 1/7 bias, B type)

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between V_{CC} (min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD₁₆ (high-order byte) and address FFFC₁₆ (low-order byte). Make sure that the reset input voltage is less than 0.2V_{CC} when a power source voltage passes V_{CC} (min.).

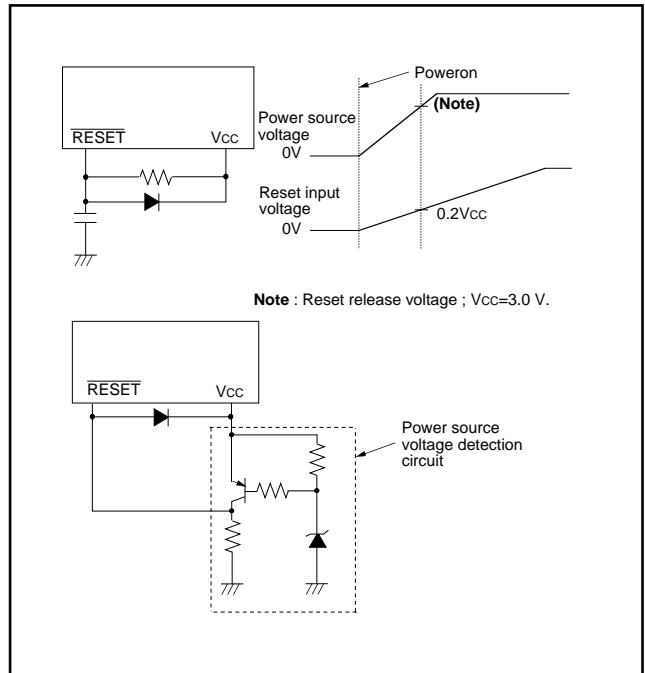


Fig. 33 Reset circuit example

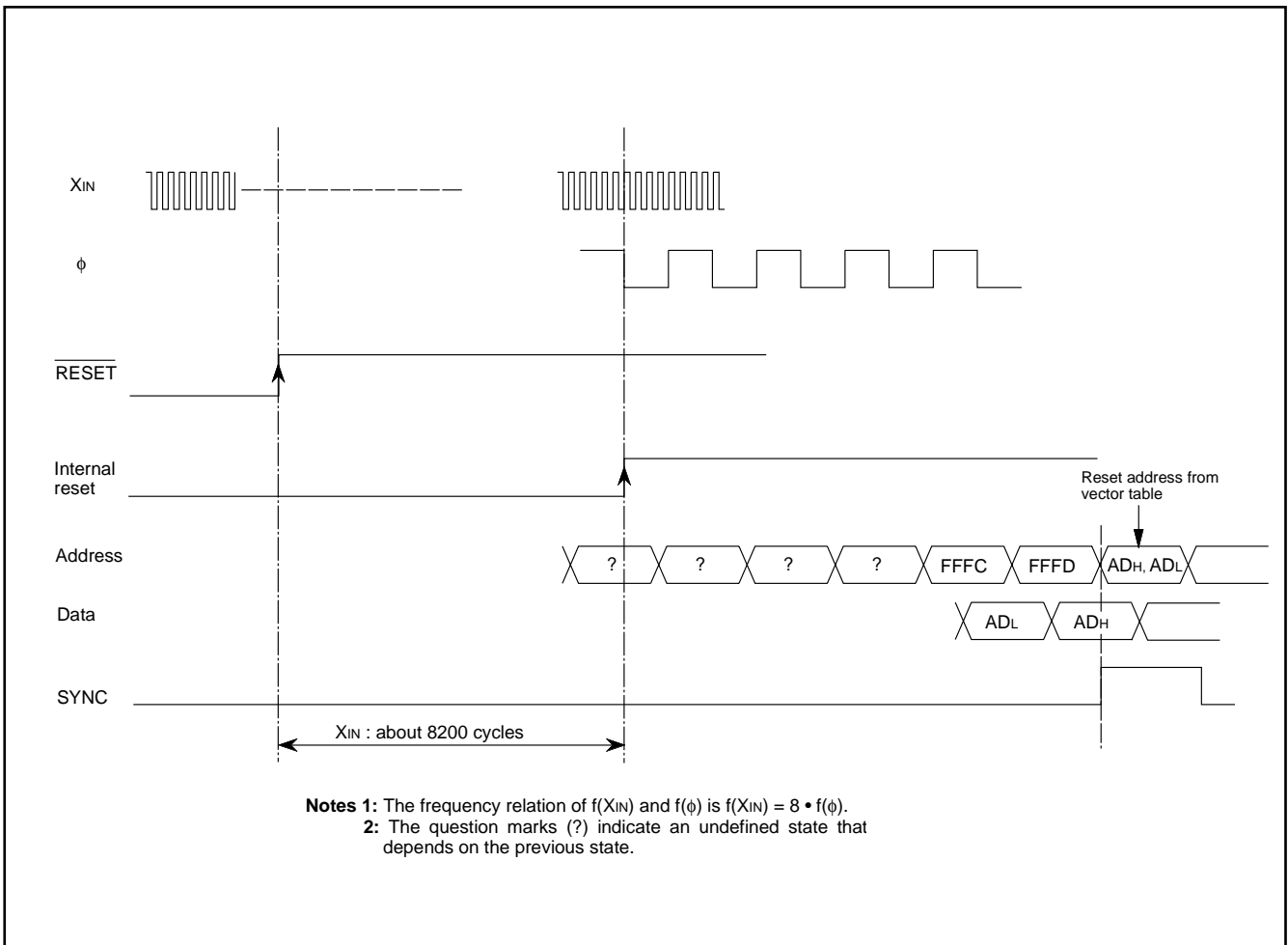


Fig. 34 Reset sequence

	Address	Register contents		Address	Register contents
(1) Port P0 direction register	0001 ₁₆	00 ₁₆	(21) A-D control register	0031 ₁₆	08 ₁₆
(2) Port P1 direction register	0003 ₁₆	00 ₁₆	(22) A-D conversion register (low-order)	0032 ₁₆	XX ₁₆
(3) Port P2 direction register	0005 ₁₆	00 ₁₆	(23) A-D conversion register (high-order)	0033 ₁₆	XX ₁₆
(4) Port P3 direction register	0007 ₁₆	00 ₁₆	(24) LCD control register 1	0037 ₁₆	00 ₁₆
(5) Port P4 direction register	0009 ₁₆	00 ₁₆	(25) LCD control register 2	0038 ₁₆	00 ₁₆
(6) PULL register A	0016 ₁₆	00 ₁₆	(26) LCD mode register	0039 ₁₆	03 ₁₆
(7) PULL register B	0017 ₁₆	00 ₁₆	(27) Interrupt edge selection register	003A ₁₆	00 ₁₆
(8) Serial I/O status register	0019 ₁₆	80 ₁₆	(28) CPU mode register	003B ₁₆	4C ₁₆
(9) Serial I/O control register	001A ₁₆	00 ₁₆	(29) Interrupt request register 1	003C ₁₆	00 ₁₆
(10) UART control register	001B ₁₆	E0 ₁₆	(30) Interrupt request register 2	003D ₁₆	00 ₁₆
(11) Timer X (low-order)	0020 ₁₆	FF ₁₆	(31) Interrupt control register 1	003E ₁₆	00 ₁₆
(12) Timer X (high-order)	0021 ₁₆	FF ₁₆	(32) Interrupt control register 2	003F ₁₆	00 ₁₆
(13) Timer Y (low-order)	0022 ₁₆	FF ₁₆	(33) Processor status register	(PS)	X X X X X 1 X X
(14) Timer Y (high-order)	0023 ₁₆	FF ₁₆	(34) Program counter	(PC _H)	Contents of address FFFD ₁₆
(15) Timer 1	0024 ₁₆	FF ₁₆		(PC _L)	Contents of address FFFC ₁₆
(16) Timer 2	0025 ₁₆	01 ₁₆			
(17) Timer 3	0026 ₁₆	FF ₁₆			
(18) Timer X mode register	0027 ₁₆	00 ₁₆			
(19) Timer Y mode register	0028 ₁₆	00 ₁₆			
(20) Timer 123 mode register	0029 ₁₆	00 ₁₆			

Note: The contents of all other register and RAM are undefined after reset, so they must be initialized by software.
 X : Undefined

Fig. 35 Internal status at reset

CLOCK GENERATING CIRCUIT

The 38C8 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). RC oscillation is available for XIN-XOUT. Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins go to high impedance state.

Main Clock

An oscillation circuit by a resonator can be formed by setting the OSCSEL pin is set to "L" level and connecting a resonator between XIN and XOUT. Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. To supply a clock signal externally, make the XOUT pin open in the "L" level state of the OSCSEL pin, and supply the clock from the XIN pin. The RC oscillation circuit can be formed by setting the OSCSEL pin to "H" level and connecting a resistor between the XIN pin and the XOUT pin. At this time, the feed-back resistor is cut off. The frequency of the RC oscillation changes owing to a parasitic capacitance or the wiring length etc. of the printed circuit board. Do not use the RC oscillation in the usage which the frequency accuracy of the main clock is needed.

Sub-clock

Connect a resonator between XCIN and XCOUT. An external feed-back resistor is needed between XCIN and XCOUT since a feed-back resistor does not exist on-chip. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Frequency Control

(1) Middle-speed Mode

The internal clock ϕ is the frequency of XIN divided by 8. At reset, this mode is selected.

(2) High-speed Mode

The internal clock ϕ is the frequency of XIN divided by 2.

(3) Low-speed Mode

The internal clock ϕ is the frequency of XCIN divided by 2. A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

■Notes on clock generating circuit

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(XIN) > 3 \cdot f(XCIN)$.

Oscillation Control

(1) Stop Mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116."

Either XIN divided by 16 or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits except bit 4 of the timer 123 mode register are cleared to "0." Set the interrupt enable bits of timer 1 and timer 2 to disabled ("0") before executing the STP instruction.

Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

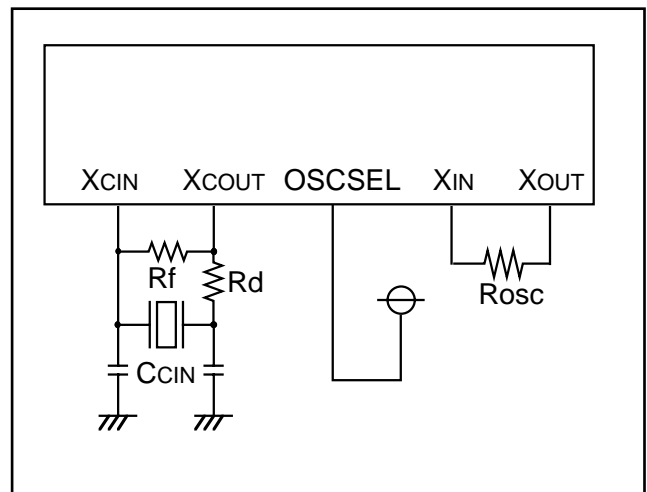


Fig. 36 RC oscillation circuit

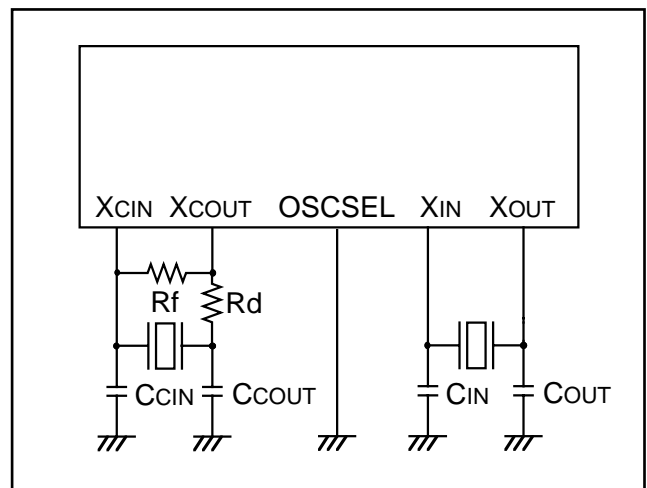


Fig. 37 Resonator circuit

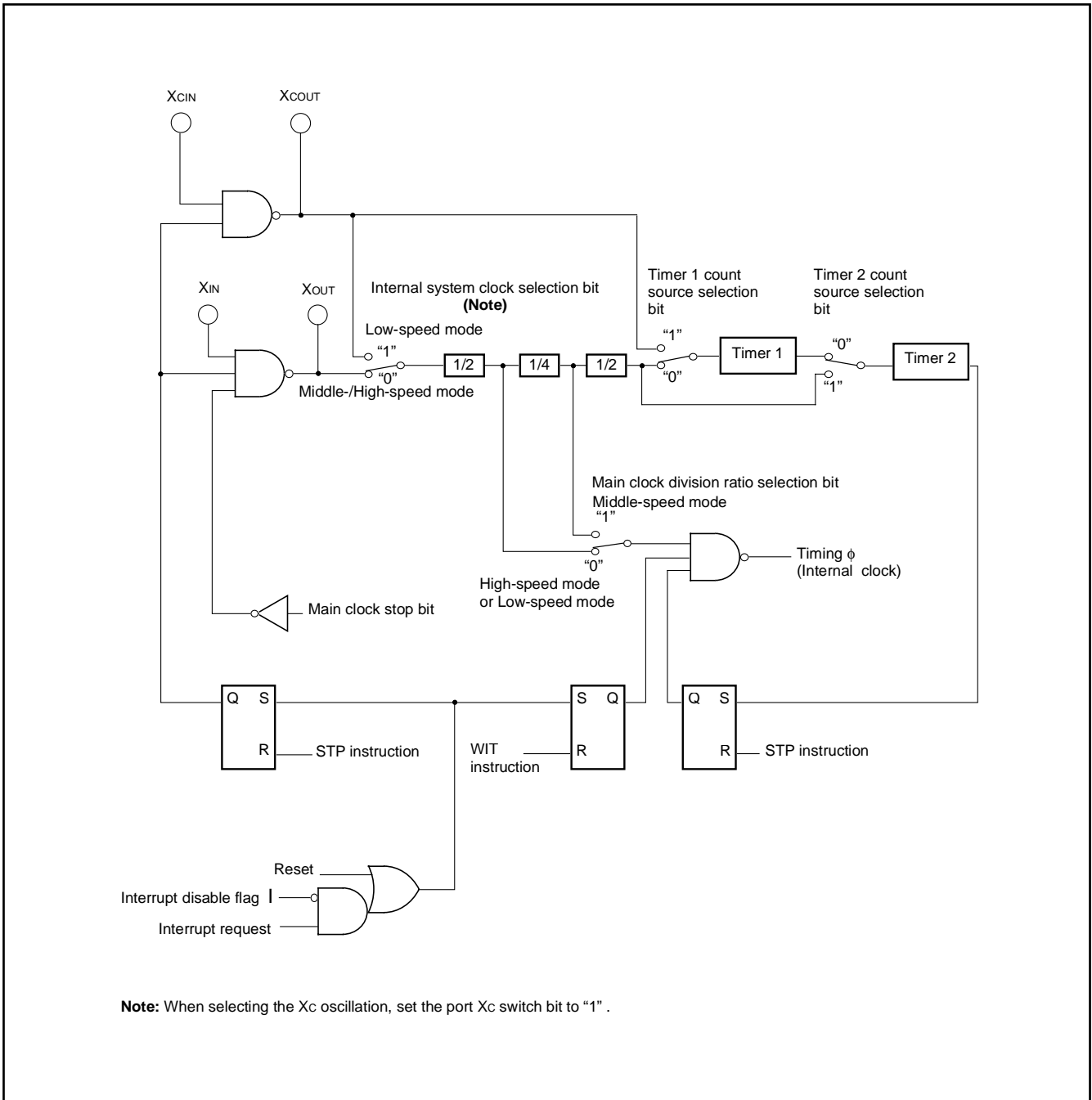
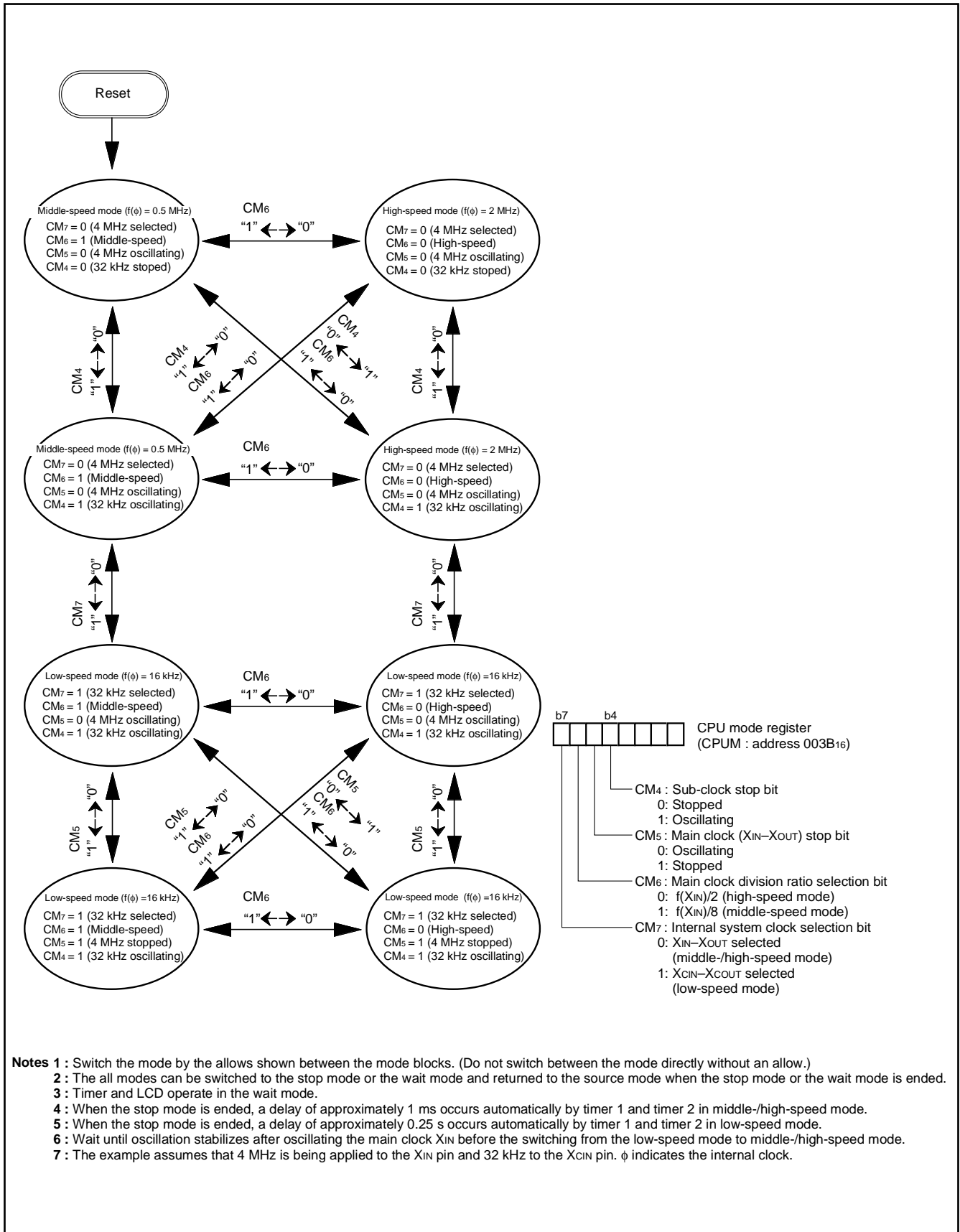


Fig. 38 Clock generating circuit block diagram



- Notes**
- 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
 - 2 : The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wait mode is ended.
 - 3 : Timer and LCD operate in the wait mode.
 - 4 : When the stop mode is ended, a delay of approximately 1 ms occurs automatically by timer 1 and timer 2 in middle-/high-speed mode.
 - 5 : When the stop mode is ended, a delay of approximately 0.25 s occurs automatically by timer 1 and timer 2 in low-speed mode.
 - 6 : Wait until oscillation stabilizes after oscillating the main clock X_{IN} before the switching from the low-speed mode to middle-/high-speed mode.
 - 7 : The example assumes that 4 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. ϕ indicates the internal clock.

Fig. 39 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1," then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A-D Converter

The comparator is constructed linked to a capacitor. When the conversion speed is not enough, the conversion accuracy might be ruined by the disappearance of the charge. When A-D conversion is performed in the middle-speed mode or the high-speed mode, set $f(\text{XIN})$ to at least 500 kHz.

Do not execute the STP or WIT instruction during an A-D conversion because a normal conversion result is not obtained.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency.

At STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

LCD Control

When using the voltage multiplier, apply prescribed voltage to the VLIN pin in the state in which the LCD enable bit is "0", and set the voltage multiplier enable bit to "1".

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form*¹
2. Mark Specification Form*²
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage.

*1 Mask ROM Confirmation Forms

<http://www.infocom.mesc.co.jp/38000/38ordere.htm>

*2 Mark Specification Forms

<http://www.infocom.mesc.co.jp/mela/markform.htm>

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter (PCA7447FP).

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 40 is recommended to verify programming.

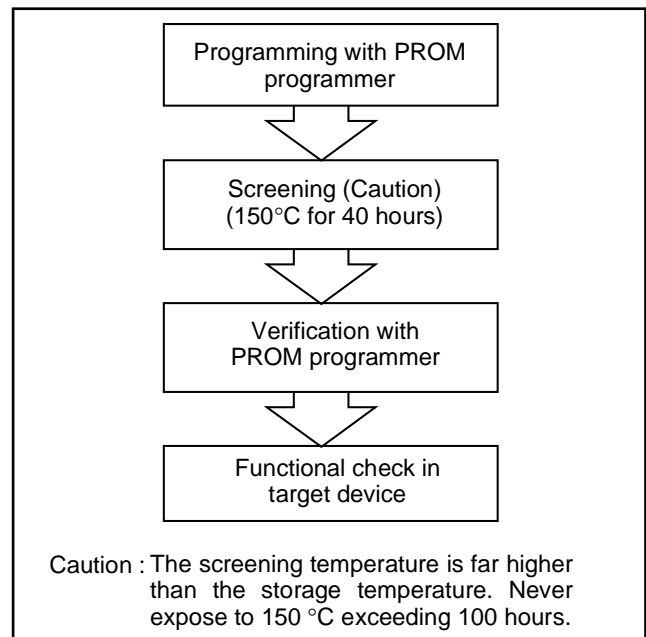


Fig. 40 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Table 10 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage		-0.3 to 7.0	V
V _I	Input voltage P00-P07, P10-P17, P20-P27, P30-P33, P40-P47	All voltages are based on V _{SS} . Output transistors are cut off.	-0.3 to V _{CC} +0.3	V
V _I	Input voltage C1, C2		-0.3 to 7.0	V
V _I	Input voltage RESET, X _{IN} , X _{CIN}		-0.3 to V _{CC} +0.3	V
V _I	Input voltage V _{LIN}	When voltage multiplier is not operated.	-0.3 to 7.0	V
V _I	Input voltage V _{L1} , V _{L2} , V _{L3} , V _{L4} , V _{L5}	V _{L1} ≤ V _{L2} ≤ V _{L3} ≤ V _{L4} ≤ V _{L5}	-0.3 to 7.0	V
V _O	Output voltage P00-P07, P10-P17, P20-P27, P30-P33, P41-P47		-0.3 to V _{CC} +0.3	V
V _O	Output voltage C1, C2, C3		-0.3 to 7.0	V
V _O	Output voltage COM0-COM31, SEG0-SEG67		-0.3 to V _{L5} +0.3	V
V _O	Output voltage X _{OUT} , X _{COU} T		-0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		-20 to 85	°C
T _{stg}	Storage temperature		-40 to 125	°C

Table 11 Recommended operating conditions (V_{CC} = 2.2 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Power source voltage	High-speed mode f(X _{IN}) ≤ 8 MHz	4.0	5.0	5.5	V
		High-speed mode f(X _{IN}) ≤ 4 MHz	3.0	5.0	5.5	V
		Middle-speed mode f(X _{IN}) ≤ 8 MHz	2.7	5.0	5.5	V
		Middle-speed mode (mask ROM version) f(X _{IN}) ≤ 4 MHz	2.2	5.0	5.5	V
		Middle-speed mode (One Time PROM version) f(X _{IN}) ≤ 4 MHz	2.5	5.0	5.5	V
		Low-speed mode (mask ROM version)	2.2	5.0	5.5	V
		Low-speed mode (One Time PROM version)	2.5	5.0	5.5	V
V _{SS}	Power source voltage		0		V	
V _{LIN}	Power source voltage	V _{LIN}			2.33	V
V _{L5}	Power source voltage	V _{L5}			7.0	V
V _{IA}	Analog input voltage	AN0-AN7	V _{SS}		V _{CC}	V
V _{IH}	"H" input voltage	P00-P07, P10-P17, P40, P43, P45, P47	0.7V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	P20-P27, P30-P33, P41, P42, P44, P46	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	RESET	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	X _{IN}	0.8V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage	P00-P07, P10-P17, P40, P43, P45, P47	V _{SS}		0.3V _{CC}	V
V _{IL}	"L" input voltage	P20-P27, P30-P33, P41, P42, P44, P46	V _{SS}		0.2V _{CC}	V
V _{IL}	"L" input voltage	RESET	V _{SS}		0.2V _{CC}	V
V _{IL}	"L" input voltage	X _{IN}	V _{SS}		0.2V _{CC}	V
ΣI _{OH(peak)}	"H" total peak output current	All ports (Note 1)			-60.0	mA
ΣI _{OL(peak)}	"L" total peak output current	All ports (Note 1)			60.0	mA
ΣI _{OH(avg)}	"H" total average output current	All ports (Note 2)			-30.0	mA
ΣI _{OL(avg)}	"L" total average output current	All ports (Note 2)			30.0	mA
I _{OH(peak)}	"H" peak output current	All ports (Note 3)			-5.0	mA
I _{OL(peak)}	"L" peak output current	All ports (Note 3)			10.0	mA
I _{OH(avg)}	"H" average output current	All ports (Note 4)			-2.5	mA
I _{OL(avg)}	"L" average output current	All ports (Note 4)			5.0	mA
ROSC	Oscillation resistor at selecting RC oscillation		5	8.2	10	kΩ

Notes 1: The total peak output current is the peak value of the peak currents flowing through all the applicable ports.

2: The total average output current is the average value measured over 100 ms flowing through all the applicable ports.

3: The peak output current is the peak current flowing in each port.

4: The average output current is an average value measured over 100 ms.

Table 12 Recommended operating conditions (mask ROM version) ($V_{CC} = 2.2$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR ₀) f(CNTR ₁)	Timer X, timer Y input frequency (duty cycle 50%)				f(X _{IN})/2	MHz
f(X _{IN})	Main clock input oscillation frequency (Note 1)	High-speed mode ($4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)			8.0	MHz
		High-speed mode ($2.2\text{ V} \leq V_{CC} < 4.0\text{ V}$)			($20 \times V_{CC} - 8$)/13	MHz
		Middle-speed mode ($2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)			8.0	MHz
f(X _{CIN})	Sub-clock input oscillation frequency (Notes 1, 2)		32.768		50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50 %.

2: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 13 Recommended operating conditions (PROM version) ($V_{CC} = 2.5$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR ₀) f(CNTR ₁)	Timer X, timer Y input frequency (duty cycle 50%)				f(X _{IN})/2	MHz
f(X _{IN})	Main clock input oscillation frequency (Note 1)	High-speed mode ($4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)			8.0	MHz
		High-speed mode ($2.5\text{ V} \leq V_{CC} < 4.0\text{ V}$)			$4 \times V_{CC} - 8$	MHz
		Middle-speed mode ($2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)			8.0	MHz
f(X _{CIN})	Sub-clock input oscillation frequency (Notes 1, 2)		32.768		50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50 %.

2: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 14 Electrical characteristics ($V_{CC} = 2.2$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P17, P30-P33	IOH = -5.0 mA VCC = 5.0 V	VCC-2.0			V
		IOH = -1.5 mA VCC = 5.0 V	VCC-0.5			V
		IOH = -1.25 mA VCC = 2.2 V	VCC-1.0			V
VOH	"H" output voltage P20-P27, P41-P47	IOH = -5.0 mA VCC = 5.0 V	VCC-2.0			V
		IOH = -1.5 mA VCC = 5.0 V	VCC-0.5			V
		IOH = -1.25 mA VCC = 2.2 V	VCC-1.0			V
VOL	"L" output voltage P00-P07, P10-P17, P30-P33	IOL = 5.0 mA VCC = 5.0 V			2.0	V
		IOL = 1.5 mA VCC = 5.0 V			0.5	V
		IOL = 1.25 mA VCC = 2.2 V			1.0	V
VOL	"L" output voltage P20-P27, P41-P47	IOL = 5.0 mA VCC = 5.0 V			2.0	V
		IOL = 1.5 mA VCC = 5.0 V			0.5	V
		IOL = 1.25 mA VCC = 2.2 V			1.0	V
VT+–VT-	Hysteresis INT0, INT1, ADT, CNTR0, CNTR1, P20–P27		0.5			V
VT+–VT-	Hysteresis SCLK, RxD		0.5			V
VT+–VT-	Hysteresis RESET		0.5			V
I _{IH}	"H" input current All ports				5.0	μA
I _{IH}	"H" input current RESET				5.0	μA
I _{IH}	"H" input current XIN		4.0			μA
I _{IL}	"L" input current All ports	VI = VSS Pull-ups "off"			-5.0	μA
		VCC = 5.0 V, VI = VCC Pull-ups "on"	-60.0	-120.0	-240.0	μA
		VCC = 2.2 V, VI = VCC Pull-ups "on"	-5.0	-20.0	-40.0	μA
I _{IL}	"L" input current RESET	VI = VSS			-5.0	μA
I _{IL}	"L" input current XIN	VI = VSS		-4.0		μA

Table 15 Electrical characteristics ($V_{CC} = 2.2$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped	2.0	5.0	5.5	V
I _{CC}	Power source current	High-speed mode, $V_{CC} = 5.0$ V $f(X_{IN}) = 8.0$ MHz $f(X_{CIN}) = 32.768$ kHz		5.5	11.0	mA
		Middle-speed mode, $V_{CC} = 5.0$ V $f(X_{IN}) = 8.0$ MHz $f(X_{CIN}) = 32.768$ kHz		3.0	6.0	mA
		Middle-speed mode, $V_{CC} = 3.0$ V $f(X_{IN}) = 8.0$ MHz $f(X_{CIN}) = 32.768$ kHz		1.0	2.0	mA
		Low-speed mode, $V_{CC} = 3.0$ V, $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32.768$ kHz		20.0	40.0	μA
		High-/Middle-speed mode, $V_{CC} = 5.0$ V, $f(X_{IN}) = 8.0$ MHz (in WIT state) $f(X_{CIN}) = 32.768$ kHz		0.9	1.8	mA
		Middle-speed mode, $V_{CC} = 3.0$ V $f(X_{IN}) = 8.0$ MHz (in WIT state) $f(X_{CIN}) = 32.768$ kHz		0.3	0.6	mA
		Low-speed mode, $V_{CC} = 3.0$ V, $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32.768$ kHz (in WIT state)		4.5	9.0	μA
		All oscillation stopped $T_a = 25^\circ\text{C}$, Output transistors "off" (in STP state)		0.1	1.0	μA
		All oscillation stopped $T_a = 85^\circ\text{C}$, Output transistors "off" (in STP state)			10.0	μA
		I _{AD}	A-D converter current dissipation	Current increase at A-D converter operated, $f(X_{IN}) = 8.0$ MHz		0.8
I _{L5}	V _{L5} input current (Note)	$V_{L5} = 6.0$ V, $T_a = 25^\circ\text{C}$		3	6	μA
FROSC	RC oscillation frequency	$R_{OSC} = 8.2$ k Ω	1.5	2.5	3.5	MHz

Note: When normal drivability (drivability selection bit 1 = "0", drivability selection bit 2 = "0") is selected.

Table 16 A-D converter characteristics

(V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85°C, f(X_{IN}) ≤ 4 MHz, in middle-speed/high-speed mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	V _{CC} = 2.7–5.5 V			±4	LSB
		V _{CC} = 2.5–2.7 V (T _a = -10 to 50 °C)			±6	LSB
t _{conv}	Conversion time	f(X _{IN}) = 4 MHz (Note)	30.5		34	μs
I _{IA}	Analog port input current			0.5	5.0	μA

Note: When main clock is selected as system clock.

Table 17 Timing requirements 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	125			ns
t _{wH} (X _{IN})	Main clock input "H" pulse width	45			ns
t _{wL} (X _{IN})	Main clock input "L" pulse width	40			ns
t _c (CNTR)	CNTR ₀ , CNTR ₁ input cycle time	250			ns
t _{wH} (CNTR)	CNTR ₀ , CNTR ₁ input "H" pulse width	105			ns
t _{wL} (CNTR)	CNTR ₀ , CNTR ₁ input "L" pulse width	105			ns
t _{wH} (INT)	INT ₀ , INT ₁ input "H" pulse width	80			ns
t _{wL} (INT)	INT ₀ , INT ₁ input "L" pulse width	80			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	800			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width (Note)	370			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width (Note)	370			ns
t _{su} (RxD-SCLK)	Serial I/O input setup time	220			ns
t _h (SCLK-RxD)	Serial I/O input hold time	100			ns

Note: When bit 6 of address 001A₁₆ is "1".

Divide this value by four when bit 6 of address 001A₁₆ is "0".

Table 18 Timing requirements 2 (V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	125			ns
t _{wH} (X _{IN})	Main clock input "H" pulse width	45			ns
t _{wL} (X _{IN})	Main clock input "L" pulse width	40			ns
t _c (CNTR)	CNTR ₀ , CNTR ₁ input cycle time	900/(V _{CC} -0.4)			ns
t _{wH} (CNTR)	CNTR ₀ , CNTR ₁ input "H" pulse width	t _c (CNTR)/2-20			ns
t _{wL} (CNTR)	CNTR ₀ , CNTR ₁ input "L" pulse width	t _c (CNTR)/2-20			ns
t _{wH} (INT)	INT ₀ , INT ₁ input "H" pulse width	230			ns
t _{wL} (INT)	INT ₀ , INT ₁ input "L" pulse width	230			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	2000			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width (Note)	950			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width (Note)	950			ns
t _{su} (RxD-SCLK)	Serial I/O input setup time	400			ns
t _h (SCLK-RxD)	Serial I/O input hold time	200			ns

Note: When bit 6 of address 001A₁₆ is "1".

Divide this value by four when bit 6 of address 001A₁₆ is "0".

Table 19 Switching characteristics 1 ($V_{cc} = 4.0$ to 5.5 V, $V_{ss} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{wH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$t_c(\text{SCLK})/2-30$			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$t_c(\text{SCLK})/2-30$			ns
$t_d(\text{SCLK-TxD})$	Serial I/O output delay time (Note 1)			140	ns
$t_v(\text{SCLK-TxD})$	Serial I/O output valid time (Note 1)	-30			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time			30	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time			30	ns
$t_r(\text{CMOS})$	CMOS output rising time (Note 2)		10	30	ns
$t_f(\text{CMOS})$	CMOS output falling time (Note 2)		10	30	ns

Notes 1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".
2: The XOUT and XCOUT pins are excluded.

Table 20 Switching characteristics 2 ($V_{cc} = 2.2$ to 4.0 V, $V_{ss} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{wH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$t_c(\text{SCLK})/2-50$			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$t_c(\text{SCLK})/2-50$			ns
$t_d(\text{SCLK-TxD})$	Serial I/O output delay time (Note 1)			350	ns
$t_v(\text{SCLK-TxD})$	Serial I/O output valid time (Note 1)	-30			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time			50	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time			50	ns
$t_r(\text{CMOS})$	CMOS output rising time (Note 2)		20	50	ns
$t_f(\text{CMOS})$	CMOS output falling time (Note 2)		20	50	ns

Notes 1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".
2: The XOUT and XCOUT pins are excluded.

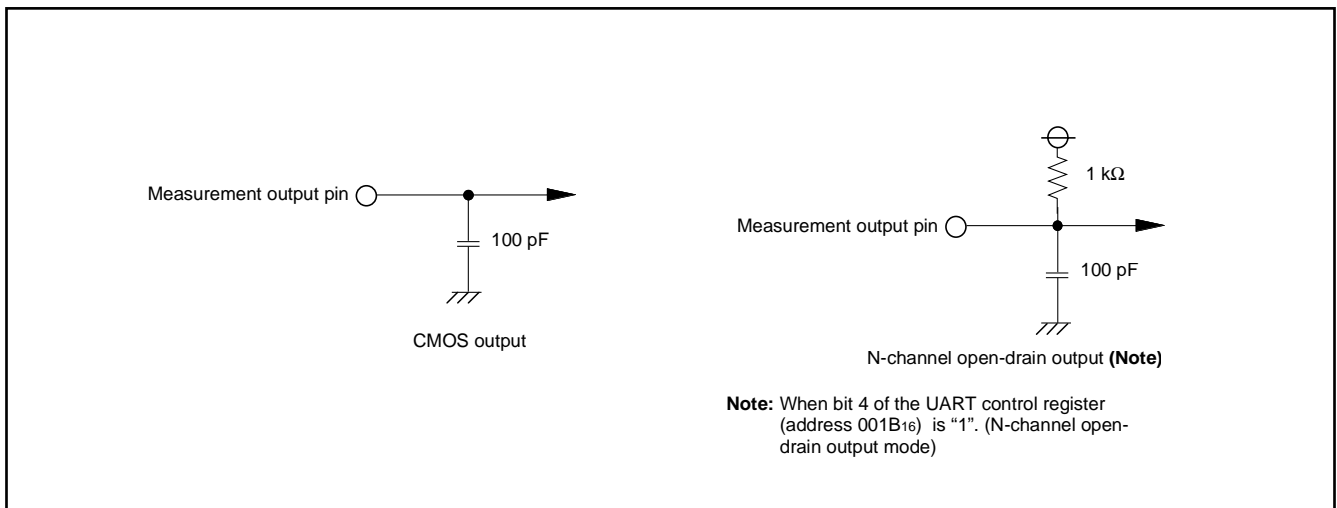


Fig. 41 Circuit for measuring output switching characteristics

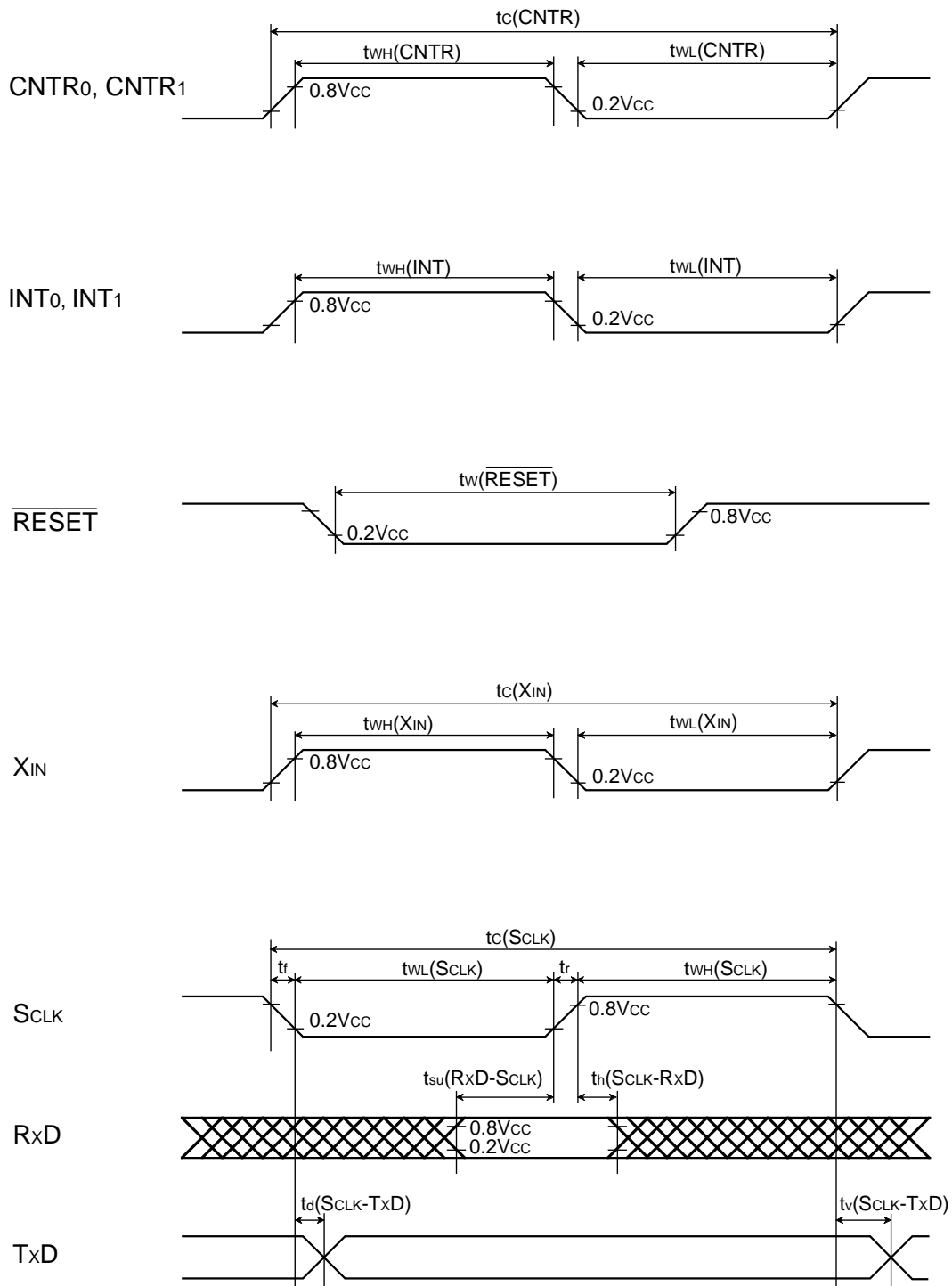


Fig. 42 Timing diagram

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to
 change.

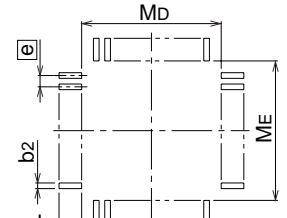
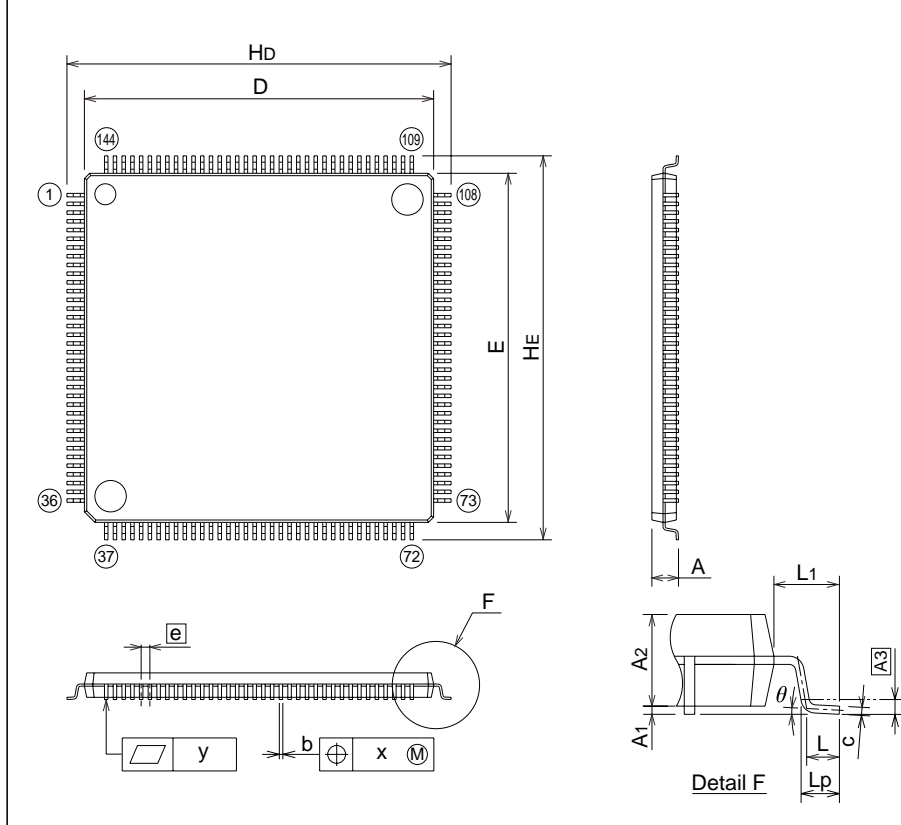
PACKAGE OUTLINE

144P6Q-A

(MMP)

Plastic 144pin 20X20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	-	1.23	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0.05	0.125	0.2
A2	-	1.4	-
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	-	0.5	-
Hd	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
theta	0°	-	8°
b2	-	0.225	-
l2	0.95	-	-
MD	-	20.4	-
ME	-	20.4	-



MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

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