LS100

Quad-Port Ethernet Switch Interface

Features

- Supports both 10 and 100 Mb Ethernet, selectable on a per-port basis
- Cut-through or Store-and-Forward switching, selectable on a per-port basis
- Supports both Half Duplex and Full Duplex, selectable on a per-port basis
- Supports Port Based VLAN
- Supports Half Duplex and Full Duplex Flow Control
- Multicast bus for efficient multicast support
- Integrated port statistics collection
- Integrated 64 entry address translation cache
- Integrated PCI bus interface for port management
- Integrated memory controller and buffer manager
- 0.5 micron, 3.3V CMOS technology
- 256 Pin Plastic Quad Flat Pack or Ball Grid Array
- JTAG for boundary scan testing

Description

The LS100 is a highly integrated quad port interface for 10 and 100 Mbit Ethernet switching. It integrates MAC Controllers, memory control and buffer management, and address translation logic. When combined with the LS101 25 port switch, the LS100 provides a low cost scalable switched Ethernet solution.

The LS100 supports the 100BASE-TX, 100BASE-T4, 100BASE-FX 100 Mbit Ethernet specifications as well as the 10BASE-T, 10BASE2, 10BASE5 10 Mbit specifications.

Figure 1 gives an overview of the functional blocks that make up the LS100.

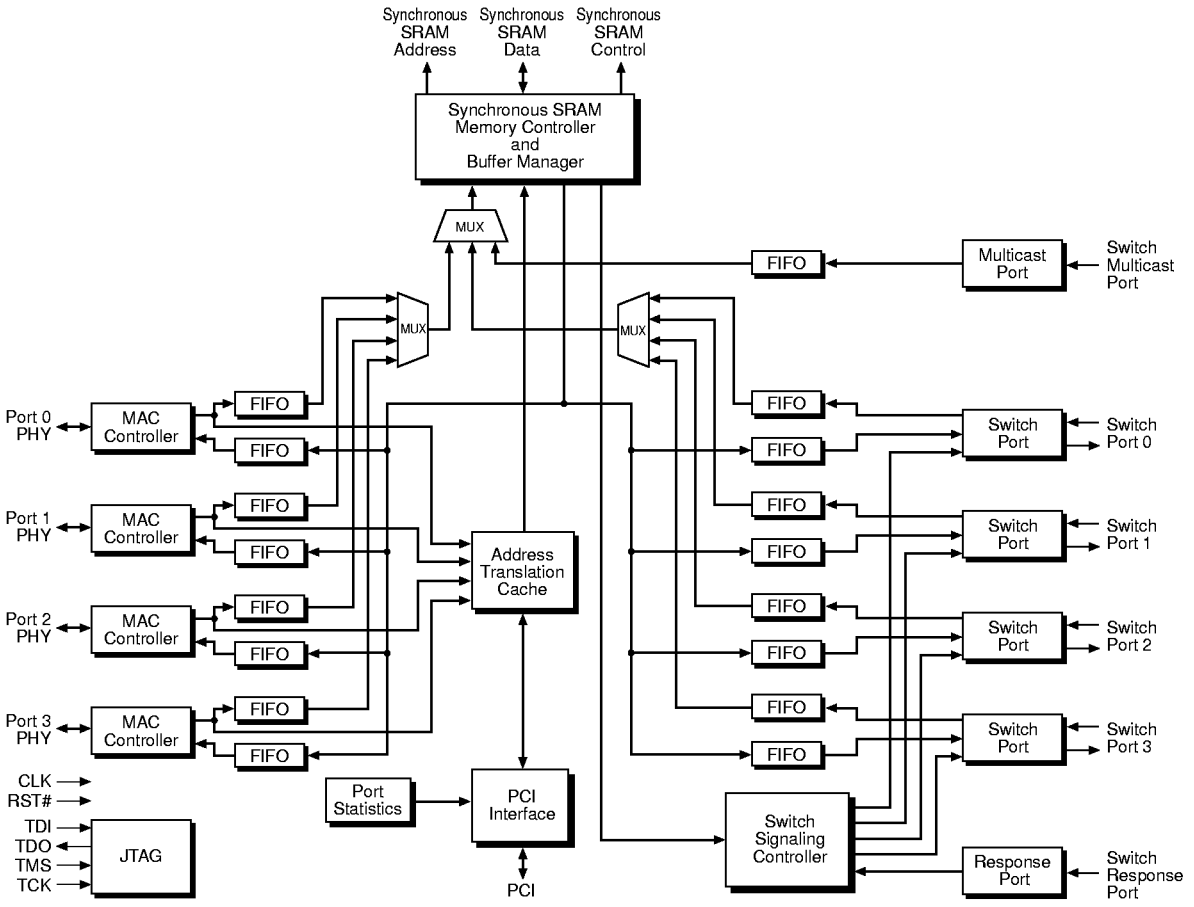


Figure 1: LS100 Functional Block Diagram

Introduction

The LS100 is a quad port interface controller for the LS Ethernet SwitchSet™. When combined with other members of the LS family it provides the backbone of a scalable, non-blocking, switching architecture. The key to these features lies in the use of I-Cube's PSID™ crossbar technology for the switch fabric. Twenty five non-blocking port count at 100 Mb is currently supported, with port counts in the hundreds achievable.

Figure 2 shows how the LS100 and LS101 twenty five port LAN switching element can be combined to create a scalable workgroup switching hub. Variations of this architecture can be used for backbone and stackable switch applications.

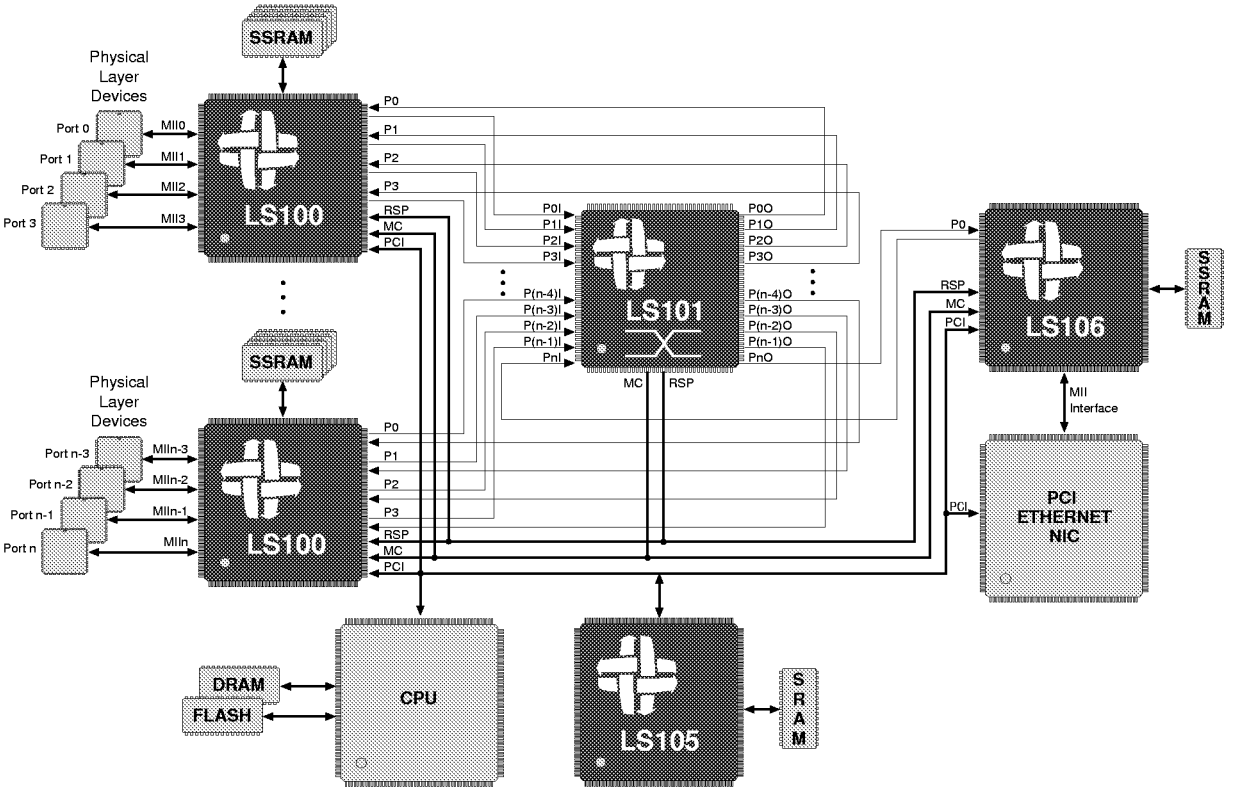


Figure 2: LS Based Workgroup Switch

The port interface logic required for four ports consists of an LS100, 1 to 16 Mb of synchronous SRAM memory buffers and four physical layer devices. Each port interface has a dedicated full duplex connection to the LS101 switching element. Port interfaces may establish connections through the switch to other port interfaces by sending requests to the switch. These requests are in the form of in-band signaling packets. Cases where more than one port interface wants to forward a packet to the same port are handled by arbitration logic within the switching element.

Switch management functions are handled by a CPU and an optional standard Ethernet network interface controller, NIC. The CPU, the NIC and the port interfaces are connected via a PCI management bus. This bus is used to transfer management packets between the CPU and the NIC. The CPU also uses it to access control registers located in the LS100s and the NIC.

LS100 Functional Blocks

The primary functional blocks that make up the LS100 are:

- Media Access and Control (MAC) Controllers
- Address Translation Cache (ATC)
- Memory Controller and Buffer Manager
- Port Statistics
- PCI Interface
- Switch Ports & Switch Signaling Controller
- Switch Multicast Port
- Switch Response Port
- JTAG

MAC Controllers

The MAC Controller blocks perform all Media Access and Control functions for both 100 Mb and 10 Mb Ethernet. Functions performed by this block include: CRC checking, CSMA/CD protocol handling, source and destination address capture, and frame delineation. The LS100 supports an MII, IEEE 802.3u Media Independent Interface, interface from the MAC controllers to external physical layer devices.

Address Translation Cache

The purpose of the Address Translation Cache is to perform high speed address mapping and checking of source and destination addresses of incoming packets. The ATC performs the following functions:

- Source address checking
- Destination address mapping
- Multicast address filtering
- LRU based entry replacement

Memory Controller and Buffer Manager

The memory controller generates all timing and control signals for one to 16 Mb of burst synchronous SRAMs (SSRAM). This SSRAM provides input and output queue memory for all four ports. Access to buffer memory is allocated the port data streams in a time division multiplexed (TDM) manner. FIFOs on the switch ports and MAC controllers smooth intermittent TDM bandwidth provided by the memory controller into continuous flows.

The buffer manager handles all of the address generation required to implement the port queues. Separate input and output queues are provided for each port. In addition there is a separate queue to buffer multicast traffic arriving from the multicast bus.

Port Statistics

Port statistics registers track all port data required to implement MIB-II functionality. In addition there is a complete set of registers for RMON performance monitoring on any port.

PCI Interface

The LS100 includes a 32 bit, target only, PCI interface compatible with Revision 2.1 of the PCI SIG specification. The PCI interface is used to access internal status and control registers for functions such as:

- Device configuration
- Collection of port statistics
- Handling address translation cache misses

Switch Ports & Switch Signaling Controller

Switch Ports connect the LS100 to the external LS switching element. Each switch port consists of a full duplex interface with two bits each for transmit and receive. A 4B5B encoding scheme is used for data between the port interfaces and the switch. Each switch interface supports from a 62.5 MHz to 65.0 MHz clock rate, giving 125 Mb to 130 Mb full duplex switch bandwidth.

The Switch Signaling Controller handles negotiation for switch connections with the switching element. This includes the generation of signaling command packets and the interpretation of response packets that are returned to the LS100 via the response port.

Switch Multicast Port

The multicast port is an input port that accepts broadcast and multicast packets from the multicast bus. The multicast ports of all LS100 devices in a switch are tied together to the multicast port on the switching element.

Switch Response Port

The response port is an input port that accepts signaling response packets from the response bus. The response ports of all LS100 devices in a switch are tied together to the response port on the switching element.

JTAG Controller

The LS100 supports the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing.

Pin Description

Pin Name	Type	Description
P0_TXEN	Output	Port 0 MII transmit enable signal
P0_TXCLK	Input	Port 0 MII transmit clock
P0_TXD[3:0]	Output	Port 0 MII transmit data
P0_COL	Bidirectional	Port 0 MII collision indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
P0_RXER	Input	Port 0 MII receive error signal
P0_RXDV	Input	Port 0 MII receive data valid signal
P0_RXCLK	Input	Port 0 MII receive clock
P0_RXD[3:0]	Input	Port 0 MII receive data
P0_CRS	Bidirectional	Port 0 MII carrier sense indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
P1_TXEN	Output	Port 1 MII transmit enable signal
P1_TXCLK	Input	Port 1 MII transmit clock
P1_TXD[3:0]	Output	Port 1 MII transmit data
P1_COL	Bidirectional	Port 1 MII collision indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
P1_RXER	Input	Port 1 MII receive error signal
P1_RXDV	Input	Port 1 MII receive data valid signal
P1_RXCLK	Input	Port 1 MII receive clock
P1_RXD[3:0]	Input	Port 1 MII receive data
P1_CRS	Bidirectional	Port 1 MII carrier sense indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
P2_TXEN	Output	Port 2 MII transmit enable signal
P2_TXCLK	Input	Port 2 MII transmit clock
P2_TXD[3:0]	Output	Port 2 MII transmit data
P2_COL	Bidirectional	Port 2 MII collision indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
P2_RXER	Input	Port 2 MII receive error signal
P2_RXDV	Input	Port 2 MII receive data valid signal
P2_RXCLK	Input	Port 2 MII receive clock
P2_RXD[3:0]	Input	Port 2 MII receive data
P2_CRS	Bidirectional	Port 2 MII carrier sense indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
P3_TXEN	Output	Port 3 MII transmit enable signal
P3_TXCLK	Input	Port 3 MII transmit clock
P3_TXD[3:0]	Output	Port 3 MII transmit data
P3_COL	Bidirectional	Port 3 MII collision indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
P3_RXER	Input	Port 3 MII receive error signal
P3_RXDV	Input	Port 3 MII receive data valid signal
P3_RXCLK	Input	Port 3 MII receive clock
P3_RXD[3:0]	Input	Port 3 MII receive data
P3_CRS	Bidirectional	Port 3 MII carrier sense indicator PHY mode: input NIC mode: output When in NIC mode, half duplex not supported
MDC	Output	MII management clock (master mode)
MDIO	Bi-directional	MII data input/output (master mode)

Table 1: Physical Interface Pin Description

All physical interface pin pads have internal pull down resistors.

Pin Name	Type	Description
M_CLK	Output	Memory clock Internal pull-up resistor
M_A[16:1]	Output	Memory address bus Internal pull-down resistor
M_DATA[31:0]	Bidirectional	Memory data bus Internal pull-down resistor
M_ADS[3:0]#	Output	Memory start of cycle device strobes Internal pull-up resistor
M_ADV[3:0]#	Output	Memory address advance device strobes Internal pull-up resistor
M_OE[3:0]#	Output	Memory output enable device strobes Internal pull-up resistor
M_GW[3:0]#	Output	Memory global write device strobes Internal pull-up resistor

Table 2: Memory Interface Pin Description

Pin Name	Type	Description
PCI_AD[31:0]	Bidirectional	PCI multiplexed address data bus
PCI_CBE[3:0]	Input	PCI bus command and byte enables
PCI_PAR	Bidirectional	PCI parity signal
PCI_FRAME#	Input	PCI frame signal
PCI_TRDY#	Output	PCI target ready signal
PCI_IRDY#	Input	PCI initiator ready
PCI_STOP#	Output	PCI transaction stop signal
PCI_DEVSEL#	Output	PCI device select signal
PCI_IDSEL#	Input	PCI initialization device select
PCI_CLK	Input	PCI clock
PCI_RST#	Input	PCI reset Schmitt non-inverting receiver
PCI_INTA#	Open Drain	PCI interrupt request A/Management exception
ATC_MISS#	Open Drain	PCI ATC miss exception

Table 3: PCI Interface Pin Description

Pin Name	Type	Description
MC[1:0]	Input	Multicast bus port
RSP[3:0]	Input	Switch command response port
P0_I[1:0]	Input	Port 0 input from switch Internal pull-up resistor
P0_O[1:0]	Output	Port 0 output to switch Internal pull-up resistor
P1_I[1:0]	Input	Port 1 input from switch Internal pull-up resistor
P1_O[1:0]	Output	Port 1 output to switch Internal pull-up resistor
P2_I[1:0]	Input	Port 2 input from switch Internal pull-up resistor
P2_O[1:0]	Output	Port 2 output to switch Internal pull-up resistor
P3_I[1:0]	Input	Port 3 input from switch Internal pull-up resistor
P3_O[1:0]	Output	Port 3 output to switch Internal pull-up resistor
CLK	Input	Switch data clock Internal pull-down resistor

Table 4: Switch Interface Pin Description

Pin Name	Type	Description
TCK	Input	JTAG Test clock Internal pull-down resistor
TDI	Input	JTAG Test Data In Internal pull-down resistor
TDO	Output	JTAG Test Data Out Tristate output
TMS	Input	JTAG Test Mode Select Internal pull-down resistor

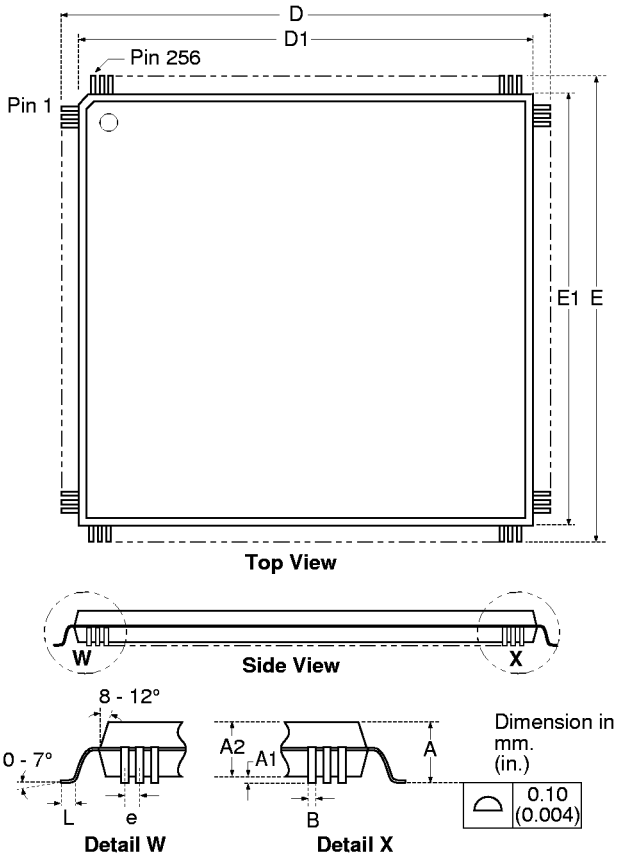
Table 5: JTAG Interface Pin Description

Pin Name	Type	Description
DV_{DD}	Power	+3.3V Power for the CoreBypass capacitors should be evenly distributed. DV_{DD} and Ov_{DD} are connected internally in the device.
DV_{SS}	Ground	Ground for the CoreDVss and Ovss are connected internally in the device.
OV_{DD}	Power	+3.3V Power for the I/OBypass capacitors should be evenly distributed. DV_{DD} and Ov_{DD} are connected internally in the device.
OV_{SS}	Ground	Ground for the I/ODV_{SS} and Ov_{SS} are connected internally in the device.

Table 6: Power Interface

Mechanical Specifications

PQ256 Package Dimensions



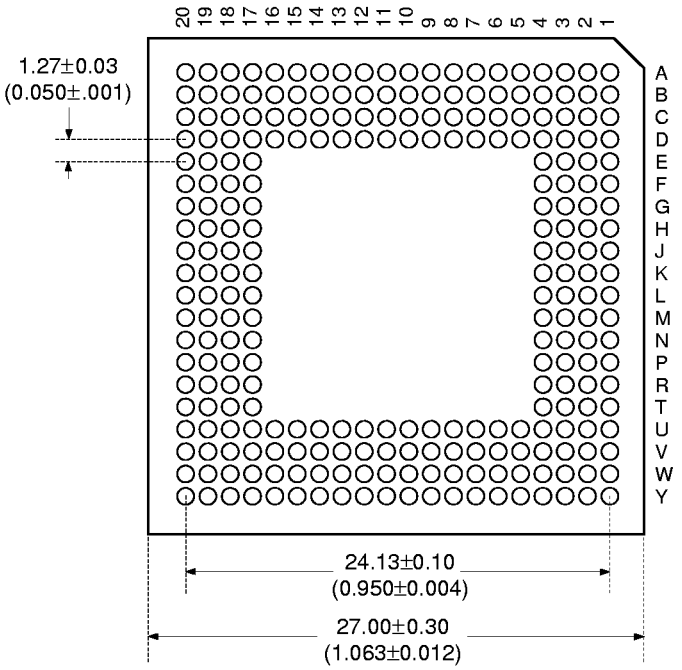
Package Dimension Table		PQFP/256L	
		inch	mm
A	max	0.160	4.07
A1	min	0.010	0.25
	max	0.017	0.43
A2	min	0.125	3.17
	max	0.144	3.67
D	min	1.195	30.40
	max	1.215	30.91
D1	min	1.098	27.93
	max	1.106	28.14
E	min	1.195	30.40
	max	1.215	30.91
E1	min	1.098	27.93
	max	1.106	28.14
L	min	0.016	0.40
	max	0.030	0.76
B	min	0.005	0.13
	max	0.009	0.23
e	BSC.	0.01575	0.40

Table 7: PQFP/256L Package Dimensions

Note:

Use "mm" as the controlling dimension.

B256 Balls Package Dimensions



Bottom View (Ball Side)

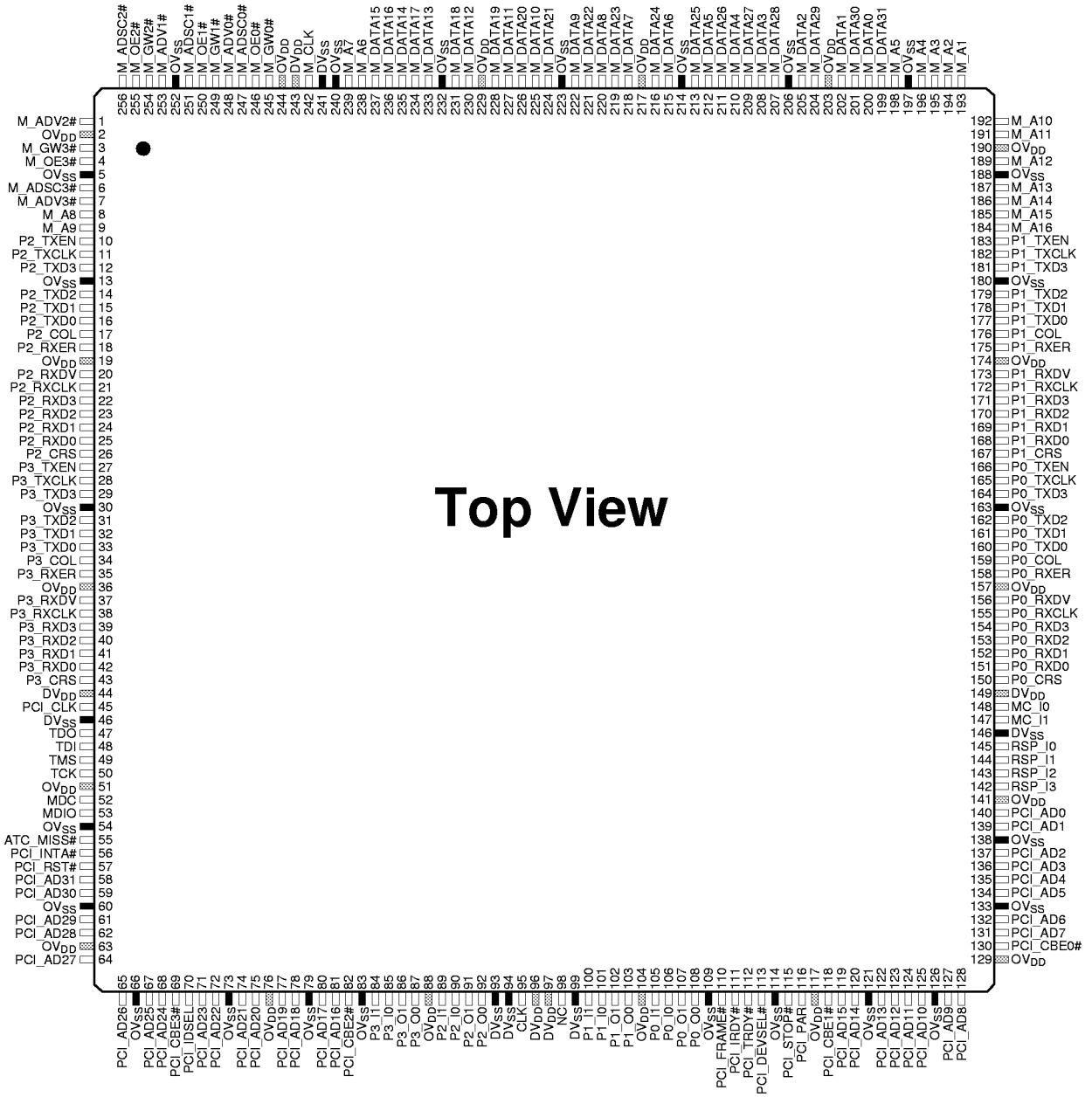
Note:
Dimensions in mm (in.)

Pinout

LS100 [PQFP/256L Package] Pinout

Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#
ATC_MISS#	55	M_DATA12	230	P0_TXD1	161	P3_CRS	43	PCI_AD25	67	OV_{DD}	51
CLK	95	M_DATA13	233	P0_TXD2	162	P3_I0	85	PCI_AD26	65	OV_{DD}	63
MC_I0	148	M_DATA14	235	P0_TXD3	164	P3_I1	84	PCI_AD27	64	OV_{DD}	76
MC_I1	147	M_DATA15	237	P0_TXEN	166	P3_O0	87	PCI_AD28	62	OV_{DD}	88
MDC	52	M_DATA16	236	P1_COL	176	P3_O1	86	PCI_AD29	61	OV_{DD}	104
MDIO	53	M_DATA17	234	P1_CRS	167	P3_RXCLK	38	PCI_AD30	59	OV_{DD}	117
M_A1	193	M_DATA18	231	P1_I0	101	P3_RXD0	42	PCI_AD31	58	OV_{DD}	129
M_A2	194	M_DATA19	228	P1_I1	100	P3_RXD1	41	PCI_CBE0#	130	OV_{DD}	141
M_A3	195	M_DATA20	226	P1_O0	103	P3_RXD2	40	PCI_CBE1#	118	OV_{DD}	157
M_A4	196	M_DATA21	224	P1_O1	102	P3_RXD3	39	PCI_CBE2#	82	OV_{DD}	174
M_A5	198	M_DATA22	221	P1_RXCLK	172	P3_RXDV	37	PCI_CBE3#	69	OV_{DD}	190
M_A6	238	M_DATA23	219	P1_RXD0	168	P3_RXER	35	PCI_CLK	45	OV_{DD}	203
M_A7	239	M_DATA24	216	P1_RXD1	169	P3_TXCLK	28	PCI_DEVSEL#	113	OV_{DD}	217
M_A8	8	M_DATA25	213	P1_RXD2	170	P3_TXD0	33	PCI_FRAME#	110	OV_{DD}	229
M_A9	9	M_DATA26	211	P1_RXD3	171	P3_TXD1	32	PCI_IDSEL	70	OV_{DD}	244
M_A10	192	M_DATA27	209	P1_RXDV	173	P3_TXD2	31	PCI_INTA#	56	OV_{SS}	5
M_A11	191	M_DATA28	207	P1_RXER	175	P3_TXD3	29	PCI_IRDY#	111	OV_{SS}	13
M_A12	189	M_DATA29	204	P1_TXCLK	182	P3_TXEN	27	PCI_PAR	116	OV_{SS}	30
M_A13	187	M_DATA30	201	P1_TXD0	177	PCI_AD0	140	PCI_RST#	57	OV_{SS}	54
M_A14	186	M_DATA31	199	P1_TXD1	178	PCI_AD1	139	PCI_STOP#	115	OV_{SS}	60
M_A15	185	M_GW0#	245	P1_TXD2	179	PCI_AD2	137	PCI_TRDY#	112	OV_{SS}	66
M_A16	184	M_GW1#	249	P1_TXD3	181	PCI_AD3	136	RSP_I0	145	OV_{SS}	73
M_ADSC0#	247	M_GW2#	254	P1_TXEN	183	PCI_AD4	135	RSP_I1	144	OV_{SS}	79
M_ADSC1#	251	M_GW3#	3	P2_COL	17	PCI_AD5	134	RSP_I2	143	OV_{SS}	83
M_ADSC2#	256	M_OE0#	246	P2_CRS	26	PCI_AD6	132	RSP_I3	142	OV_{SS}	109
M_ADSC3#	6	M_OE1#	250	P2_I0	90	PCI_AD7	131	TCK	50	OV_{SS}	114
M_ADV0#	248	M_OE2#	255	P2_I1	89	PCI_AD8	128	TDI	48	OV_{SS}	121
M_ADV1#	253	M_OE3#	4	P2_O0	92	PCI_AD9	127	TDO	47	OV_{SS}	126
M_ADV2#	1	P0_COL	159	P2_O1	91	PCI_AD10	125	TMS	49	OV_{SS}	133
M_ADV3#	7	P0_CRS	150	P2_RXCLK	21	PCI_AD11	124	DV_{DD}	44	OV_{SS}	138
M_CLK	242	P0_I0	106	P2_RXD0	25	PCI_AD12	123	DV_{DD}	96	OV_{SS}	163
M_DATA0	200	P0_I1	105	P2_RXD1	24	PCI_AD13	122	DV_{DD}	97	OV_{SS}	180
M_DATA1	202	P0_O0	108	P2_RXD2	23	PCI_AD14	120	DV_{DD}	149	OV_{SS}	188
M_DATA2	205	P0_O1	107	P2_RXD3	22	PCI_AD15	119	DV_{DD}	243	OV_{SS}	197
M_DATA3	208	P0_RXCLK	155	P2_RXDV	20	PCI_AD16	81	DV_{SS}	46	OV_{SS}	206
M_DATA4	210	P0_RXD0	151	P2_RXER	18	PCI_AD17	80	DV_{SS}	93	OV_{SS}	214
M_DATA5	212	P0_RXD1	152	P2_TXCLK	11	PCI_AD18	78	DV_{SS}	94	OV_{SS}	223
M_DATA6	215	P0_RXD2	153	P2_TXD0	16	PCI_AD19	77	DV_{SS}	99	OV_{SS}	232
M_DATA7	218	P0_RXD3	154	P2_TXD1	15	PCI_AD20	75	DV_{SS}	146	OV_{SS}	240
M_DATA8	220	P0_RXDV	156	P2_TXD2	14	PCI_AD21	74	DV_{SS}	241	OV_{SS}	252
M_DATA9	222	P0_RXER	158	P2_TXD3	12	PCI_AD22	72	OV_{DD}	2	NC	98
M_DATA10	225	P0_TXCLK	165	P2_TXEN	10	PCI_AD23	71	OV_{DD}	19		
M_DATA11	227	P0_TXD0	160	P3_COL	34	PCI_AD24	68	OV_{DD}	36		

LS100 [PQFP/256L Package] Pinout



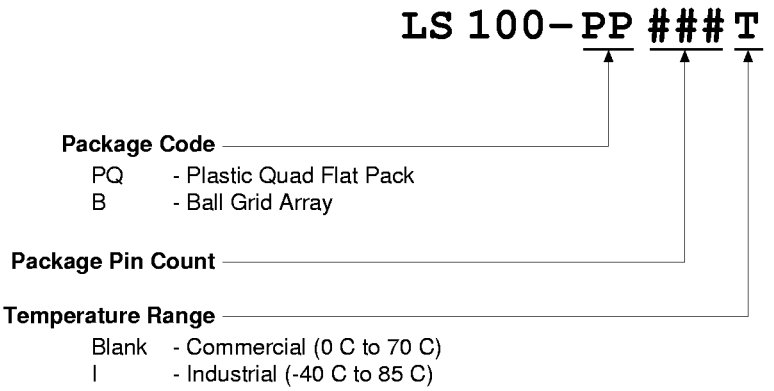
Component Availability and Ordering Information

The following table lists the LS100 package options and operating temperature ranges that are currently available. Contact I-Cube Marketing for more up–to–date information.

Device	Speed Grade	Pins	
		256	256
	Package Type:	PQFP	BGA
	Package Code:	PQ256	B256
LS100	NA	C	C

C = Commercial = 0° to +70° C

Table 8: Current Component Availability



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