

## LMC568 Low Power Phase-Locked Loop

### General Description

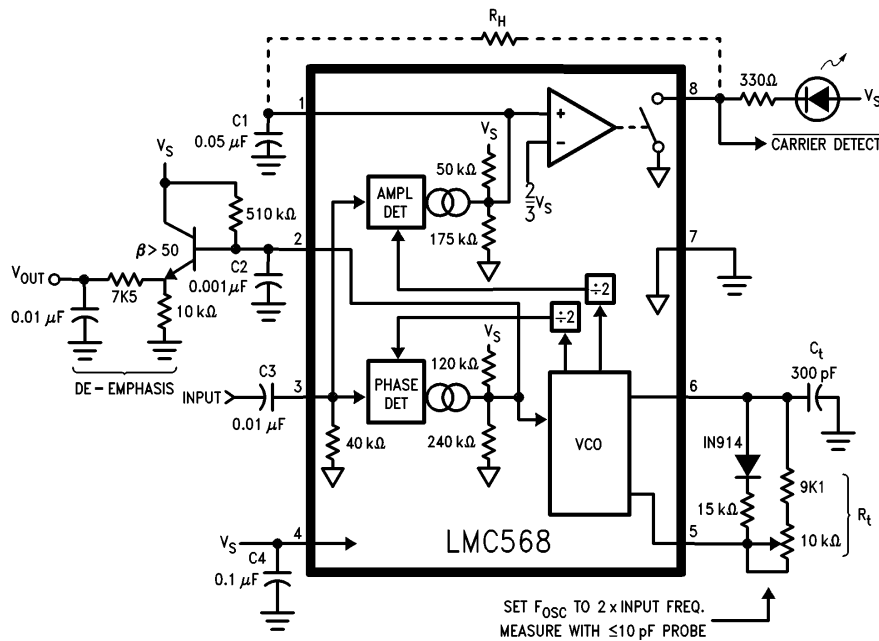
The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LMC MOS™ technology is employed for high performance with low power consumption.

The VCO has a linearized control range of  $\pm 30\%$  to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

### Features

- Demodulates  $\pm 15\%$  deviation FM/FSK signals
- Carrier Detect Output with hysteresis
- Operation to 500 kHz input frequency
- Low THD—0.5% typ. for  $\pm 10\%$  deviation
- 2V to 9V supply voltage range
- Low supply current drain

### Typical Application (100 kHz input frequency, refer to notes pg. 3)



Order Number LMC568CM or LMC568CN  
See NS Package Number M08A or N08E

TL/H/9135-1

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage, Pin 3	2 V <sub>p-p</sub>
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	V <sub>S</sub> to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW

Operating Temperature Range (T<sub>A</sub>) -25°C to +125°C  
Storage Temperature Range -55°C to +150°C

Soldering Information  
Dual-In-Line Package  
Soldering (10 seconds) 260°C  
Small Outline Package  
Vapor Phase (60 seconds) 215°C  
Infrared (15 seconds) 220°C

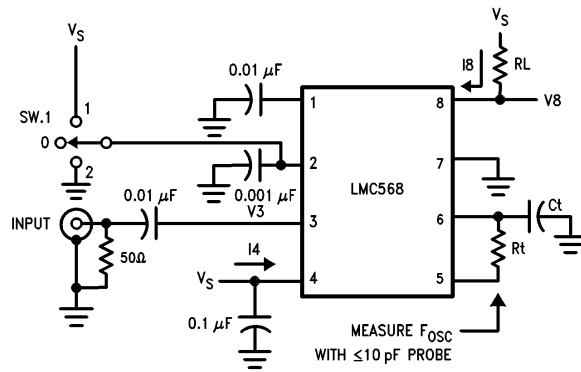
See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics

Test Circuit, T<sub>A</sub> = 25°C, V<sub>S</sub> = 5V, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
I <sub>4</sub>	Power Supply Current	RtCt #1, Quiescent or Activated	V <sub>S</sub> = 2V	0.35		mAdc	
			V <sub>S</sub> = 5V	0.75	1.5		
			V <sub>S</sub> = 9V	1.2	2.4		
V <sub>3</sub>	Input D.C. Bias			0		mVdc	
R <sub>3</sub>	Input Resistance			40		kΩ	
I <sub>8</sub>	Output Leakage			1	100	nAdc	
f <sub>0</sub>	Center Frequency F <sub>osc</sub> ÷ 2	RtCt #2, Measure Oscillator Frequency and Divide by 2	V <sub>S</sub> = 2V	98		kHz	
			V <sub>S</sub> = 5V	90	103		115
			V <sub>S</sub> = 9V		105		
Δf <sub>0</sub>	Center Frequency Shift with Supply	$\frac{f_{0 9V} - f_{0 2V}}{7 f_{0 5V}} \times 100$		1.0	2.0	%/V	
V <sub>in</sub>	Input Threshold	Set Input Frequency Equal to f <sub>0</sub> Measured Above, Increase Input Level until Pin 8 Goes Low.	V <sub>S</sub> = 2V	8	16	25	mVrms
			V <sub>S</sub> = 5V	15	26	42	
			V <sub>S</sub> = 9V		45		
ΔV <sub>in</sub>	Input Hysteresis	Starting at Input Threshold, Decrease Input Level until Pin 8 Goes High.		1.5		mVrms	
V <sub>8</sub>	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I <sub>8</sub>	I <sub>8</sub> = 2 mA	0.06	0.15	Vdc	
			I <sub>8</sub> = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F <sub>osc</sub> with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W. = $\frac{F_{osc P2} - F_{osc P1}}{F_{osc P0}} \times 100$	V <sub>S</sub> = 2V		30	%	
			V <sub>S</sub> = 5V	40	55		
			V <sub>S</sub> = 9V		60		
ΔBW	Bandwidth Skew	$Skew = \left( \frac{F_{osc P2} + F_{osc P1}}{2 F_{osc P0}} - 1 \right) \times 100$		1	±5	%	
V <sub>out</sub>	Recovered Audio	Typical Application Circuit Input = 100 mVrms, F = 100 kHz F <sub>mod</sub> = 400 Hz, ±10 kHz Dev.	V <sub>S</sub> = 2V	170		mVrms	
			V <sub>S</sub> = 5V		270		
			V <sub>S</sub> = 9V		400		
THD	Total Harmonic Distortion	Typical Application Circuit as Above, Measure V <sub>out</sub> Distortion.		0.5		%	
$\frac{S+N}{N}$	Signal to Noise Ratio	Typical Application Circuit Remove Modulation, Measure V <sub>n</sub> (S + N)/N = 20 log (V <sub>out</sub> /V <sub>n</sub> ).		65		dB	
f <sub>max</sub>	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2		700		kHz	

## Test Circuit



RtCt	Rt	Ct
# 1	100k	300 pF
# 2	10k	300 pF
# 3	5.1k	62 pF

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## Notes to Typical Application

### SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close to possible to pin 4. Also, due to pin voltages tracking supply, a large C4 is necessary for low frequency PSRR.

### OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC568 must be set up to run at twice the frequency of the input signal. The components shown in the typical application are for  $F_{osc} = 200$  kHz (100 kHz input frequency). For operation at lower frequencies, increase the capacitor value; for higher frequencies proportionally reduce the resistor values.

If low distortion is not a requirement, the series diode/resistor between pins 6 and 5 may be omitted. This will reduce VCO supply dependence and increase  $V_{out}$  by approximately 2 dB with THD = 2% typical. The center frequency as a function of  $R_t$  and  $C_t$  is given by:

$$F_{osc} \cong \frac{1}{1.4 R_t C_t} \text{ Hz}$$

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of  $R_t$ , although  $C_t$  could also be padded. The amount of initial frequency variation due to the LMC568 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of  $R_t$  and  $C_t$ .

### INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 k $\Omega$  resistor. Signals that are centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via C3.

### OUTPUT TAKEOFF

The output signal is taken off the loop filter at pin 2. Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). The nominal pin 2 source resistance is 80 k $\Omega$ , requiring the use of an external buffer transistor to drive nominal loads.

For small values of  $C_2$ , the PLL will have a fast acquisition time and the pull-in range will be set by the built-in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing  $C_2$  results in improved noise immunity at the expense of acquisition time, and the pull-in range will become narrower than the LDBW. However, the maximum hold-in range will always equal the LDBW. The 2 kHz de-emphasis pole shown may be modified or omitted as required by the application.

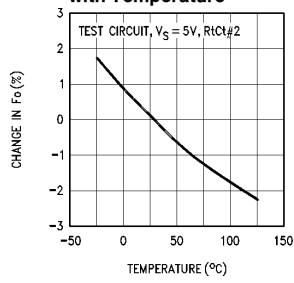
### CARRIER DETECT

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of  $7/9 V_s$ . The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input is of sufficient amplitude to cause pin 1 to fall below  $2/3 V_s$ . The carrier detect threshold is internally set to 26 mVrms typical on a 5V supply.

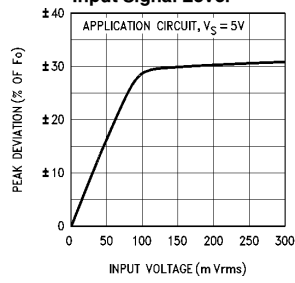
Capacitor  $C_1$  in conjunction with the nominal 40 k $\Omega$  pin 1 internal resistance forms the output filter. The size of  $C_1$  is a tradeoff between slew rate and carrier ripple at the output comparator. Optional resistor  $R_H$  increases the hysteresis in the pin 8 output for applications such as audio mute control. The minimum allowable value for  $R_H$  is 330 k $\Omega$ .

# LMC568 Typical Performance Characteristics

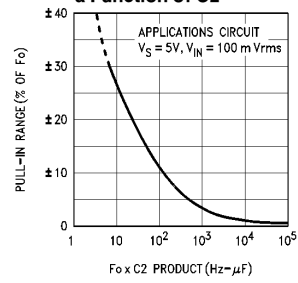
**Frequency Drift with Temperature**



**Peak Deviation vs Input Signal Level**

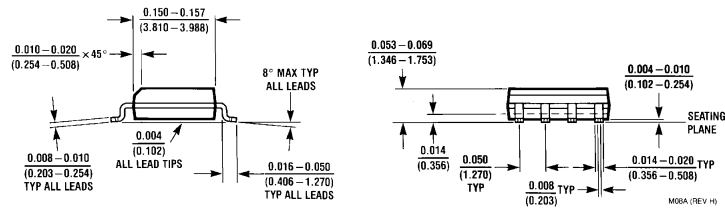
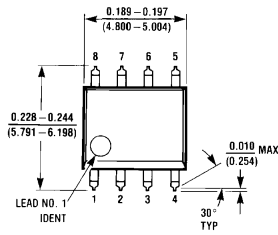


**Pull-In Range as a Function of C2**



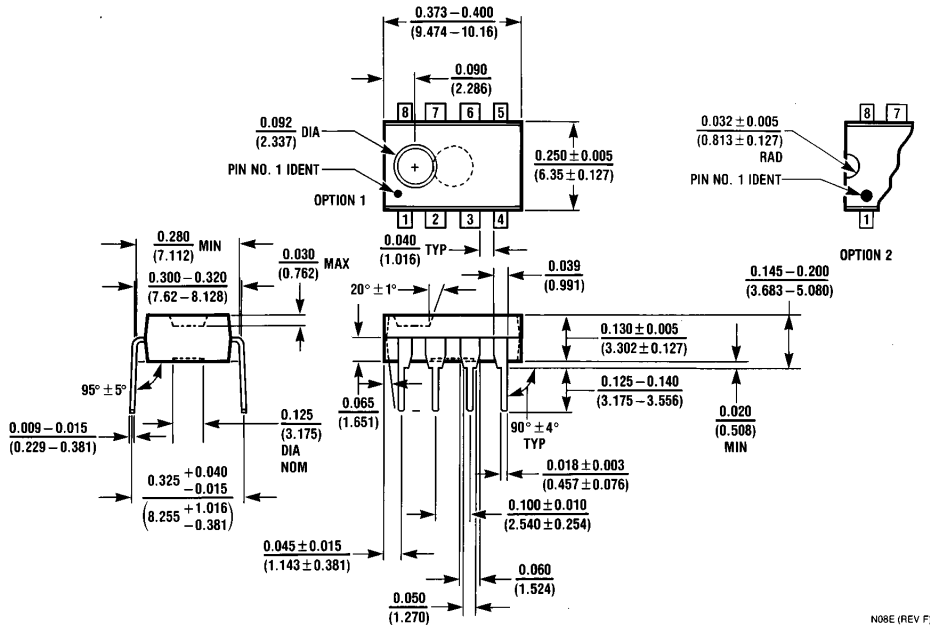
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**Physical Dimensions** inches (millimeters)



**SO Package (M)**  
**Order Number LMC568CM**  
**NS Package Number M08A**

**Physical Dimensions** inches (millimeters) (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number LMC568CN**  
**NS Package Number N08E**

N08E (REV F)

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