64M-Bit (8Mx8 /4Mx16) CMOS MASK ROM

FEATURES

- Switchable organization
  8,388,608 x 8(byte mode)
  4,194,304 x 16(word mode)
- Fast access Time
  Random Access Time/Page Access Time
  3.3V Operation : 100/30ns(max.)
  3.0V Operation : 120/40ns(max.)
- 8 words / 16bytes page access
- Supply voltage
  V_{CC} : single +3.3V/ single +3.0V
  V_{CCQ} : equal to V_{CC}
- Temperature : 0°C ~ +70°C
- Current consumption
  Operating(I_{CC}) : 60mA (max)
  Standby(I_{SB2}) : 50uA (max)
- Fully static operation
- All inputs and outputs TTL compatible
- Package
  K3P7V(U)1000B-FC : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The K3P7V(U)1000B-FC is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 8,388,608 x 8 bit(byte mode) or as 4,194,304 x 16 bit(word mode) depending on BHE voltage level. This device includes page read mode function, page read mode allows 8 words (or 16 bytes) of data to be read fast in the same page, $\overline{CE}$ and A_3 ~ A_{21} should not be changed.

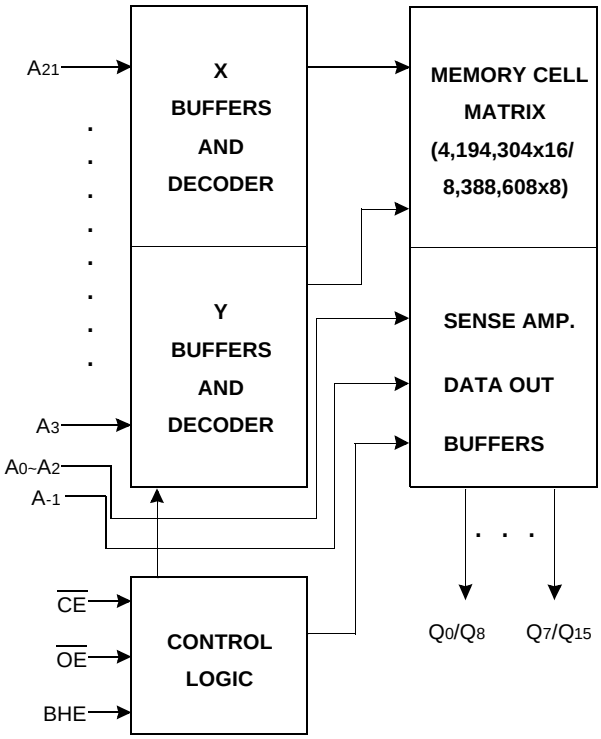
This device operates with 3.0V or 3.3V power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and operating system and/or application software storage for hand-held application.

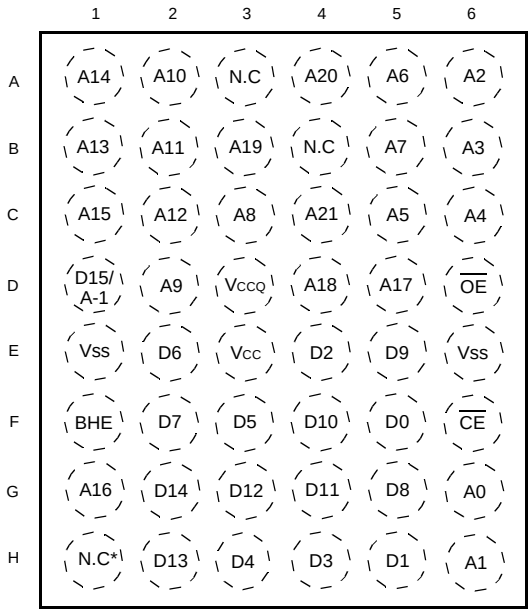
The K3P7V(U)1000B-FC is packaged in a 48-CSP with 0.75mm ball pitch and 6x8 ball array.

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0 - A_2	Page Address Inputs
A_3 - A_{21}	Address Inputs
Q_0 - Q_{14}	Data Outputs
Q_{15} /A_{-1}	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
V_{CCQ}	Data Output Power (=V_{CC})
V_{SS}	Ground
NC	No Connection

48FP-BGA PIN CONFIGURATION (TOP VIEW)



Note : See last page for package dimension.
N.C* : will be MSB Address for the 128Mbit.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to +4.5	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{Stg}	-55 to +150	°C
Operating Temperature	T_A	0 to +70	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}/V_{CCQ}	2.7/3.0	3.0/3.3	3.3/3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$=$\overline{OE}$=V_{IL}, all outputs open	V_{CC}=3.3V±0.3V	-	60	mA
			V_{CC}=3.0V±0.3V		50	mA
Standby Current(TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, all outputs open			500	µA
Standby Current(CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}, all outputs open			50	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		-	10	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		-	10	µA
Input High Voltage, All Inputs	V_{IH}			2.0	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.6	V
Output High Voltage Level	V_{OH}	I_{OH}=-400µA		2.4	-	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{DD}+0.3V which, during transitions, may overshoot to V_{DD}+2.0V for periods <20ns.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	BHE	Q_{15}/A_{-1}	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q_0~Q_{15} : Dout	Active
		L	Input	Operating	Q_0~Q_7 : Dout Q_8~Q_{14} : Hi-Z	Active

CAPACITANCE(T_A =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS(T_A=0°C to +70°C, V_{CC}=3.3V/3.0V±0.3V, V_{CCQ}=V_{CC}, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

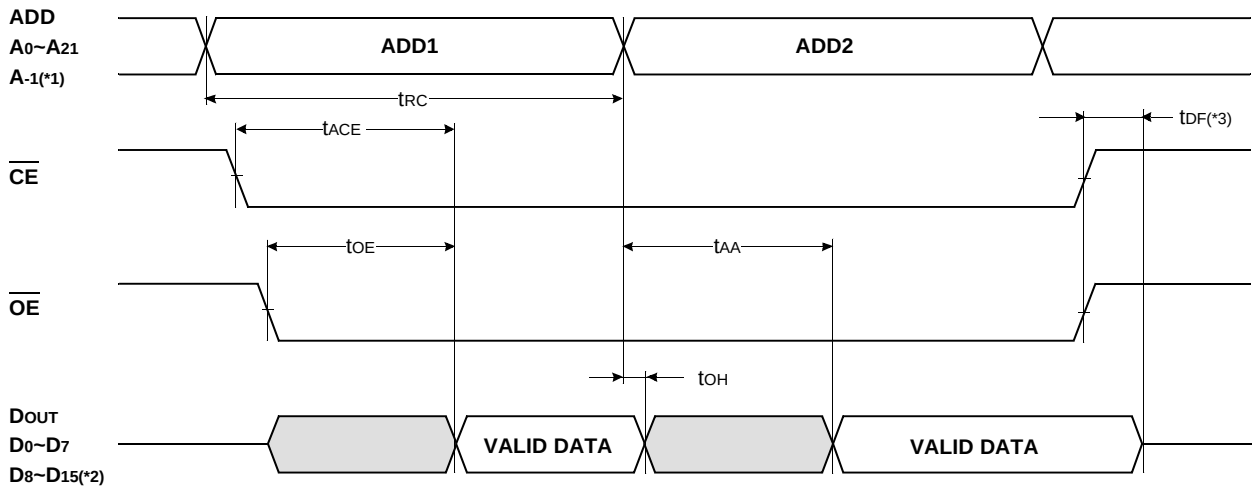
READ CYCLE

Item	Symbol	Vcc=3.3V±0.3V		Vcc=3.0V±0.3V		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	100		120		ns
Chip Enable Access Time	tACE		100		120	ns
Address Access Time	tAA		100		120	ns
Page Address Access Time	tPA		30		40	ns
Output Enable Access Time	tOE		30		40	ns
Output or Chip Disable to Output High-Z	tDF		20		20	ns
Output Hold from Address Change	tOH	0		0		ns

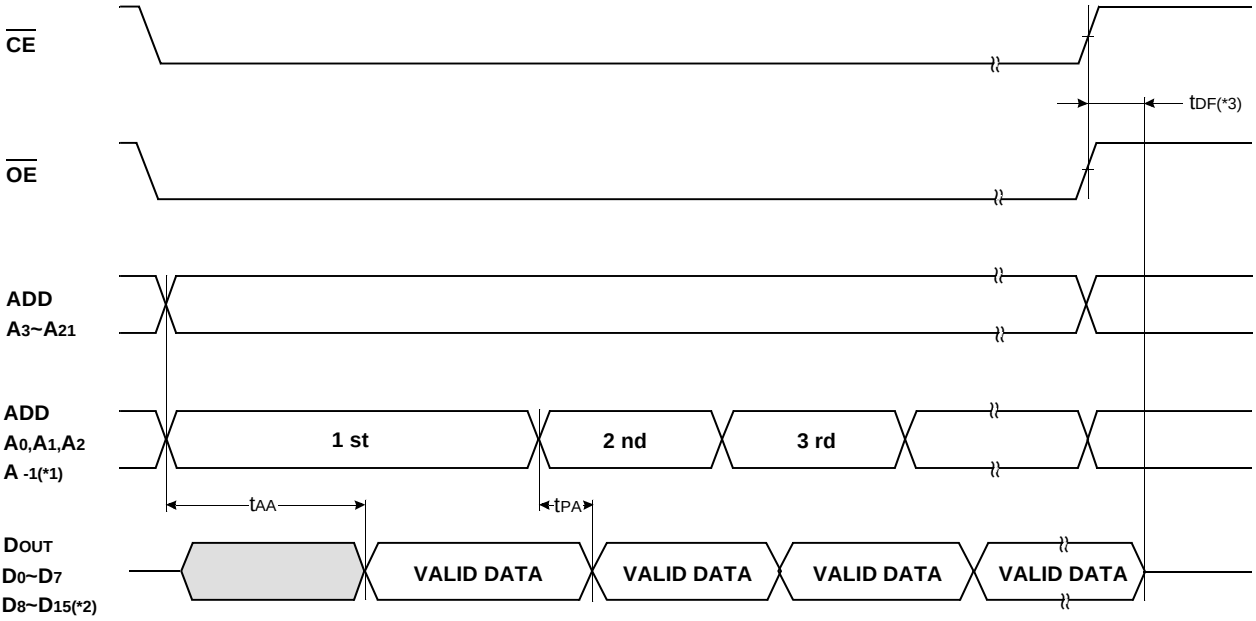
NOTE : Page Address is determined as below.
Word mode (BHE=V_{IH}) : A_0, A_1, A_2
Byte mode (BHE=V_{IL}) : A_{-1}, A_0, A_1, A_2

TIMING DIAGRAM

READ



PAGE READ



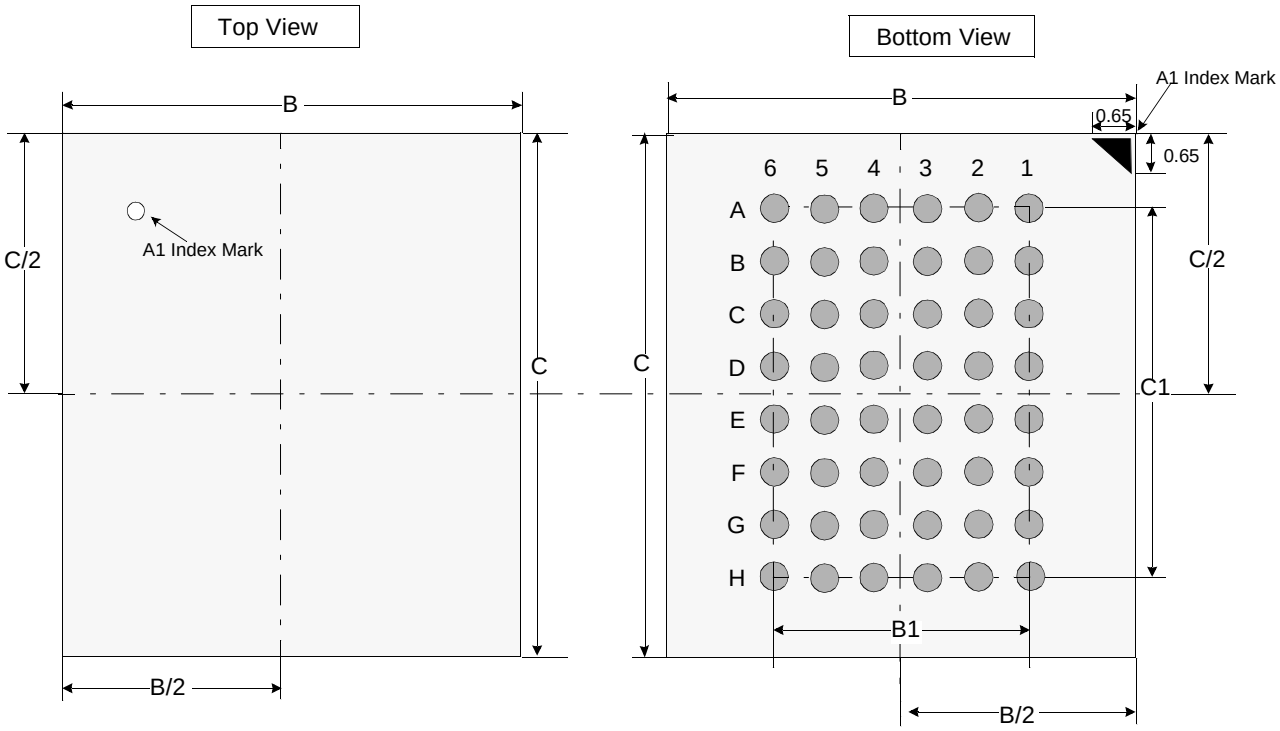
NOTES :

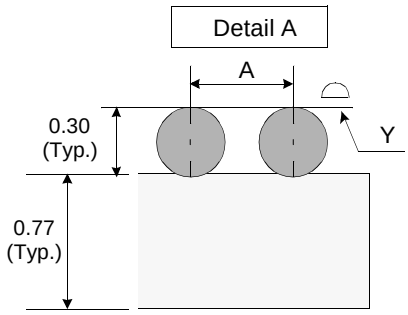
*1.Byte Mode only. A_{-1} is Least Significant Bit Address.(BHE = V_{IL})

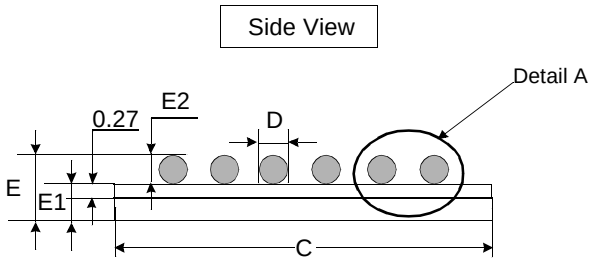
*2. Word Mode only.(BHE = V_{IH})

*3. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.

PACKAGE DIMENSIONS (48 FP-BGA)







Notes.

1. Bump counts : 48 (6 x 8 Array)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(max)

(Unit : mm)

	Min	Typ.	Max
A	-	0.75	-
B	8.90	9.00	9.10
B1	-	3.75	-
C	8.90	9.00	9.10
C1	-	5.25	-
D	0.35	0.40	0.45
E	1.00	1.10	1.20
E1	0.72	0.77	0.82
E2	0.25	0.30	0.35
Y	-	-	0.08