HARRIS

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HI-222/883

HI-222

May 1999

High Frequency/Video Switch

Features

- Wideband Operation 200MHz
- Differential Gain 0.03%
- Differential Phase . . . . . 0.003 Degrees
- Switching Speed 100ns
- r_{ON} 35Ω
- Off Isolation at 10MHz . . . . . -65dB
- Crosstalk at 10MHz . . . . . -80dB

Applications

- Routing Switchers
- Production Mixers
- High Definition TV
- Radar Signal Conditioning
- Medical Imaging
- Heads-Up Displays
- Simulators
- Sonar

Related Literature

- HI-222/883 Data Sheet in 1989 Military Analog Data Book

Description

The HI-222 is a high frequency analog switch that complements the Harris family of high speed op amps and buffers. Fabricated with our Dielectric Isolation process and using silicon gate technology, many key parameters have been enhanced.

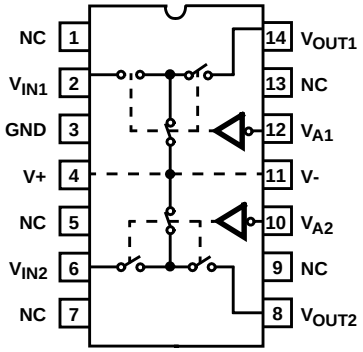
Crosstalk and off isolation are optimized with a T-switch configuration and the use of nonconnected pins for extended shielding. Other features of the HI-222 include wideband operation, low r_{ON}, fast switching speeds and low differential gain and phase. The characteristics of this TTL compatible device make it ideal for designs where improved switching performance is required.

The primary application of this dual SPST switch is the routing of high frequency signals in equipment ranging from video production mixers to military RF circuits.

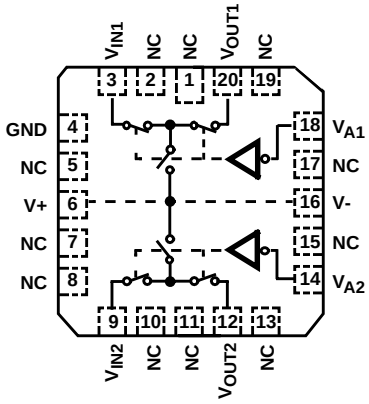
For specifications on HI-222/883, refer to Harris Military Analog Data book.

Pinouts

HI-222 (CERDIP, PDIP) (LOGIC "1" INPUT)
TOP VIEW



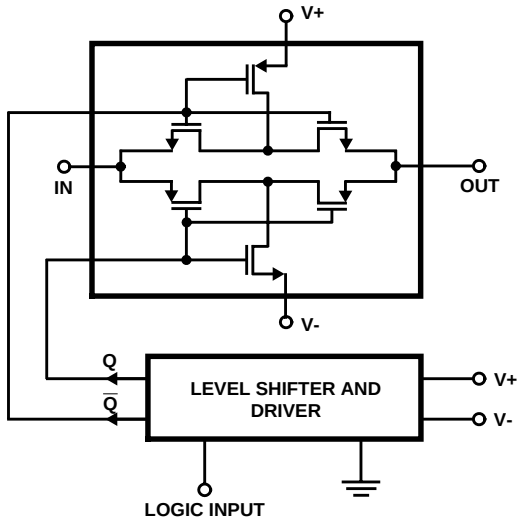
HI-222 (CLCC/PLCC) (LOGIC "0" INPUT)
TOP VIEW



Part Number Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI4P0222-5	0 to 75	20 Ld PLCC	N20.35
HI1-0222-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0222-5	0 to 75	14 Ld PDIP	E14.3

Functional Diagram



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output, respectively. They may be interchanged without affecting performance. All nonconnected pins should be tied to ground.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3124.2**

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V+ to V-) (Terminals) 36V
$\pm V_S$ to Ground (V+ to V-) . . . . . $\pm$18V
Digital Analog Input Voltage (V_A, V_S, V_D) . . . . . $\pm V_S$ $\pm$2V
I_{PEAK} (S to D) (Pulse at 0.8ms, 10% Duty Cycle Max) 100mA
I_{PEAK} (Any Pin, 50% Duty Cycle) 28mA
Continuous Current (Any Pin) 15mA
ESD Rating . . . . . <2000V

Operating Conditions

Temperature Range, HI-222-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	80	30
CLCC Package	70	18
PDIP Package	90	N/A
PLCC Package	75	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $\pm V_S = \pm 15V$, $V_{AH} = 2.0V$, $V_{AL} = 0.8V$, Unless Otherwise Specified

PARAMETER	TEMP (^oC)	HI-222-5			UNITS
		MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS					
V_S, Analog Signal Range	Full	-15	-	+15	V
r_{ON}, ON Resistance (Note 2)	25	-	35	50	Ω
	Full	-	-	75	Ω
I_{SOFF} Leakage	25	-	0.1	2.5	nA
	Full	-	-	200	nA
I_{DOFF} Leakage	25	-	0.1	2.5	nA
	Full	-	-	200	nA
I_{DON} Leakage	25	-	0.3	2.5	A
	Full	-	-	200	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Low Threshold	Full	-	-	0.8	V
V_{AH}, High Threshold	Full	2.0	-	-	V
I_{AL}, Low Level Leakage	25	-	0.1	1.0	µA
	Full	-	-	1.0	µA
I_{AH}, High Level Leakage	25	-	0.1	1.0	µA
	Full	-	-	1.0	µA
SWITCHING CHARACTERISTICS					
t_{ON} (Note 3)	25	-	100	200	ns
t_{OFF} (Note 3)	25	-	70	200	ns
Off-Isolation at 10MHz (Note 4)	25	-	-65	-	dB
Crosstalk at 10MHz (Note 4)	25	-	-80	-	dB
Differential Gain (Note 5)	25	-	0.03	-	%
Differential Phase (Note 5)	25	-	0.003	-	Degrees

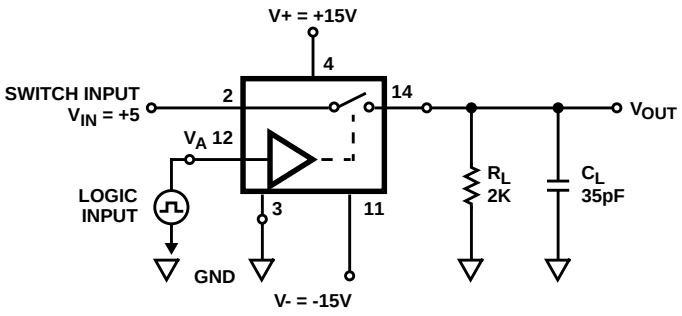
Electrical Specifications $\pm V_S = \pm 15V$, $V_{AH} = 2.0V$, $V_{AL} = 0.8V$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP (^oC)	HI-222-5			UNITS
		MIN	TYP	MAX	
Gain Tolerance At 1MHz (Note 6)	25	-	0.05	-	dB
At 8MHz	25	-	0.15	-	dB
Bandwidth (Note 6)	25	-	200	-	MHz
$C_{S(OFF)}$, Switch Input Capacitance	25	-	12	-	pF
$C_{D(OFF)}$, Switch Output Capacitance	25	-	28	-	pF
$C_{D(ON)}$, Switch Output Capacitance	25	-	83	-	pF
$C_{A(ON)}$, Switch Output Capacitance	25	-	5	-	pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	25	-	0.2	-	pF
POWER REQUIREMENTS					
1± at ±15V Quiescent Current	25	-	2.5	4.0	mA
	Full	-	-	6.0	mA
P_D, Quiescent Power Dissipation	25	-	75	120	mW
	Full	-	-	180	mW

NOTES:

2. As with all semiconductors, stresses listed under “Absolute Maximum Ratings” may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under “Electrical Specifications” are the only conditions recommended for satisfactory operation.
3. $V_{OUT} = \pm 5V$, I_{OUT} - 7.5mA.
4. $V_{IN} = +5V$, $R_L = 2k\Omega$, $C_L = 40pF$. V_A levels are 0.0V to 3.0V for switch under test. Switch not under test has $V_A = 4.0V$.
5. $V_{IN} = 300mV_{P-P}$, $R_L = 50\Omega$, $V_{AH} = +2.0V$, $V_{AL} = 0.8$, f = 10MHz.
6. $V_{IN} = 300mV_{P-P}$, $V_{OFFSET} = 1.0$, f = 3.58MHz and 4.43MHz, $V_{AL} = 0.V$, $R_L = 2k\Omega$.
7. $V_{IN} = 300mV_{P-P}$ $R_L = 50\Omega$, $V_{AL} = 0.8V$.

Test Circuits



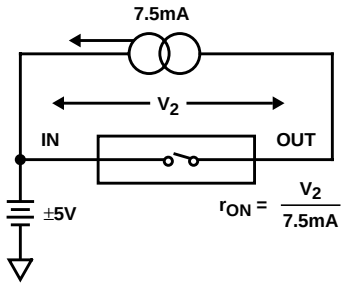
$$V_O = V_{IN} \frac{R_L}{R_L + r_{ON}}$$

C_L Includes $C_{FIXTURE} + C_{PROBE}$

FIGURE 1. SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1})

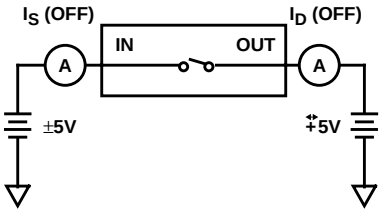
Test Circuits (Continued)

R_{DS}



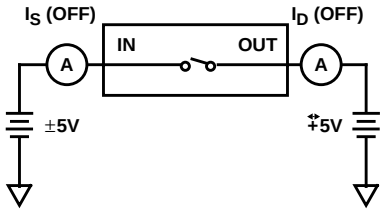
V_{IN} = ±5V, I = 7.5mA, V_A = 0.8V

I_S (OFF)



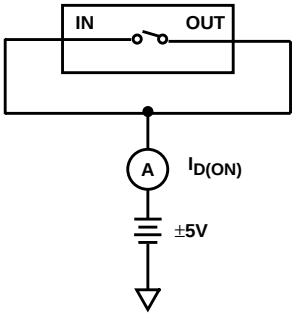
V_{IN} = ±5V, V_{OUT} = ∓5V, V_A = 2.0V

I_D (OFF)



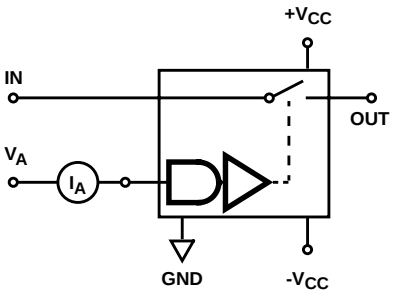
V_{IN} = ±5V, V_{OUT} = ∓5V, V_A = 2.0V

$I_{D(ON)}$



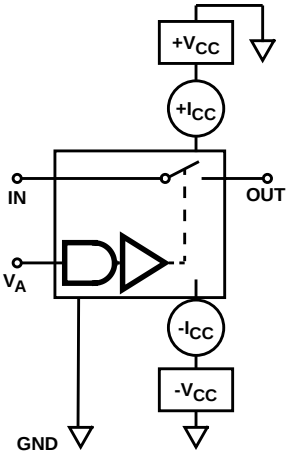
V_{IN} = ±5V, V_{OUT} = ±5V V_A = 0.8V

ADDRESS CURRENT



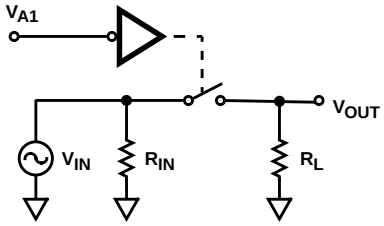
V_{AH} = 2.0V, V_{AL} = 0.8V

SUPPLY CURRENTS



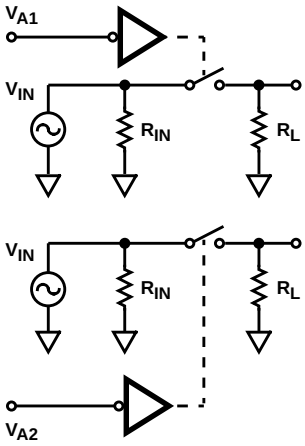
V_A = 0.8V, 2.0V

OFF ISOLATION



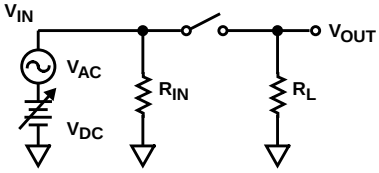
V_{IN} = 300mV_{P-P}, f = 10MHz. R_{IN} = R_L = 50Ω, V_{A1} = 2.0V

CROSSTALK



V_{IN} = 300mV_{P-P}, f = 10MHz R_{IN} = R_L = 50Ω, V_{A1} = 2.0V, V_{A2} = 0.8V

DIFFERENTIAL GAIN, PHASE



V_{AC} = 300mV_{P-P}, f = 3.58MHz AND 4.43MHz, V_{DC} = 0.0V TO 1.0V, R_L = 2kΩ, R_{IN} = 50Ω

Switching Waveforms

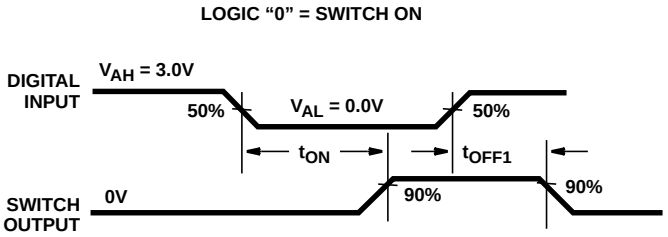
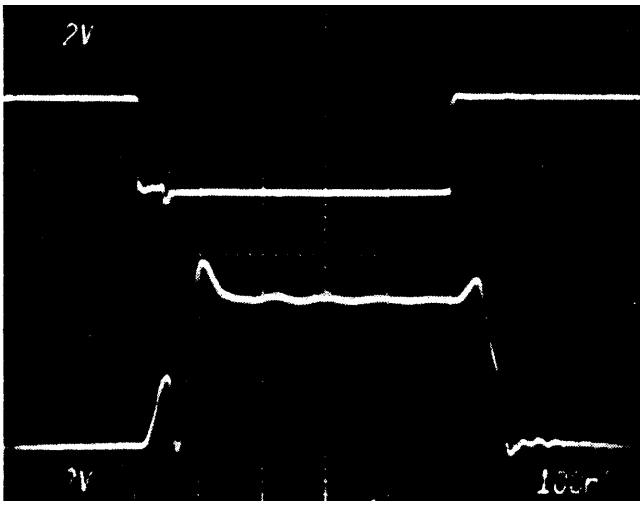


FIGURE 2. LOGIC “0” = SWITCH ON



TOP: (2V/DIV.)
BOTTOM: OUTPUT (2V/DIV.)
HORIZONTAL: 100ns/DIV.

FIGURE 3. t_{ON}, t_{OFF}, V_{AL} = 0.0V, V_{AH} = 3.0V

Typical Performance Curves

Unless Otherwise Specified: $T_A = 25^oC$, $VS_{UPPLY} = \pm 15V$

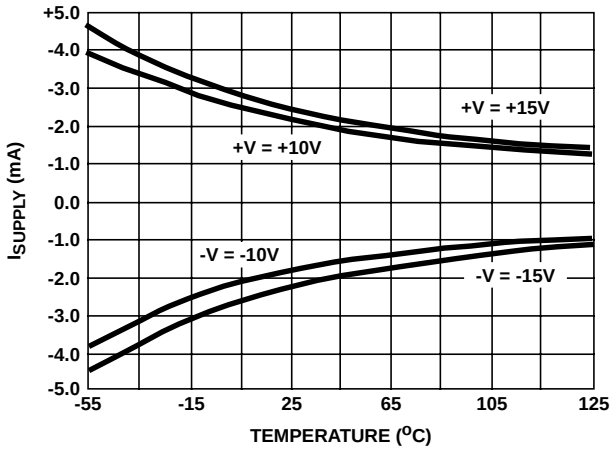


FIGURE 4. SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

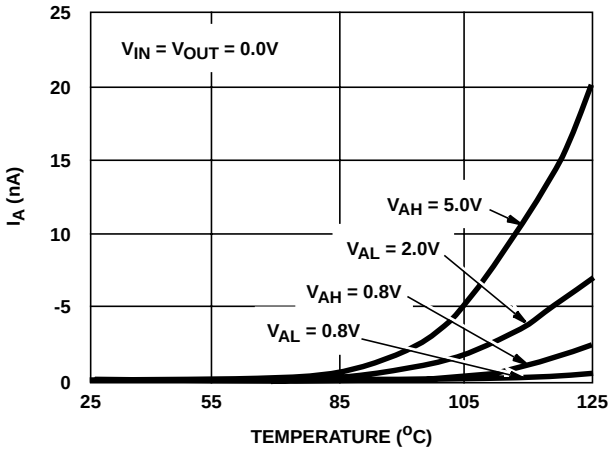


FIGURE 5. STEADY STATE ADDRESS INPUT CURRENT vs TEMPERATURE

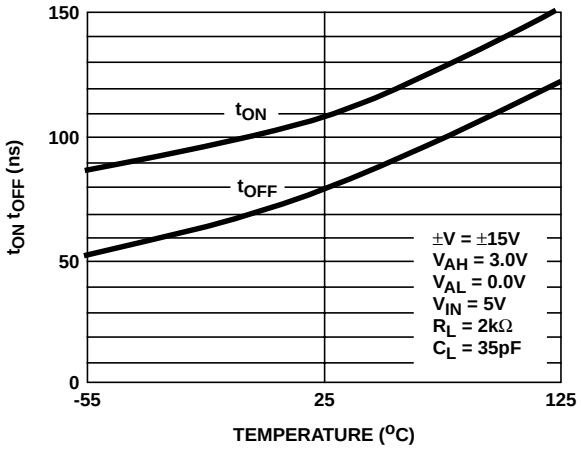


FIGURE 6. SWITCHING TIME vs TEMPERATURE

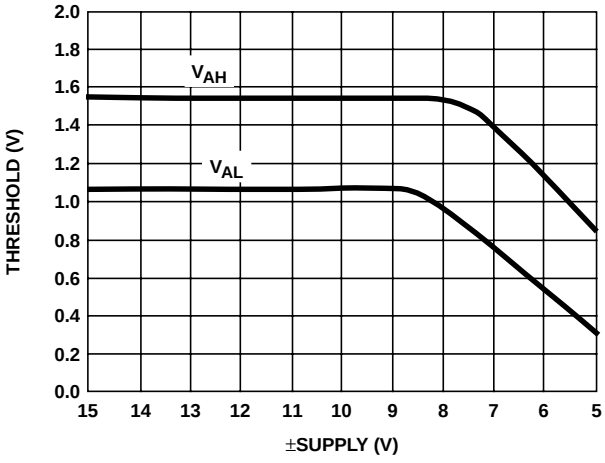


FIGURE 7. SWITCHING THRESHOLD vs ±SUPPLY VOLTAGE

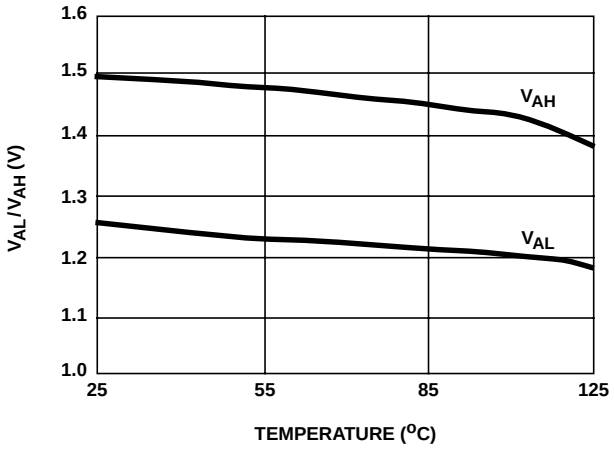


FIGURE 8. ADDRESS INPUT THRESHOLD vs TEMPERATURE

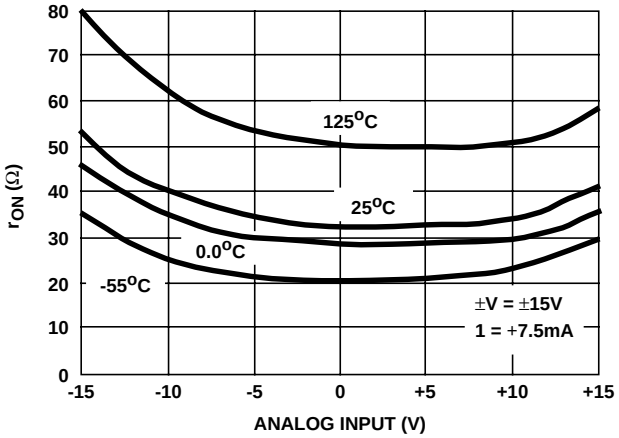


FIGURE 9. r_{ON} vs ANALOG INPUT vs TEMPERATURE

Typical Performance Curves

Unless Otherwise Specified: $T_A = 25^oC$, $VS_{UPPLY} = \pm15V$ **(Continued)**

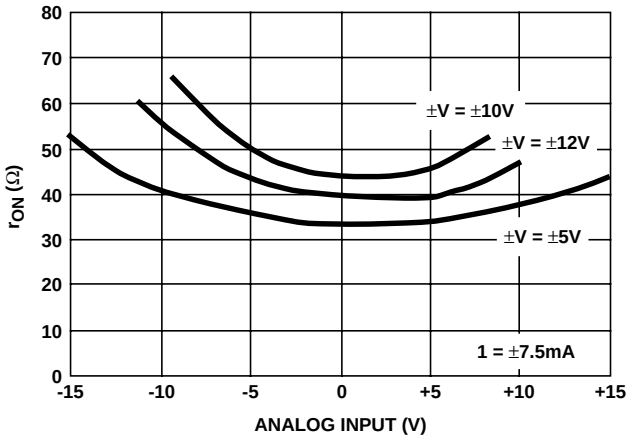


FIGURE 10. r_{ON} vs ANALOG INPUT vs SUPPLY VOLTAGE

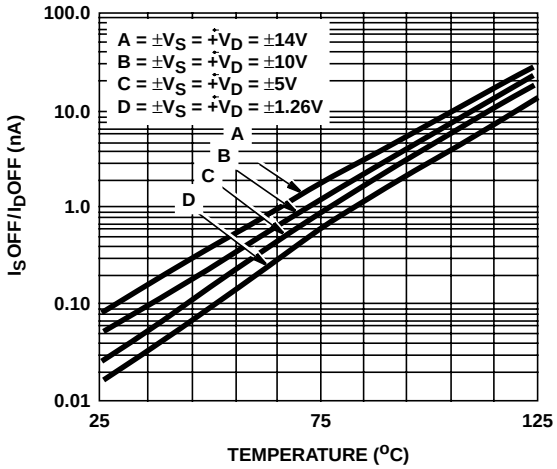


FIGURE 11. I_{SOFF}/I_{DOFF} vs TEMPERATURE vs ANALOG INPUT

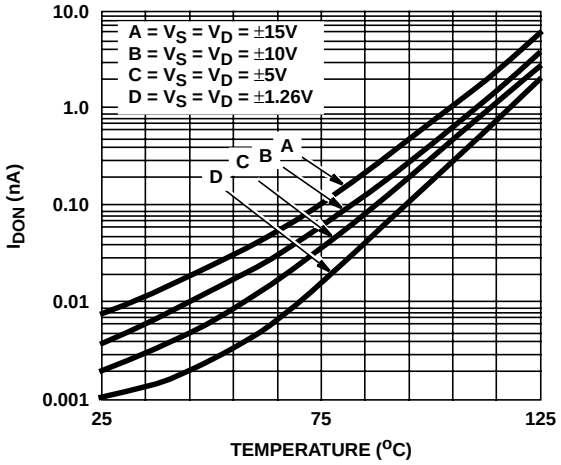


FIGURE 12. I_{DON} vs TEMPERATURE vs ANALOG INPUT

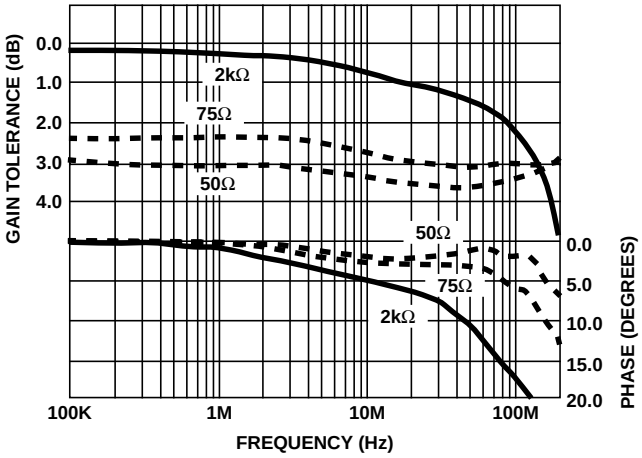


FIGURE 13. BANDWIDTH

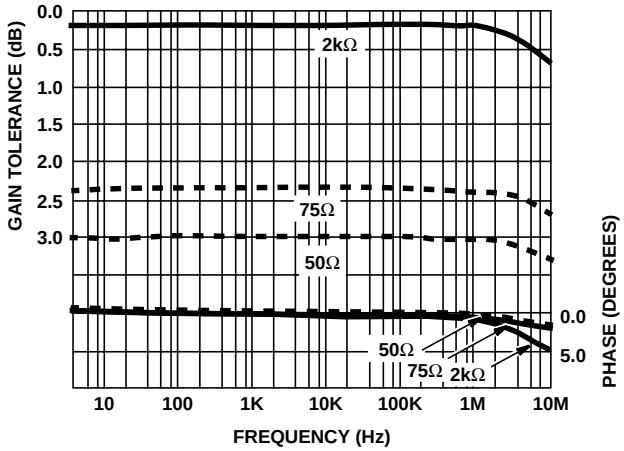


FIGURE 14. GAIN TOLERANCE

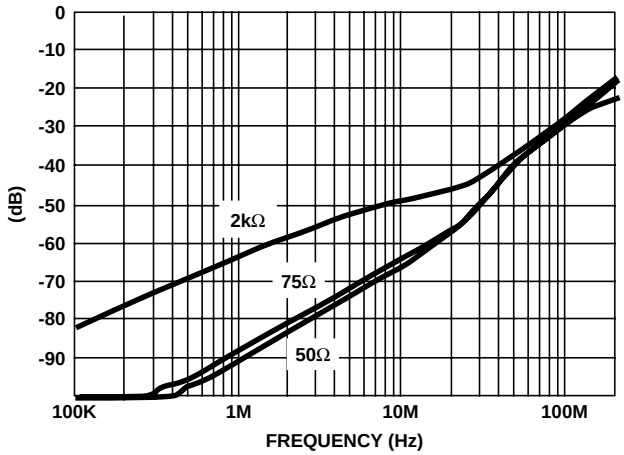
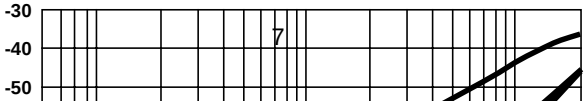
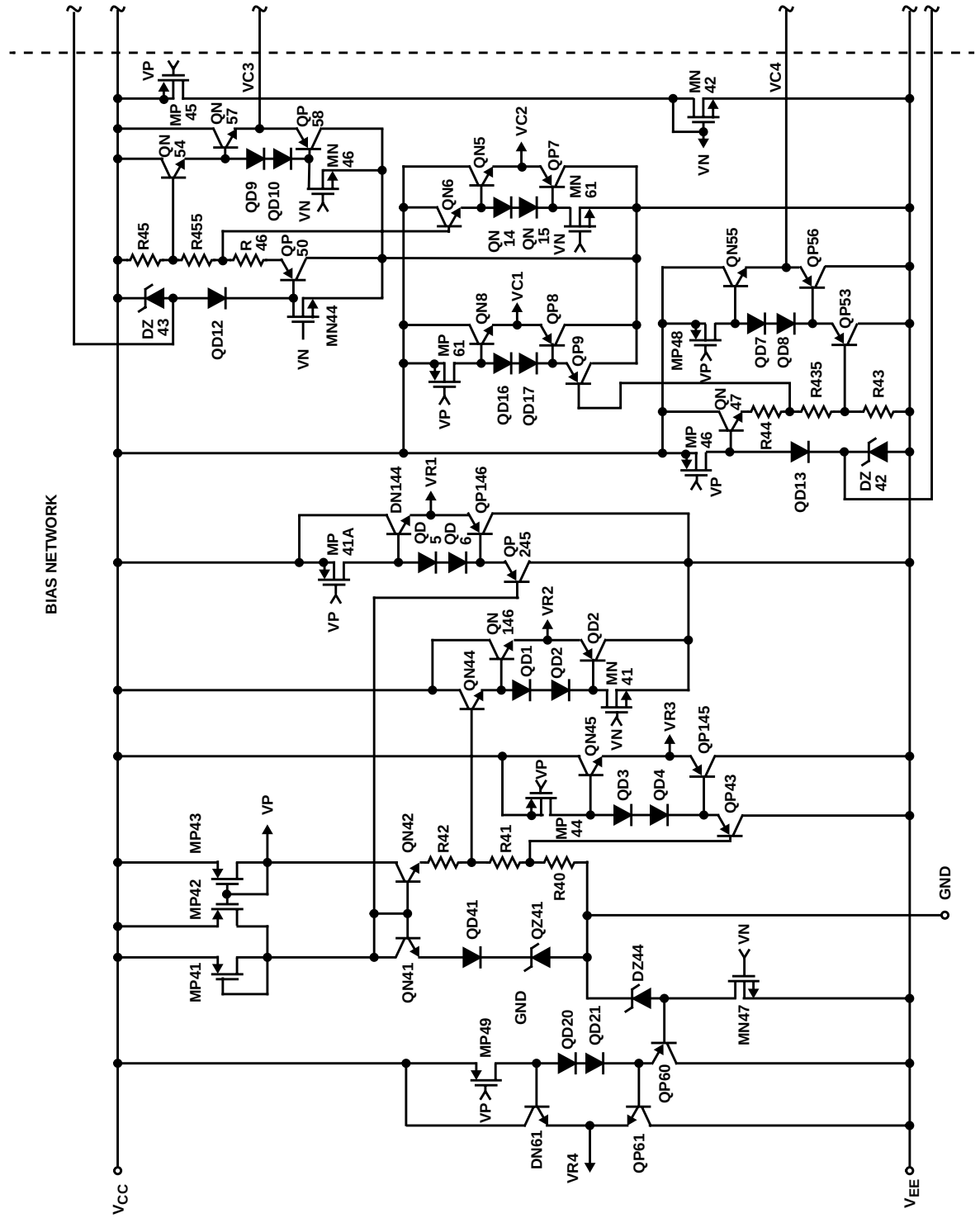


FIGURE 15. OFF ISOLATION



Schematic Diagram



Schematic Diagram (Continued)