

## FIN1047

### 3.3V LVDS 4-Bit Flow-Through High Speed Differential Driver

#### General Description

This quad driver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTTL signal levels to LVDS levels with a typical differential output swing of 350mV which provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1047 can be paired with its companion receiver, the FIN1048, or any other LVDS receiver.

#### Features

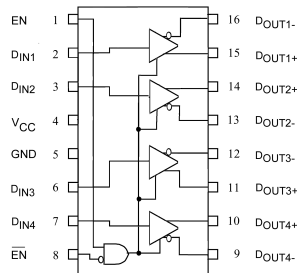
- Greater than 400Mbps data rate
- Flow-through pinout simplifies PCB layout
- 3.3V power supply operation
- 0.4 ns maximum differential pulse skew
- 1.7 ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and LVPECL devices
- 16-Lead SOIC and TSSOP packages save space

#### Ordering Code:

Order Number	Package Number	Package Description
FIN1047M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1047MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



#### Pin Descriptions

Pin Name	Description
D <sub>IN1</sub> , D <sub>IN2</sub> , D <sub>IN3</sub> , D <sub>IN4</sub>	LVTTTL Data Inputs
D <sub>OUT1+</sub> , D <sub>OUT2+</sub> , D <sub>OUT3+</sub> , D <sub>OUT4+</sub>	Non-Inverting Driver Outputs
D <sub>OUT1-</sub> , D <sub>OUT2-</sub> , D <sub>OUT3-</sub> , D <sub>OUT4-</sub>	Inverting Driver Outputs
EN	Driver Enable Pin
$\overline{\text{EN}}$	Inverting Driver Enable Pin
V <sub>CC</sub>	Power Supply
GND	Ground

#### Truth Table

Inputs			Outputs	
EN	$\overline{\text{EN}}$	D <sub>IN</sub>	D <sub>OUT+</sub>	D <sub>OUT-</sub>
H	L or OPEN	H	H	L
H	L or OPEN	L	L	H
H	L or OPEN	OPEN	L	H
X	H	X	Z	Z
L or OPEN	X	X	Z	Z

H = HIGH Logic Level    L = LOW Logic Level  
X = Don't Care          Z = High Impedance

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +6V
DC Input Voltage ( $V_{OUT}$ )	-0.5V to 4.6V
Driver Short Circuit Current ( $I_{OSD}$ )	Continuous
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Max Junction Temperature ( $T_J$ )	150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 9000V
ESD (Machine Model)	≥ 1200V

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	3.0V to 3.6V
Input Voltage ( $V_{IN}$ )	0 to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C

**Note 1:** The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

**DC Electrical Characteristics**

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
$V_{OD}$	Output Differential Voltage	$R_L = 100\Omega$ , Driver Enabled, See Figure 1	250	340	450	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change from Differential LOW-to-HIGH		1.4	25	mV	
$V_{OS}$	Offset Voltage		1.125	1.25	1.375	V
$\Delta V_{OS}$	Offset Magnitude Change from Differential LOW-to-HIGH		1.2	25	mV	
$V_{OH}$	HIGH Output Voltage	$V_{IN} = V_{CC}$		1.4	1.6	V
$V_{OL}$	LOW Output Voltage	$V_{IN} = 0V$	0.9	1.05		V
$I_{OFF}$	Power Off Output Current	$V_{CC} = 0V$ , $V_{OUT} = 0V$ or 3.6V	-20		20	$\mu A$
$I_{OS}$	Short Circuit Output Current	$V_{OUT} = 0V$ , Driver Enabled		-3	-6	mA
		$V_{OD} = 0V$ , Driver Enabled		-3.5	-6	
$V_{IH}$	Input HIGH Voltage		2.0		$V_{CC} + 1.0$	V
$V_{IL}$	Input LOW Voltage (Note 3)		GND		0.8	V
$I_{IN}$	Input Current	$V_{IN} = 0V$ or $V_{CC}$	-20		20	$\mu A$
$I_{OZ}$	Disabled Output Leakage Current	$V_{OUT} = 0V$ or 4.6V	-20		20	$\mu A$
$I_{I(OFF)}$	Power-Off Input Current	$V_{CC} = 0V$ , $V_{IN} = 0V$ or 3.6V	-20		20	$\mu A$
$V_{IK}$	Input Clamp Voltage	$I_{IK} = -18$ mA	-1.5	-0.7		V
$I_{CC}$	Power Supply Current	No Load, $V_{IN} = 0V$ or $V_{CC}$ , Driver Enabled		5	8	mA
		$R_L = 100\Omega$ , Driver Disabled		1.7	4	
		$R_L = 100\Omega$ , $V_{IN} = 0V$ or $V_{CC}$ , Driver Enabled		16	22	
$I_{PU/PD}$	Output Power Up/Power Down High Z Leakage Current	$V_{CC} = 0V$ or 1.5V	-20		20	$\mu A$

**Note 2:** All typical values are at  $T_A = 25^\circ C$  and with  $V_{CC} = 3.3V$ .

**Note 3:** For transient conditions when  $t \leq 5ns$  and  $I_{IN} \leq -100$  mA,  $V_{ILmin} = -1.0V$ .

## AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Units
$t_{PLHD}$	Differential Propagation Delay LOW-to-HIGH	$R_L = 100\ \Omega$ , $C_L = 10\ \text{pF}$ , See Figure 2 (Note 8), and Figure 3	0.6	1.1	1.7	ns
$t_{PHLD}$	Differential Propagation Delay HIGH-to-LOW		0.6	1.2	1.7	ns
$t_{TLHD}$	Differential Output Rise Time (20% to 80%)		0.4		1.2	ns
$t_{THLD}$	Differential Output Fall Time (80% to 20%)		0.4		1.2	ns
$t_{SK(P)}$	Pulse Skew $ t_{PLH} - t_{PHL} $				0.4	ns
$t_{SK(LH)}$	Channel-to-Channel Skew (Note 5)			0.05	0.3	ns
$t_{SK(HL)}$	Channel-to-Channel Skew (Note 5)				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 6)			1.0	ns	
$f_{MAX}$	Maximum Frequency (Note 7)	$R_L = 100\ \Omega$ , See Figure 6 (Note 8)	200	250		MHz
$t_{ZHD}$	Differential Output Enable Time from Z to HIGH	$R_L = 100\ \Omega$ , $C_L = 10\ \text{pF}$ , See Figure 4 (Note 8), and Figure 5		1.7	5.0	ns
$t_{ZLD}$	Differential Output Enable Time from Z to LOW			1.7	5.0	ns
$t_{HZD}$	Differential Output Disable Time from HIGH to Z			2.7	5.0	ns
$t_{LZD}$	Differential Output Disable Time from LOW to Z			2.7	5.0	ns
$C_{IN}$	Input Capacitance			4.2		pF
$C_{OUT}$	Output Capacitance			5.2		pF

**Note 4:** All typical values are at  $T_A = 25^\circ\text{C}$  and with  $V_{CC} = 3.3\text{V}$ .

**Note 5:**  $t_{SK(LH)}$ ,  $t_{SK(HL)}$  is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

**Note 6:**  $t_{SK(PP)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

**Note 7:**  $f_{MAX}$  criteria: Input  $t_R = t_F < 1\text{ns}$ , 0V to 3V, 50% Duty Cycle; Output  $V_{OD} > 250\text{mV}$ , 45% to 55% Duty Cycle; all switching in phase channels.

**Note 8:** Test Circuits in Figures 2, 4, 6 are simplified representations of test fixture and DUT loading.

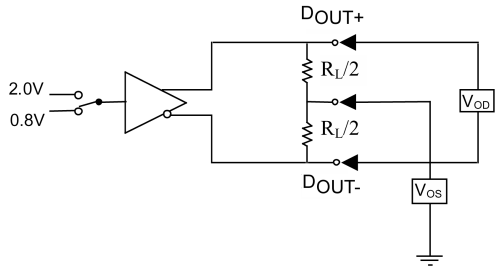
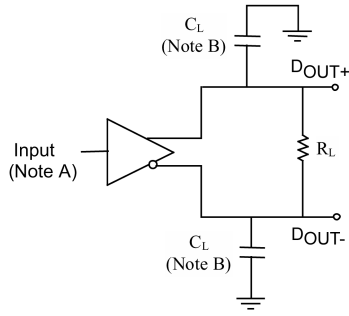


FIGURE 1. Differential Driver DC Test Circuit



Note A: All input pulses have frequency = 10 MHz,  $t_R$  or  $t_F$  = 1 ns

Note B:  $C_L$  includes all fixture and instrumentation capacitance

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

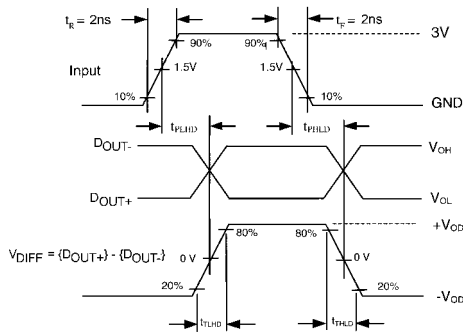
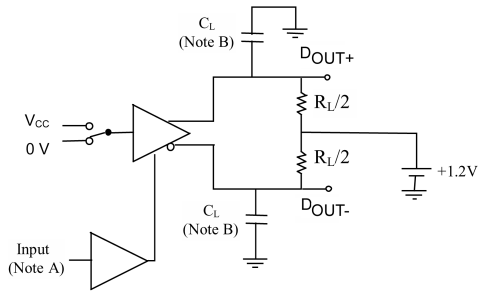


FIGURE 3. AC Waveforms



Note B: All input pulses have the frequency = 10 MHz,  $t_R$  or  $t_F$  = 1 ns

Note A:  $C_L$  includes all fixture and instrumentation capacitance

FIGURE 4. Differential Driver Enable and Disable Test Circuit

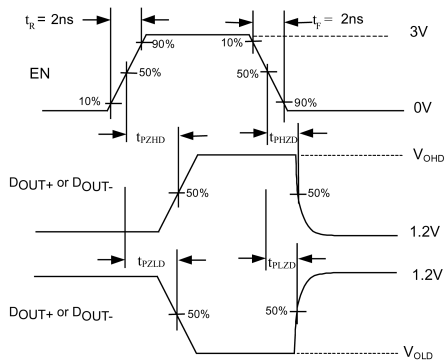


FIGURE 5. Enable and Disable AC Waveforms

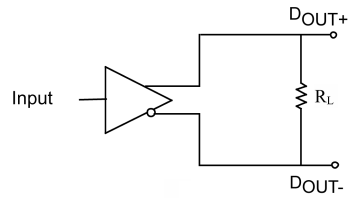


FIGURE 6.  $f_{MAX}$  Test Circuit

DC / AC Typical Performance Curves

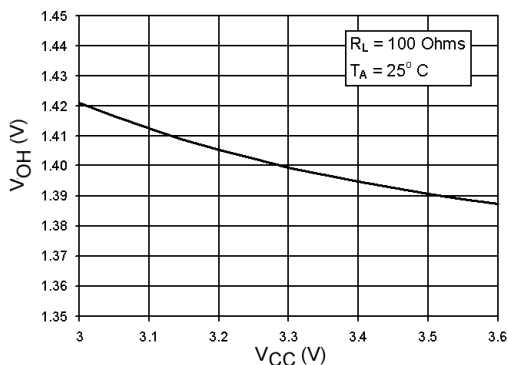


FIGURE 7. Output High Voltage vs. Power Supply Voltage

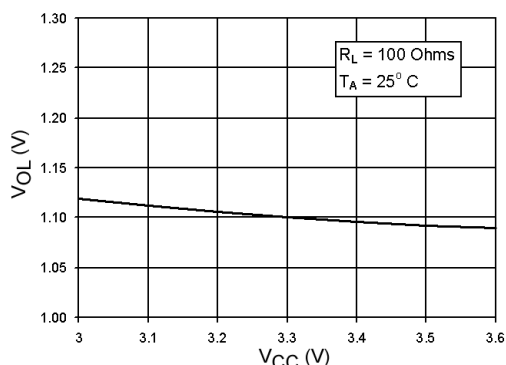


FIGURE 8. Output Low Voltage vs. Power Supply Voltage

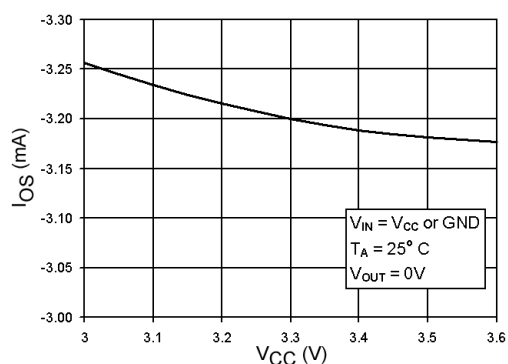


FIGURE 9. Output Short Circuit Current vs. Power Supply Voltage

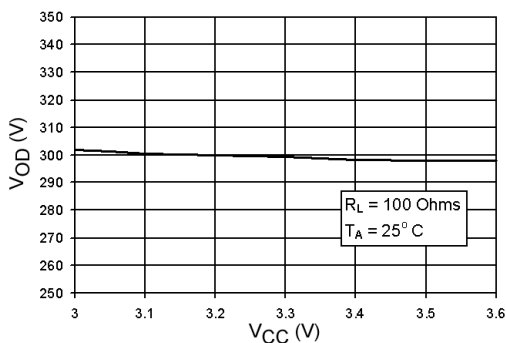


FIGURE 10. Differential Output Voltage vs. Power Supply Voltage

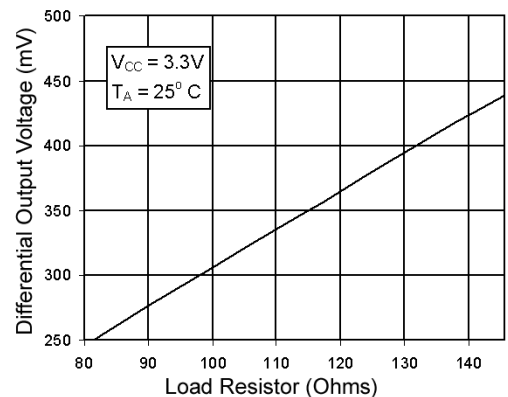


FIGURE 11. Differential Output Voltage vs. Load Resistor

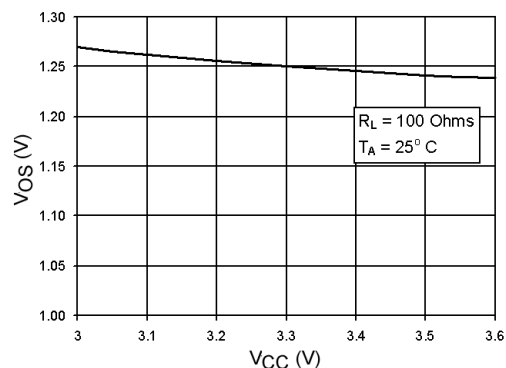


FIGURE 12. Offset Voltage vs. Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

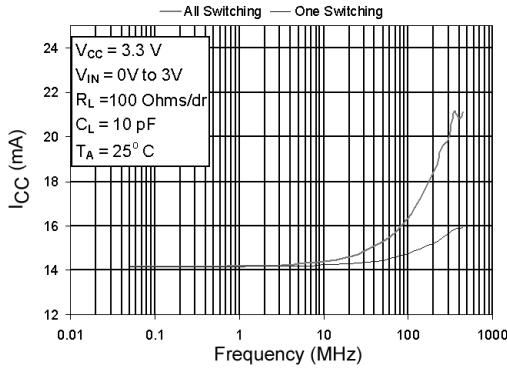


FIGURE 13. Power Supply Current vs. Frequency

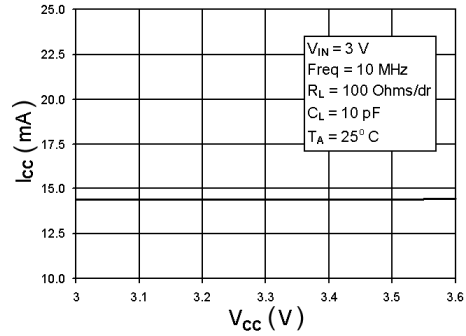


FIGURE 14. Power Supply Current vs. Power Supply Voltage

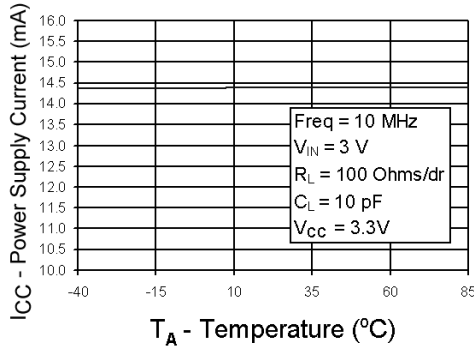


FIGURE 15. Power Supply Current vs. Ambient Temperature

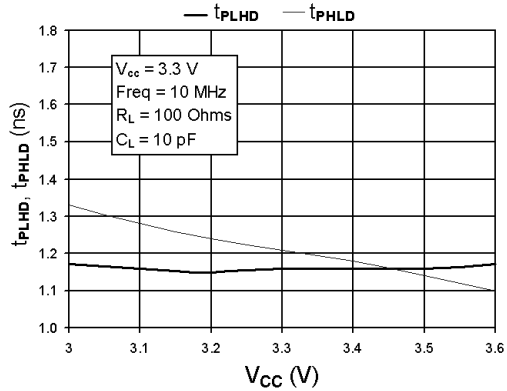


FIGURE 16. Differential Propagation Delay vs. Power Supply Voltage

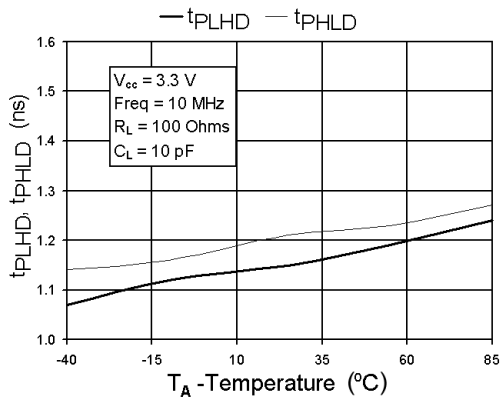


FIGURE 17. Differential Propagation Delay vs. Ambient Temperature

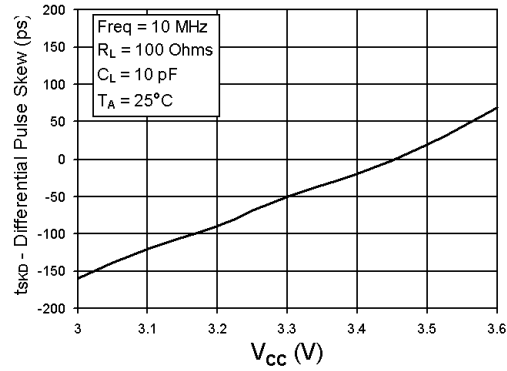


FIGURE 18. Differential Pulse Skew ( $t_{PLH} - t_{PHL}$ ) vs. Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

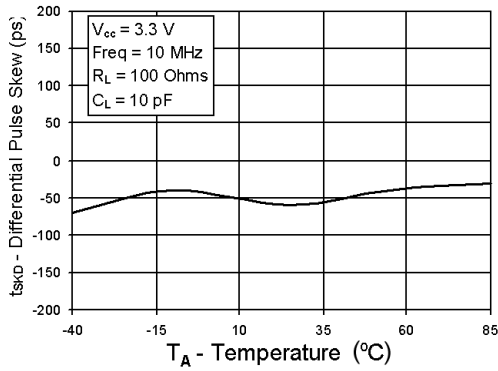


FIGURE 19. Differential Pulse Skew ( $t_{PLH} - t_{PHL}$ ) vs. Ambient Temperature

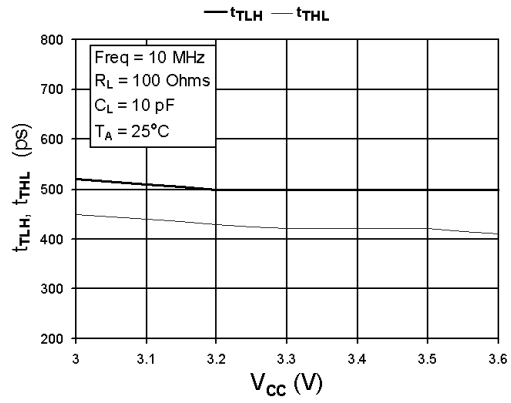


FIGURE 20. Transition Time vs. Power Supply Voltage

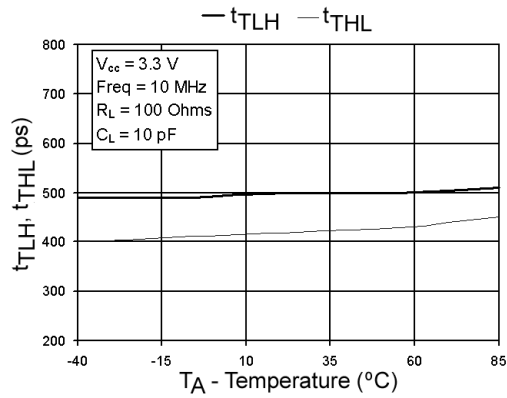
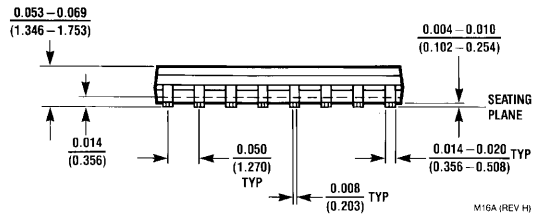
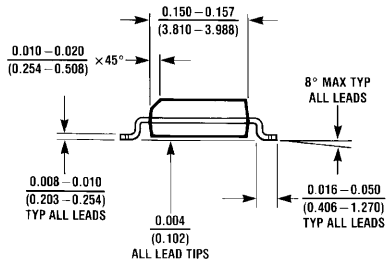
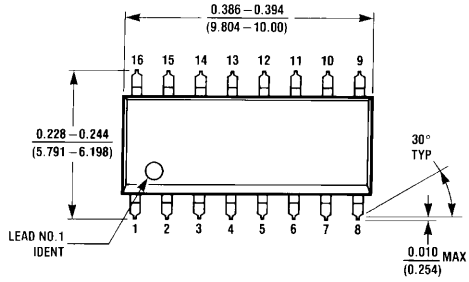


FIGURE 21. Transition Time vs. Ambient Temperature

**Physical Dimensions** inches (millimeters) unless otherwise noted

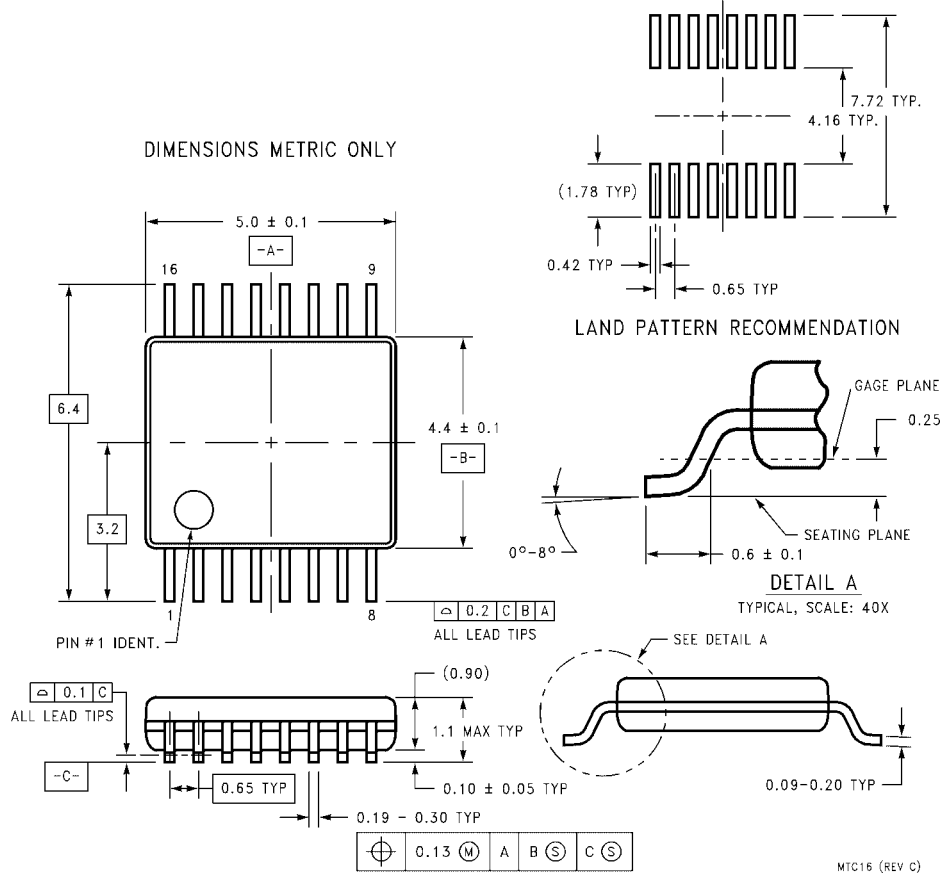


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**

M16A (REV H)



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.