ADVANCE INFORMATION

DRP 3510A
Digital Radio Processor

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MICRONAS

Contents

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Digital Radio Processor

1. Introduction

The DRP 3510A decodes digital audio data transmitted according to the Astra Digital Radio standard[1]. The DRP 3510A has a well-defined interface to the Multistandard Sound Processor MSP 3400C. The DRP 3510A and the MSP 3400C (alternatively MSP 3410D[2]) provide all functions that are necessary for ADR and DMX[3] decoding. The IC is manufactured in a low-cost 0.8 µm CMOS technology and housed in a 44-pin PLCC package.

The DRP is designed as a coprocessor for the MSP, which may already be used in a standard satellite receiver. The video baseband A/D converter, the channel selection, some preprocessing of the digital audio subcarrier, and the TV-sound output are shared with the MSP. Only those parts that are additionally required for ADR-decoding are implemented in the DRP. Thus, upgrading of existing receiver concepts for ADR compatibility is comparably simple and generates a minimum of additional costs.

The core of the digital radio processor is based on the Micronas MASC DSP. A very important feature of the MASC core is its two operating modes: the standard mode that works with 20-bit fixed point numbers and the complex mode that works with 2*10-bit numbers, consisting of a10-bit fixed point real part and a 10-bit fixed point imaginary part. This feature offers the opportunity of using the same processor for different tasks like QPSK channel demodulation, MPEG Layer 2 source decoding, and system controlling. Consequently, most parts of the ADR decoder are implemented as firmware and could easily be updated if required.

A special controllable viterbi module has been integrated with a burst decoding rate of 2 MBit/s. The data transport between the viterbi module and the DSP is done in the background with an internal non-cycle stealing DMA. This is exactly the same kind of transport mechanism that is used between the processor core and its various interfaces. The complete data-I/O handling is pushed into the background and does not affect the main processing.

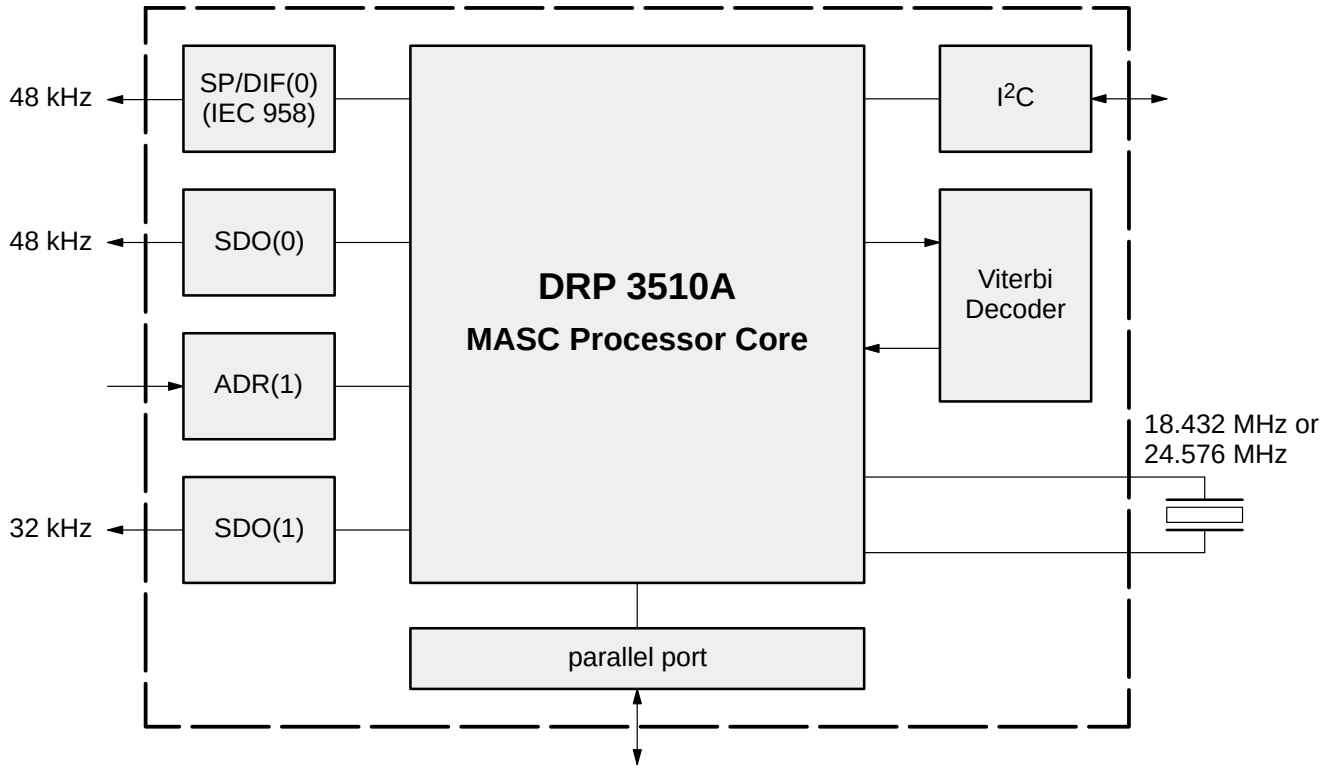


Fig. 1–1: DRP 3510A interfaces

1) ASTRA ADR/Rev. 1.3 SYS –078/02–94 TW/ab 15 December 1994

2) MSP 3410D is derived from MSP 3400C with an added NICAM decoding feature.

3) Digital Music Express (for DMX decoding, a verifier-IC and a smartcard reader is additionally required)

1.1. Main Features

– single power supply 5 V

– 44-pin PLCC plastic package

– on-chip crystal oscillator (18.432 MHz or 24.576 MHz) and internal DCO

– general purpose parallel interface

– 1 serial input interface and 2 serial output interfaces I^2S (32 kHz and 48 kHz audio out)

– SP/DIF output interface (48 kHz)

– I^2C control interface

– download feature for alternative operation modes

1.2. Building Blocks

– 20-bit MASC DSP kernel

– 2-kWord internal RAM and 6-kWord ROM (0.75 k config RAM)

– QPSK demodulator

– Viterbi decoder

– V.35 descrambling

– DMX-descrambler

– MPEG1 layer 2 decoder

– ancillary data processing

– sample rate converter

2. Functional Description

The incoming preprocessed ADR-data stream first passes the carrier offset adjustment and the intersymbol interference filtering blocks. Then, the sample rate of the signal will be decimated to the symbol rate. A bit slicer is used for the generation of the timing recovery and carrier offset adjustment control signals. Then, the signal is sent to the soft decision viterbi decoder. A linear transformation that is placed in front of the viterbi decoder leads to an optimal signal mapping with respect to signal space of the viterbi decoder. The output of the viterbi decoder is copied to the bit stream buffer of the following MPEG1 layer 2 (MUSICAM) decoder.

After the data decompression, the audio signal is available at a sampling frequency of 48 kHz at the I^2S and the SP/DIF output interfaces. A third output is used as audio feedback for the MSP. For compatibility reasons, a sample rate converter reduces the sampling frequency to 32 kHz. In addition to the pure audio signal, some ancillary data are embedded in the MPEG signal. These data are extracted, deinterleaved, error corrected, and sent to the I^2C interface, where they may be read by the receiver system controller. The software/hardware module that performs a descrambling of pay radio services (in addition to a verifier IC and a “smart card” reader) is also controlled via the I^2C bus.

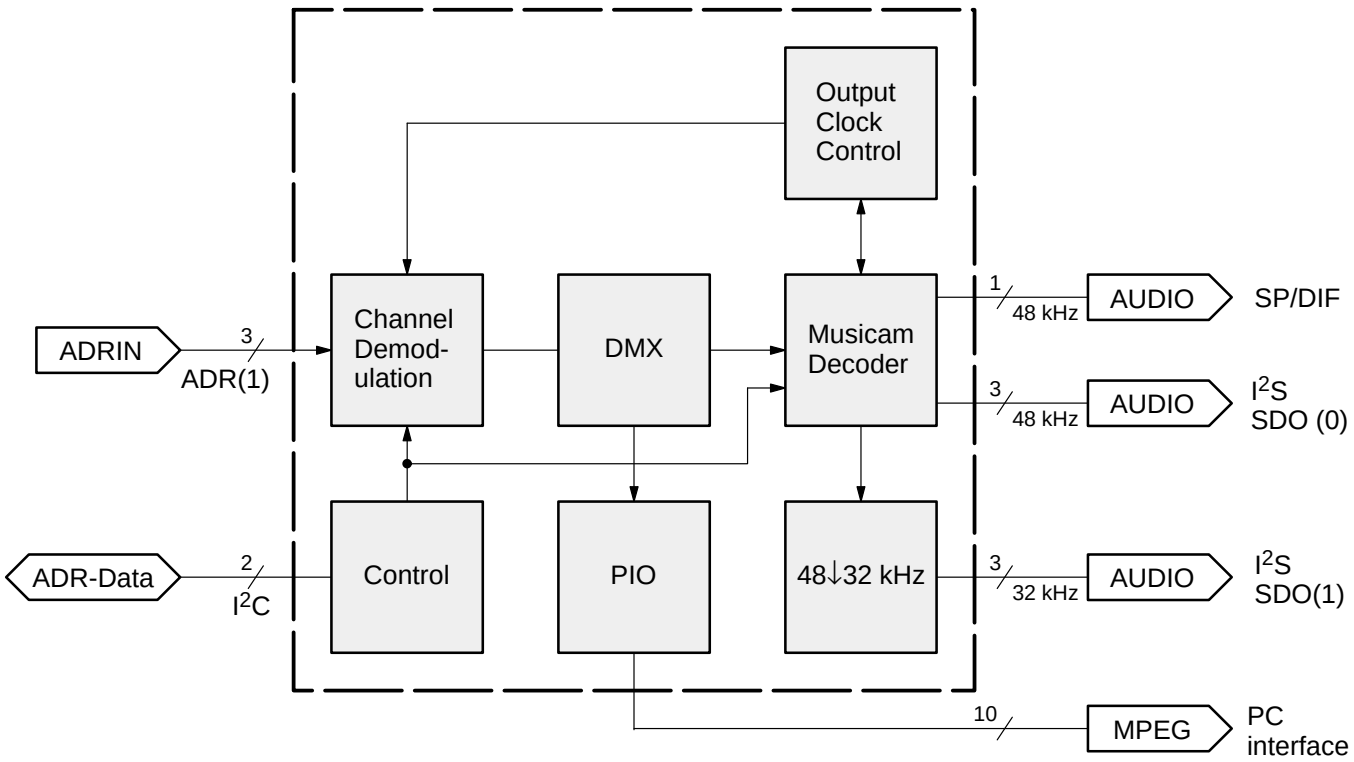


Fig. 1–2: DRP 3510A simplified block diagram

3. Specifications

3.1. Outline Dimensions

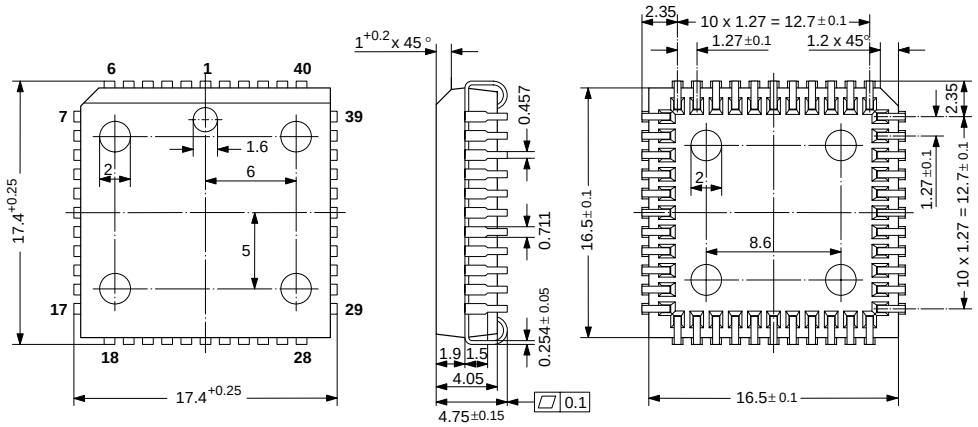


Fig. 3–1: 44-Pin Plastic Leaded Chip Carrier Package **(PLCC44)**
Weight approximately 2.5 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

VDD_10k = connected with VDD via 10 k resistor
VSS_10k = connected with VSS via 10 k resistor

Pin No. PLCC 44-pin	Connection (if not used)	Pin Name	Type	Short Description
1	X	VSS	SUPPLY	Digital Ground
2	X	VDD	SUPPLY	4.75 to 5.25 V power supply
3	LV	I^2CD	IN/OUT	I^2C-Data Line
4	VDD	I^2CC	IN/OUT	I^2C-Clock Line (must be set to VDD on reset)
5	X	PORQ	IN	Reset active low
6	LV	CLKO	OUT	Clock Out
7	X	AVSS	SUPPLY	0 V for analog circuits
8	X	XTI	IN	Crystal Input (18.432 or 24.576 MHz) base mode, Clock Input
9	X	AVDD	SUPPLY	4.75 to 5.25 V for analog circuits
10	LV	XTO	OUT	Crystal Oscillator Output
11	VSS	TE	IN	Test Enable
12	NC			

Pin No. PLCC 44-pin	Connection (if not used)	Pin Name	Type	Short Description
13	X	PI0	IN	PIO DATA [0] Crystal Select. 0: 18.432 MHz, 1: 24.576 MHz; should be connected with VSS (VDD) via a resistor (e.g. 10 k)
14	VSS_10k	PI1	IN	PIO DATA [1] reserved TASK Input; should be connected with VSS via resistors (10k)
15	VSS_10k	PI2	IN	PIO DATA [2] reserved TASK Input; should be connected with VSS via resistors (10k)
16	X	PI3	IN	PIO DATA [3] 0: ADR-mode, 1: Layer 2 decoder; should be connected with VSS (VDD) via a resistor (e.g. 10 k)
17	X	SO1C	IN/OUT	Clock of the SDO1 interface, 32 kHz audio out
18	X	SO1I	OUT	Frame indication of the SDO1 interface, 32 kHz audio out
19	X	SO1D	OUT	Data of the SDO1 interface, 32 kHz audio out
20	X	SI1C	IN/OUT	Clock of the SDI1 interface, 384 kHz clock of ADR data
21	X	SI1I	IN	Frame indication of the SDI1 interface, (I/O of ADR data)
22	X	SI1D	IN	Data of the SDI1 interface, ADR input data
23	X	VSS	SUPPLY	Digital Ground
24	X	VDD	SUPPLY	4.75 to 5.25 V power supply
25	NC			
26	LV	SPDIF	OUT	Sony Philips digital interface, 48 kHz stereo audio
27	LV	SO0C	IN/OUT	Clock of the SDO0 interface, 48 kHz audio out
28	LV	SO0I	OUT	Frame indication of the SDO0 interface, 48 kHz audio out
29	LV	SO0D	OUT	Data of the SDO0 interface, 48 kHz audio out
30	LV	PI12	(IN/OUT)	PIO DATA [12] in/out
31	LV	PI13	(IN/OUT)	PIO DATA [13] in/out
32	VSS_10k	PI14 (SI1D*)	(IN/OUT) I	PIO DATA [14] (alternative input for SI1D)
33	VSS_10k	PI15 (SI1I*)	(IN/OUT) I	PIO DATA [15] (alternative input for SI1I)
34	NC			
35	VSS_10k	PI16 (SI1C*)	(IN/OUT) I	PIO DATA [16] (alternative input for SI1C)
36	LV	PI17	(IN/OUT) O	PIO DATA [17] (not used)

Pin No. PLCC 44-pin	Connection (if not used)	Pin Name	Type	Short Description
37	LV	PI18 (CRCE)	(IN/OUT) O	PIO DATA [18] (CRC-error)
38	LV	PI19 ($\overline{FSI}$)	(IN/OUT) O	PIO DATA [19] (frame start impulse, low active)
39	VDD_10k	PCSQ	IN	PIO Chip Select
40	VDD_10k	PR	IN	PIO Read/Write
41	LV	PRTWQ	OUT	PIO Ready to Write
42	LV	PRTRQ	OUT	PIO Ready to Read
43	LV	EODQ	OUT	PIO End of DMA
44	NC			

3.3. Pin Descriptions

3.3.1. VDD, AVDD, VSS, AVSS

VDD and AVDD should be blocked against VSS and AVSS. For proper operation and in order to avoid EMV problems, a capacitive blocking of VDD against VSS over a wide frequency range is recommended.

3.3.2. I²CD

The I²CD line is used for I²C data transfers from the DRP to a controller and vice versa.

3.3.3. I²CC

The I²C clock line is used for the I²C clock if the IC is in the operation mode. However, on a power on reset, the I²C line determines the operating mode of the internal clock generator of the DRP. If the I²CC line is set to low during power on reset, the internal DRP clock is directly taken from the crystal input XTI and the internal crystal oscillator is disabled. In standard ADR mode, the I²C clock pin has to set to high level, in order to activate the internal oscillator and the internal DCO, which is used to synchronize the DRP clock system with the data rate of the incoming ADR signal.

3.3.4. PORQ

Reset input (active low). The minimum length of a reset impulse should be 100 µs. See the timing diagrams (section 12.) for the recommended power up sequence and further details.

3.3.5. CLKO

If the DRPA is driven with a 24.576 MHz quartz, the CLKO pin delivers a synchronized 18.432 MHz clock, otherwise the the CLKO pin is muted.

3.3.6. XTI, XTO

The crystal input XTI can either be used for the crystal application or for a direct input of a clock signal with the correct frequency. If the XTI signal is used for direct input, the input signal has to be DC-free, a minimum level of 0.7 V_{SS} and a maximum level of 3 V_{SS}.The XTO signal is the output of the internal crystal oscillator.

3.3.7. TE

The TE pin is reserved for chip testing only. For customer applications, this pin must always be connected to VSS.

3.3.8. PI0..PI3

In standard PIO mode, these pins are static input pins that allow the selection of different operating modes. The PI0 pin is used to select the used crystal frequency. The level of the PI0 pin is evaluated within 10 ms after reset. The PI3 pin is used to select the basic operating mode (either ADR or L2-only decoding). The PI1 and PI2 inputs are reserved for future use and have to be set to ‘0’. Because these PIx pins are generally used as input pins, it is recommended to connect them with a fixed potential. However, in DMA output mode, they operate as output pins. Thus, their connection with VSS or VDD should be done via 10 k resistors in order to avoid short-circuits.

3.3.9. SO1C, SO1I, SO1D

These three serial data output lines transport the decoded ADR/DMX signal at a sample rate of 32 kHz. An

internal sample rate converter performs the 48 to 32 kHz downsampling. For proper ADR-operation, it is mandatory to connect them with one I^2S input of the MSP. The MSP clock system has to be switched into ‘slave mode’. The data word is not delayed vs. the word-strobe (SO1I) signal.

3.3.10. SI1C, SI1D, SI1I (ADR input interface)

The ADR input interface has to be connected with the ADR/S-Bus interface of the MSP chip. In Layer 2 mode, the lines SI1C (for clock) and SI1D (for data) will expect a valid Layer 2 data stream.

3.3.11. SPDIF

The SPDIF interface provides the ADR/DMX data in the digital SPDIF format, in accordance with the consumer standard IEC 958.

3.3.12. SO0C, SO0I, SO0D

The SO0 output interface is the standard interface for a 48 kHz additional DAC, for full sampling rate output, which is not implemented in the MSP. The data word is not delayed vs. the word-strobe (SO1I) signal by default.

3.3.13. SI1C*, SI1D*, SI1I* (PI14..16)

These lines are used as alternative input lines and could be connected e.g. with the I^2S output of the MSP. However, these input pins are not supported by the built-in firmware. Downloaded program codes can use these input lines for alternative functionality of the DRP. An example for an adequate download program is an I^2S to SP/DIF converter program that can be used to map the analog FM-sound signal from the MSP to the SP/DIF output interface of the DRP. In the standard ADR-mode, these lines are input pins that should be connected via resistors to a fixed level (VSS).

3.3.14. PI12..PI19

In standard ADR mode, the PIO pin PI19 shows the Frame Start Impulse (FSI). This impulse is synchronized with the MPEG frame and is set to low level for at maximum 23 ms, which indicates that a new ADR ancillary data block is available for read-out via I^2C. The CRC-error pin PI18 will be set to high level for 24 ms (duration of one MPEG Layer 2 frame) when an MPEG CRC error has been detected. In DMA mode, the PI12..PI19 pins will contain the 8-bit aligned undecoded MPEG data stream.

3.3.15. EODQ, PRTWQ, PR, (PRTRQ, PCSQ)

For a description of EODQ, PRTRQ, PR, see section 6.4.2. The PRTRQ line is reserved for future use. The PCSQ line is not used by the actual firmware and should be connected to VDD via a resistor.

3.4. Pin Configuration

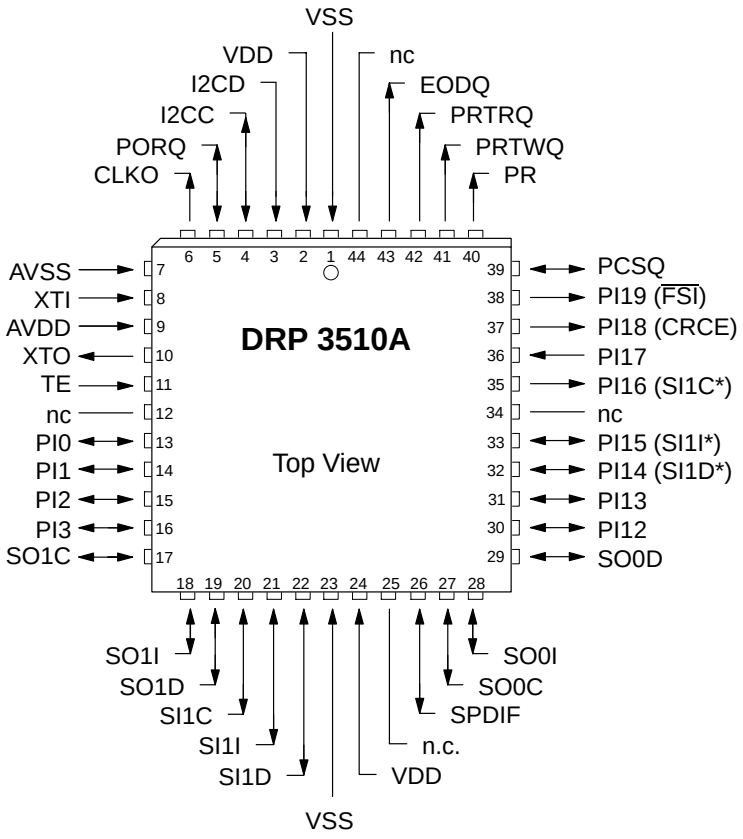


Fig. 3–2: 44-pin PLCC package

3.5. Electrical Characteristics

3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	–20	85	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP}	Supply Voltage	2, 9, 24	–0.2	6	V
V_{PIN}	Pin Voltage	all other pins	–0.3	V_{SUP}+0.3 or 6 whatever is less	V
C_L	Load Capacitance	all output pins	0	200	pF
R_L	Load Resistance to V_{SUP} or GND		500[1)]	infinite	Ω
I_L	Load Current Open Drain Outputs	3, 4		10	mA
[1)] Shorts will not damage the IC, if they do not exceed a time period of 5 s					

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.5.2. Recommended Operating Conditions at V_{SUP} = 4.75 to 5.25 V

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–	0		65	°C
V_{SUP}	Supply Voltage	2, 9, 24	4.75	–	5.25	V
f_{CP}	Internal Processor Clock Frequency (set by software)	–			40	MHz
V_{DIL}	Data Input Low Voltage	all other inputs	–		1	V
V_{DIH}	Data Input High Voltage		V_{SUP} –1		–	V
t_{RES}	$\overline{\text{Reset}}$ Input Low Time (after V_{SUP} has reached specified range)	5	20			ms
t_{Pic}	PIO Timing (see Fig. 12–1)	13–22, 28–43	50		no limit	ns
t_{Pip}	PIO Timing (see Fig. 12–1)		0		no limit	ns
t_{Pir}	PIO Timing (see Fig. 12–1)		0		no limit	ns
t_{Piset}	PIO Timing (see Fig. 12–1)		50		no limit	ns
t_{Pihold}	PIO Timing (see Fig. 12–1)		50		no limit	ns
t_{SISCLK}	SDI Timing (see Fig. 12–3)	20–22, (32, 33, 35)	120			ns
t_{SIISS}	SDI Timing (see Fig. 12–3)		30			ns
t_{SIIDS}	SDI Timing (see Fig. 12–3)		30			ns
t_{SIISH}	SDI Timing (see Fig. 12–3)		30			ns
t_{SIIDH}	SDI Timing (see Fig. 12–3)		30			ns
t_{SIILIA}	SDI Timing (see Fig. 12–3)		480		no limit	ns
t_{SOSCLK}	SDO Timing (see Fig. 12–4)	17, 27	120			ns
V_{I2ICIL}	I^2C-Bus Input Low Voltage	3, 4			0.3	V_{SUP}
V_{I2ICIH}	I^2C-Bus Input High Voltage		0.6			V_{SUP}
t_{I2C1}	I^2C-Start Condition Setup Time		120			ns
t_{I2C2}	I^2C-Stop Condition Setup Time		120			ns
t_{I2C3}	I^2C-Clock Low Pulse Time		500			ns
t_{I2C4}	I^2C-Clock High Pulse Time		500			ns
t_{I2C5}	I^2C-Data Setup Time before Rising Edge of Clock		55			ns
t_{I2C6}	I^2C-Data Hold Time after Falling Edge of Clock		55			ns
f_{I2CIH}	I^2C-Bus Frequency				1.0	MHz

3.5.3. Characteristics at V_{SUP} = 4.75 to 5.25 V, T_{amb} = 0 to 65 °C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
P	Power Consumption			900	1100	mW	at 40 MHz C_L = 30 pF on all outputs
V_{DOL}	Data Output Low Voltage	1)			0.6	V	I_{LOAD} = 10 µA
T_{FALL}	Data Output High to Low Transition Time	2)			10	ns	C_L = 50 pF max.
V_{DOH}	Data Output High Voltage	1)	V_{SUP}–0.6			V	I_{LOAD} = –10 µA
T_{Rise}	Data Output High to Low Transition Time	1)			10	ns	C_L = 50 pF max.
V_{DOLI}	I^2C Output Low Voltage, I^2C switching hysteresis on $\overline{POR}$	3, 4			0.4 0.6	V V	I_{LOAD} = 3 mA I_{LOAD} = 6 mA
I_{DOHI}	I^2C Output High Leakage Current		0		2	µA	V_{DOH} = 5 V
V_{RESHYS}	Hysteresis Voltage of $\overline{POR}$	5	160	240	320	mV	
t_{Piw}	PIO Timing (see Fig. 12–1)	13–22, 28–43	0			ns	
t_{Pie}	PIO Timing (see Fig. 12–1)		–25	0	25	ns	Equal Load Capacitance on $\overline{EOD}$, $\overline{RTR}$, and $\overline{RTW}$
t_{Pieset}	PIO Timing (see Fig. 12–1)		50			ns	C_L = 50 pF max.
t_{Pihold}	PIO Timing (see Fig. 12–1)		50			ns	C_L = 5 pF min.
t_{FSIV}	FSI Timing, (see Fig. 12–2)	38		22	23	ms	C_L = 5 pF min.
t_{FSIP}	FSI Timing, (see Fig. 12–2)		23	24	25	ms	C_L = 5 pF min.
t_{SOSCLK}	SDO Timing (see Fig. 12–4)	17–19, 27–29	120			ns	
t_{SOISS}	SDO Timing (see Fig. 12–4)		10			ns	
t_{SOODC}	SDO TIming (see Fig. 12–4)		10			ns	
t_{SPCLK}	SPDIF Timing (see Fig. 12–5)			325		ns	

1) all other output and input/output pins except 3 and 4
2) all output and input/output pins

3.5.4. Recommended Crystal Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{XCA}	External Clock Amplitude	8	0.7			V_{pp}
T_{Jitter}	Clock Jitter without Timing Recovery Control				2	ns

3.5.4.1. Single Crystal Mode – 24.576 MHz at DRP 3510A

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			24.576		MHz
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
R_R	Series Resistance				20	Ω
C_0	Shunt (Parallel) Capacitance				7.0	pF
Load Capacitance Recommendations						
C_L	External Load Capacitance*)	8, 10	18			pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)		24.574	24.576	24.578	MHz

***) Remark on defining the External Load Capacitance:**

External capacitors at each crystal pin to ground are required. They are necessary to tune the free running frequency of the DRP or the open-loop frequency of the MSP. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match 18.432/24.576 MHz as closely as possible. Due to different layouts of customer PCBs the matching capacitor size should be defined in the application. The suggested values are figures based on experience with various PCB layouts. For adjusting the DRP crystal frequency, use external capacitors with 5% tolerance.

3.5.4.2. Single Crystal Mode – 18.432 MHz at MSP 3400C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–30		+30	ppm
D_{TEM}	Frequency Variation versus Temperature		–30		+30	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
C_1	Motional (Dynamic) Capacitance		15			fF
Load Capacitance Recommendations						
C_L	External Load Capacitance*)	8, 10	3.3			pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)		18.4305	18.432	18.4335	MHz

3.5.4.3. Dual Crystal Mode – 18.432/24.576 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
For MSP						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
C_1	Motional (Dynamic) Capacitance		19	24		fF
Load Capacitance Recommendations						
C_L	External Load Capacitance*)	8, 10	3.3			pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)		18.431	18.432	18.433	MHz
For DRP						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			24.576		MHz
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
R_R	Series Resistance				20	Ω
C_0	Shunt (Parallel) Capacitance				7.0	pF
Load Capacitance Recommendations						
C_L	External Load Capacitance*)	8, 10	18			pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)		24.5747	24.576	24.5773	MHz

3.5.4.4. Dual Crystal Mode – 18.432/18.432 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
C_1	Motional (Dynamic) Capacitance (at MSP, not required at DRP)		19	24		fF
Load Capacitance Recommendations						
C_L	External Load Capacitance*)	8, 10	MSP: 3.3 DRP: 18			pF pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)		18.431	18.432	18.433	MHz

3.5.5. System Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_R	Covered frequency range for receiving	0.180		9.00	MHz
C/N_{clear}	C/N for error rate < $1*10^{-5}$		9.5		dB
C/N_{Aqu}	C/N for acquisition		8.5		dB
T_{rec}	Lock time		0.2		s
$F_{LockRange}$	Carrier Lock Range	–2.0		+2.0	kHz

4. Basic Application

The ADR decoder application shows the obligatory parts: MSP 3400C and DRP 3510A. In full transponder mode (48 ADR-channels on one transponder), the tuner output signal should be directly connected with the MSP. In standard mode, the video signal should be suppressed with a highpass filter. The two analog inputs of the MSP can be used for selecting either full-transponder or standard mode. The built-in D/A converter of the MSP generates the analog audio output. Optionally, a 48 kHz D/A converter may be connected to the second I^2S output interface. The system controlling is done via the I^2C interface.

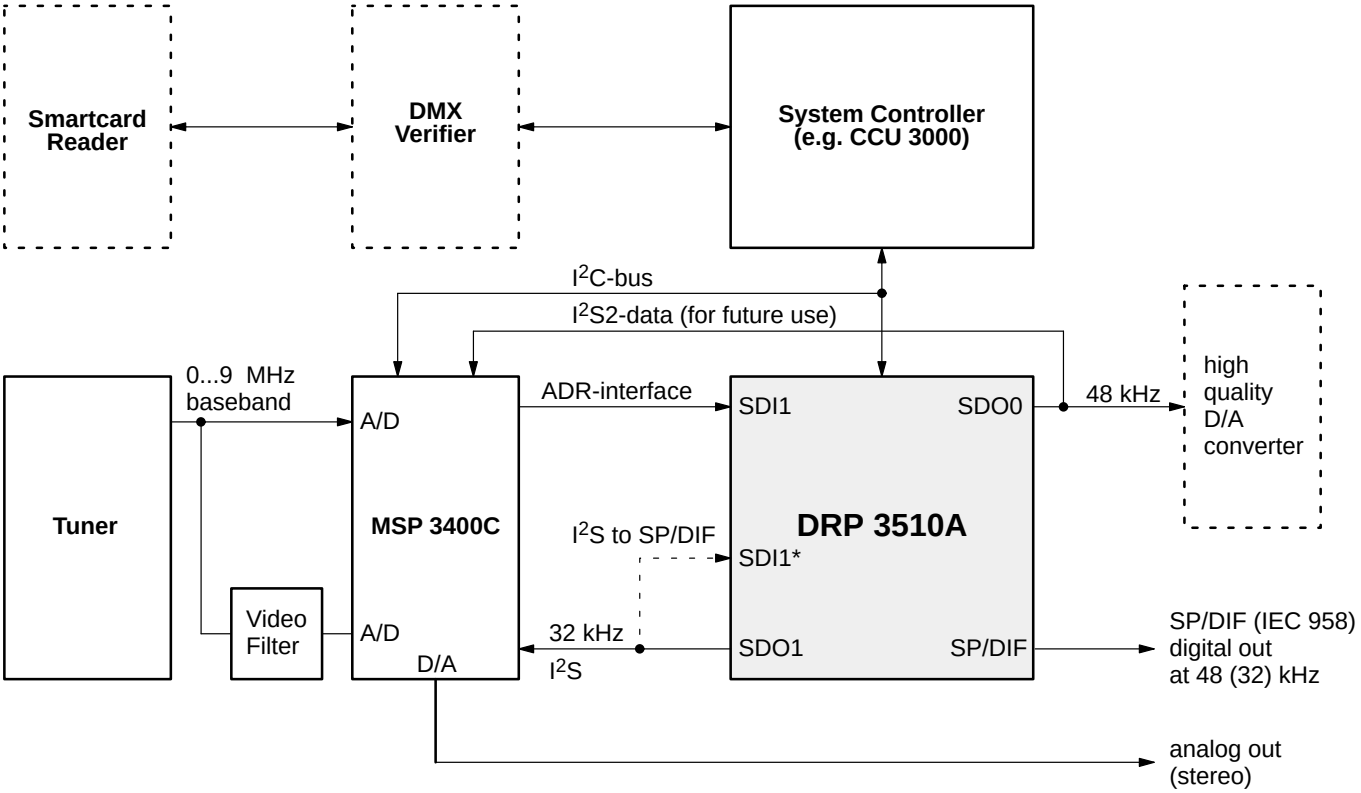


Fig. 4–1: ADR/DMX decoder application

5. Clock Concepts

In order to support various applications and board layouts, different clock concepts are supported. Each of the described clock concepts has its advantages. The digital nature of the ADR bit stream forces the decoder IC to synchronize its clock frequency to the symbol rate of the incoming signal. Both the MSP and the DRP clock have to be synchronized, but only the DRP does the timing recovery. The MSP clock is synchronized indirectly with a PLL that locks onto the I^2S (SO1) signal from the DRP. Thus, the I^2S feedback connection is mandatory in all ADR applications. See the application recommendations (section 11.) for further details.

5.1. Both MSP and DRP with own crystal running at a 18.432 MHz frequency

The “two crystal mode” is the standard application for the ADR-chip set. Two identical crystals may be used. This mode is preferable in all applications where a considerable physical distance between both ICs is given by the actual board layout.

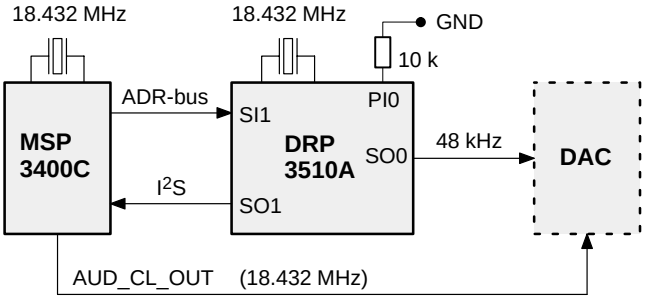


Fig. 5–1: Two crystal mode

5.2. MSP running with a 18.432 MHz crystal, DRP running with a 24.576 MHz crystal

The “two crystal mode” with a 18.432 and a 24.576 MHz crystal leads to a smaller power dissipation (about 10% smaller) for the DRP and makes it possible to derive the oversampling clock for the optional 48 kHz DAC directly from the DRP (position II of the switch in Fig. 5–2).

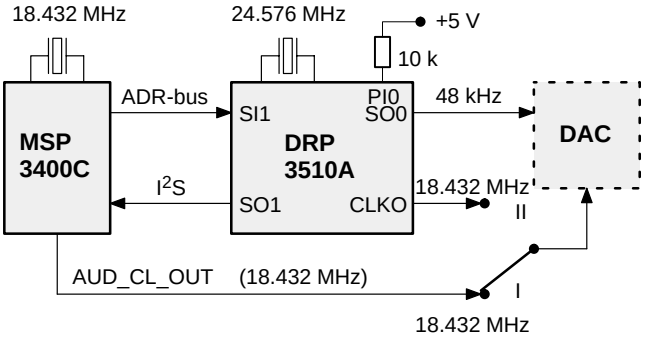


Fig. 5–2: Two crystal mode with 18.432 and 24.576 MHz crystal

Table 5–1: Clock concepts

	Clock Concept			
	5.1.	**5.2. (I/II)**	**5.3.**	**5.4.**
Processor clock	39.936 MHz	36.864 MHz	36.864 MHz	39.936 MHz
Timing recovery control register (see 9.6.)	no action required	no action required	no action required	$200
Comment		less power consumption	MSP crystal is omitted, best C/N, low crystal spec., less power consumption	4-bit DAC (48 kHz) is required

5.3. DRP running with a 24.576 MHz crystal, MSP receives its clock from DRP

In this “single crystal mode”, the MSP clock is taken from the DRP. This avoids any problems that may arise due to frequency deviations of the crystals. The DRP-PLL works directly without any effects caused by the MSP. So the best C/N performance can be reached. The 24.576 MHz crystal leads to a smaller power dissipation (about 10% smaller) for the DRP. This is the most cost effective solution, because the crystal specification is very low. The oversampling clock for the optional 48 kHz DAC comes directly from the DRP. The NICAM mode of the MSP 3410D is not useable. If the system in this mode is running without an ADR-carrier at the input, the clock will slowly drift to its maximum deviation. The DRP clock can be restored either to its default value by writing the value ‘0’ into the clock-deviation register (see 9.5.) or better with an initialization value according to section 11.5. After a simultaneous hardware reset of MSP and DRP, it is necessary to give the MSP a software reset using an I^2C-command. A MSP software reset (via I^2C) is necessary after each reset (by hardware or by I^2C) of the DRP.

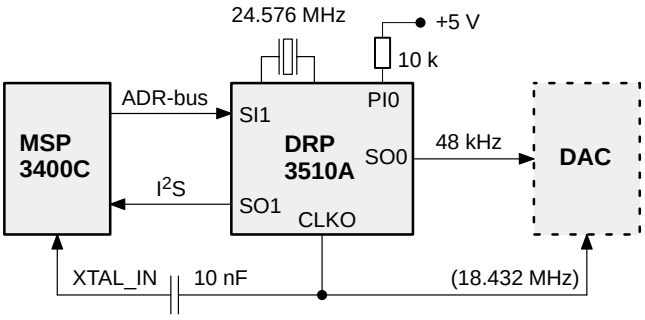


Fig. 5–3: Single-crystal mode with 24.576 MHz

5.4. DRP receives its clock from the MSP

In this “single crystal mode”, the DRP clock is taken from the MSP. This avoids any problems that may arise due to frequency deviations of the crystals. However, this mode leads to a more critical symbol-clock recovery. The reference clock of the DRP is generated by the MSP, which again is the base for the DRP system. This causes an integrating system behavior that has to be stabilized by changing some control circuit parameters (write $200 into timing recovery control register – see 9.6.). If the system in this mode is running without an ADR-carrier at the input, the clock will slowly drift to its maximum deviation. The DRP clock can be restored either to its default value by writing the value ‘0’ into the clock-deviation register (see 9.5.) or better with an initialization value according to section 11.5.

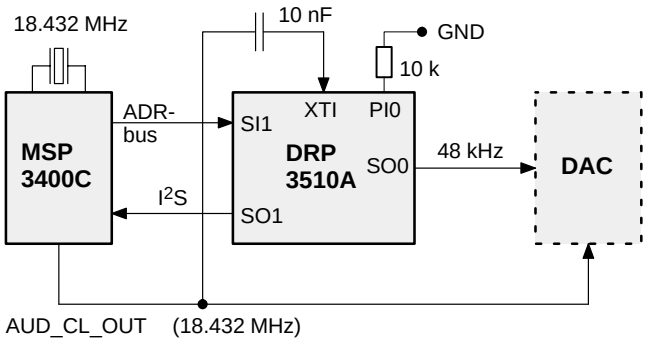


Fig. 5–4: Single crystal mode with 18.432 MHz

6. Interfaces

6.1. The ADR Input Interface

The ADR input lines SI1C, SI1D, and SI1I are designed as a direct interface to the MSP. These lines transport some preprocessed channel-data from the MSP, which are directly used for the channel decoding within the DRP (see the MSP 3400C/D data sheet for connecting the MSP with the DRP). If the Layer 2 mode is selected, the ADR interface expects Layer 2 data instead of ADR data. The format for the L2 data stream is shown in Fig. 6–1. Short interruptions of the data stream are allowed (< 5 ms). However, the mean input data rate must correspond to the data rate that is coded in the MPEG bit stream. It is possible to route the input to SDI1* by using the input selection register (see 9.12.).

6.2. The SDO0 Interface

The SDO0 interface passes the decoded 48 kHz audio signal e.g. to a high quality D/A converter. The serial format generates 2*32 bits for stereo audio samples on the data line SO0D, a word strobe SO0I, and a serial clock at the SO0C line. The first 18 bits of each mono-sample contain valid data, bit 19 and bit 20 are always set to zero. The 12 trailing bits are determined by the content of the SO0AUXA (left) and SO0AUXB (right) registers. Some high quality DACs do need an oversampled clock signal. If the DRP is working with a 24.576 MHz crystal, the oversampled clock may be taken from the CLKOUT pin of the DRP. If working with a 18.432 MHz crystal, the oversampled clock has to be taken from the MSP-clock-out. In the 18.432 MHz MSP single crystal mode, the external DAC should not be a 1-bit converter. This is to prevent clock jitter effects caused by the timing recovery.

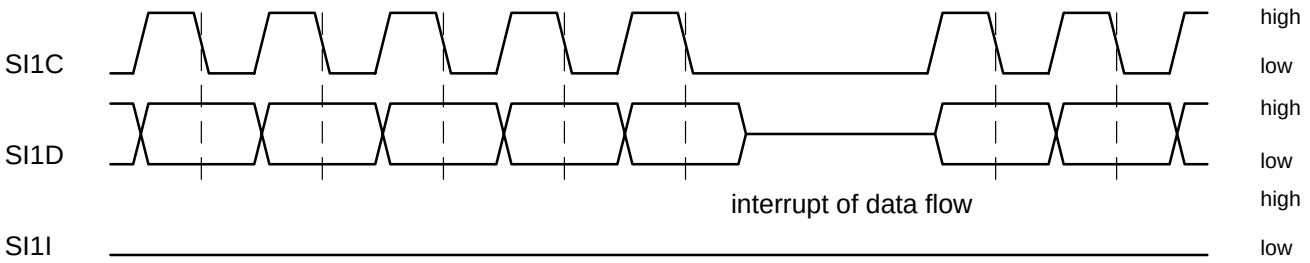


Fig. 6–1: Schematic timing of a MPEG Layer2 input data stream

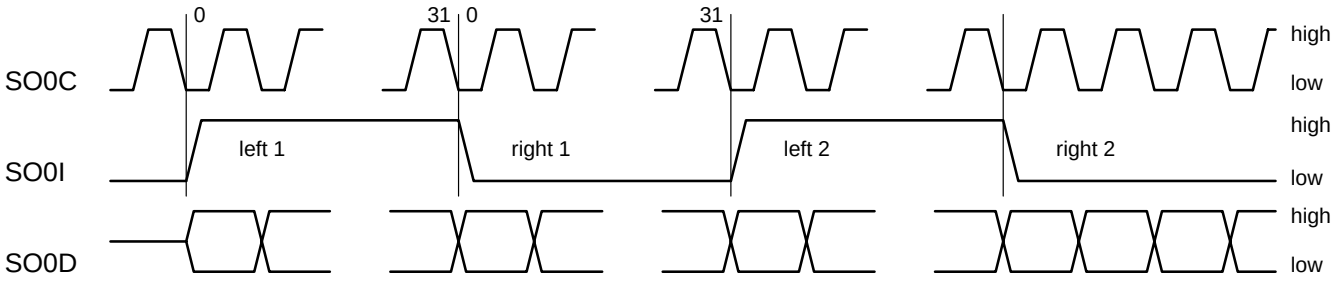


Fig. 6–2: Schematic timing of the SDO0 output interface

6.3. The SDO1 Interface

The SDO1 interface sends a decoded 32 kHz audio signal back to the MSP. The 32 kHz signal is generated via an internal high quality sample rate converter, which is perfectly matched to the performance of the MSP DACs. The cutoff frequency now is reduced to approximately 15 kHz. The signal of most of the free to air ADR-stations, however, does not exceed this cutoff frequency. The serial format generates 2*16 bits for stereo audio samples on the data line SO1D, a word strobe on the SO1I, and a serial clock at the SO1C line. This offers the opportunity to use the MSPC DACs for analog output. This connection to the MSPC is obligatory for every application, even if it is not intended to use the MSPC DACs. This is due to the fact that the clock synchronization between DRP and MSP uses this connection. The timing of the SDO1 interface is shown in Fig. 6–3.

6.4. The PIO Interface

The PIO interface can be used in two different modes. In the standard mode, the PIO lines PI0..PI3 are used to select the crystal frequency or to switch between different applications; and the PI12..PI19 lines are used as signalling outputs or serial interface pins (see section 3.2.). In a second mode, the DMA mode (direct memory access), the internal MPEG Layer 2 data stream (after descrambling but before decoding) is provided on the PIO lines PI12..PI19.

6.4.1. General Purpose PIO Mode

The general purpose PIO mode is selected after reset. In this mode, the PIO-lines have the functionality as described below. The PI0 and PI3 pins are only read out after a reset of the DRP.

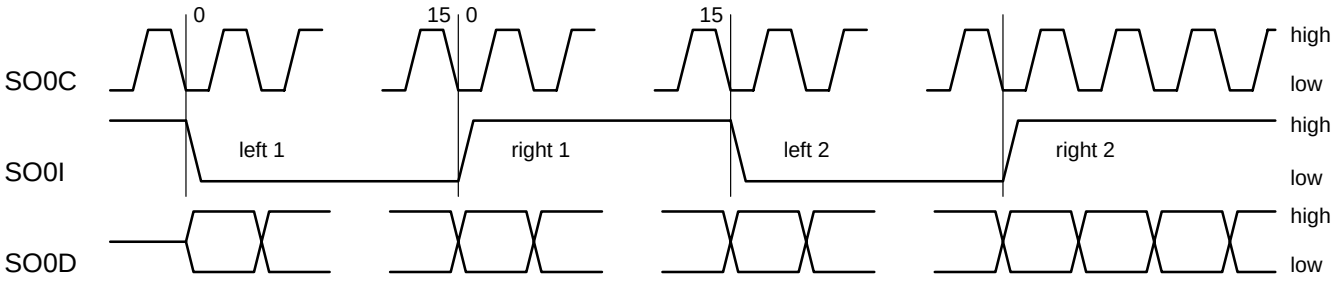


Fig. 6–3: Schematic timing of the SDO1 output interface

Table 6–1: Functionality of the PIO mode

	PI0	PI1	PI2	PI3	PI14	PI15	PI16	PI18	PI19
	crystal select			Mode select	SI1D*	SI1I*	SI1C*	CRCE	$\overline{FSI}$ (def. mode)
0	18.432			ADR	Alternative input lines (for example: I^2S to SP/DIF conversion in combination with downloaded software)			no CRC error	anc.data available
1	24.576			L2 decoder				CRC error	anc.data invalid

6.4.2. PIO-DMA Mode

The PIO-DMA mode is selected by setting the corresponding bit in the main configuration register 96. The PIO-DMA mode gives access to the undecoded data, which are simultaneously sent to the integrated MPEG Layer 2 decoder. In this mode, PIO lines PI0..PI3 and PI12..PI19 are switched to output. The PIO lines PI12..PI19 will give an 8-bit parallel access to the bit stream data. The data is always sent in packets of 16 bytes every 0.667 ms. The data are 8-bit aligned with MSB first (at position PI19). The MPEG data are aligned in such a way that the first bit of the MPEG header is always positioned at the MSB (PI19) of the 8-bit word. In order to read out the data stream, a special handshake protocol must be used (see Fig. 6–4).

The data transfer is started after the EODQ-pin of the DRP is set to an active state. After checking this, the controller requests data by activating the PR-line. The DRP asserts that the first data word is placed on the bus by generating a negative strobe impulse on $\overline{\text{PRTW}}$. Now, the controller may read the data word, and subsequently, it may request the next byte by activating the PR-line again. This procedure will be repeated 16 times. After the 17th PR impulse of the controller, the EODQ signal of the DRP will be activated, which indicates that the transfer of one data block has been finalized. The data for one 16-byte block is transmitted in 0.$\overline{6}$ms. However, the complete protocol should be executed in less than 0.5 ms to avoid data loss. A description of timing details can be found in section 12.1. This PIO-DMA mode will not work in the E4 version (see also section 13).

6.5. The SP/DIF Interface

The SP/DIF interface generates a 48, 44.1, or 32 kHz digital signal conforming to the IEC 958 consumer standard. In ADR mode, only 48 kHz sampling frequencies are generated. The interface definition covers the data stream and the physical timing specifications of the data transmission. The transmission is done via the “biphase-mark” code (Fig. 6–5).

The SP/DIF signal consists of 32-bit subframes. The first 4 bits are used for the sync impulse (Preambles). There are three different sync signals: The first subframe normally starts with preamble “X”. However, the preamble changes to preamble “Z” once every 192 frames. “Z” also indicates the block begin, which is used to organize the channel status information. The second subframe always starts with preamble “Y”. (see Fig 6–7). Two subframes form one frame, 192 frames are collected into one super-frame (or block). The preamble is followed by 4 auxiliary bits, which are not used in this application (forced to 0), and 20 data bits. A subframe will be completed with the validity bit, user bit, channel status bit, and parity bit (see Fig 6–6).

6.6. Copy Protection

The copy protection mode is set either according to the incoming MPEG bit stream or explicitly to “no copy allowed” regardless of the copy protection setting of the MPEG bit stream. The copy protection mode is selectable by setting bit 8 in the main configuration register. In the default mode (bit 8 = 0), the copy bit of the MPEG bit stream that is set by the service provider is directly evaluated to set the copy protection within the SPDIF output bit stream. If copy protection is coded in the MPEG header, one can record the program, but a further digital copy of the recorded material is not allowed. If no copy protection is coded in the MPEG header, a digital copy is allowed. The copy protection can be forced regardless of the copy protection setting in the MPEG bit stream by setting the main configuration register (bit 8 = 1).

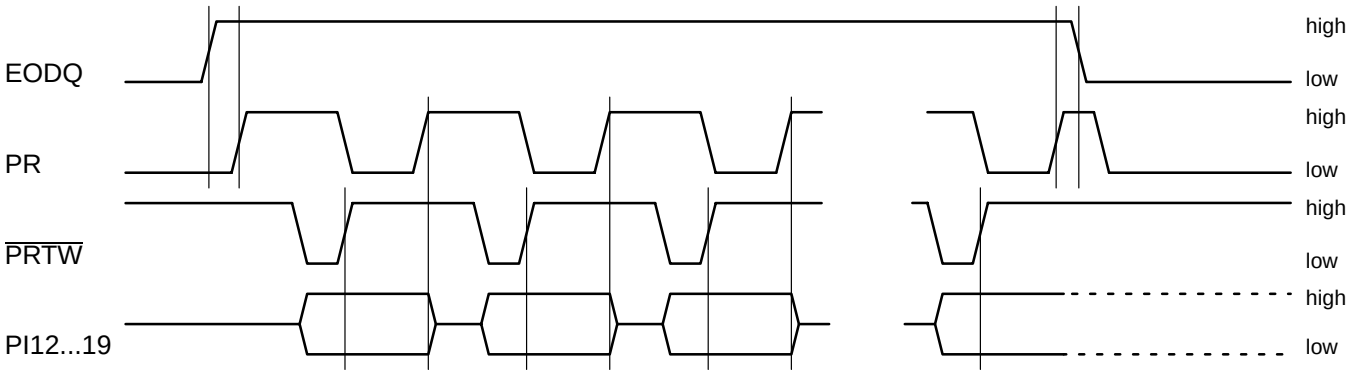


Fig. 6–4: Handshake protocol for getting MPEG data via PIO-DMA

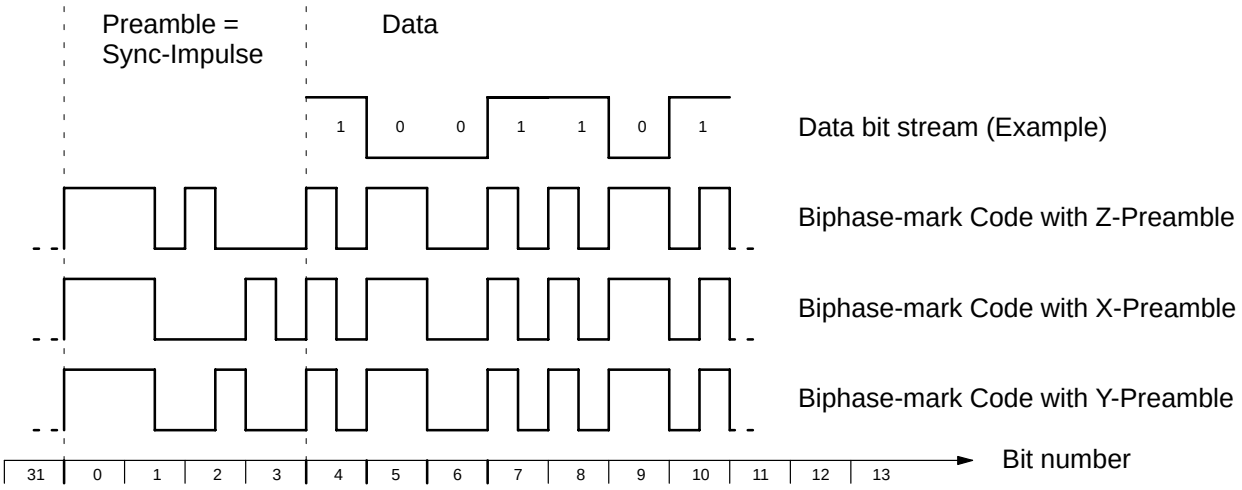


Fig. 6–5: Preamble and biphase-mark code specification (polarity may be changed)

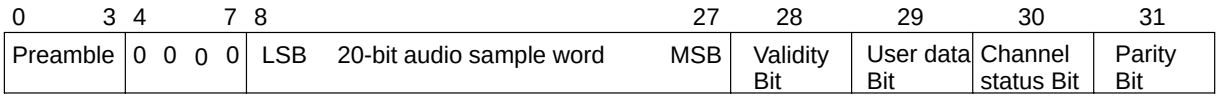


Fig. 6–6: Subframe format

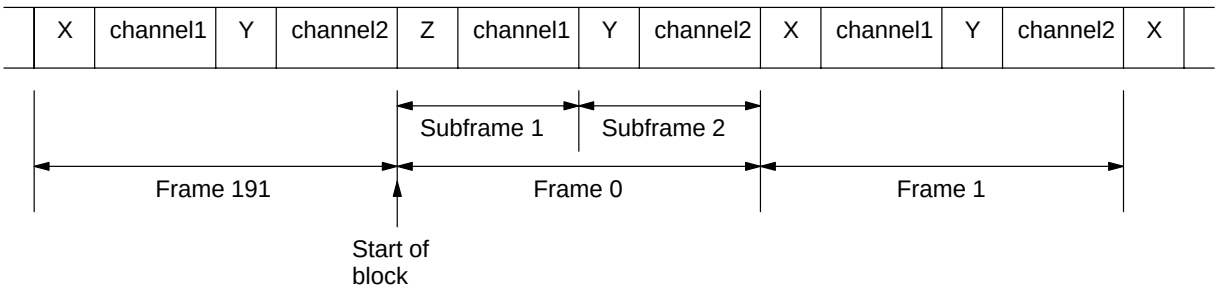
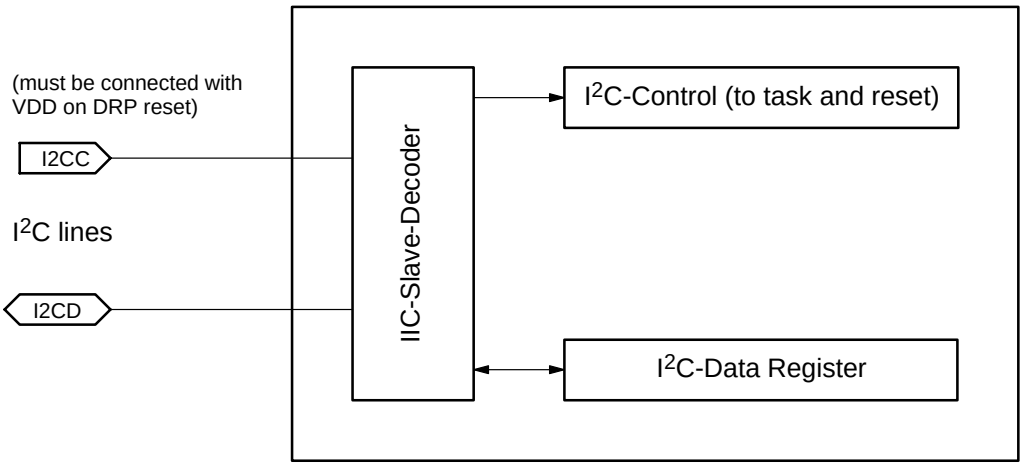


Fig. 6–7: Frame format

7. The I²C Interface



Device address: 1101010X ($D4 (dev_write), $D5 dev_read))

Slave-Subaddresses:	01101000 ($68)	subaddress write
	01101001 ($69)	subaddress read
	01101010 ($6A)	control

Fig. 7–1: Schematic diagram of the I²C-Bus-Interface of the DRP

7.1. The I²C-Data Register

The I²C-Data Register is used to communicate with the internal firmware of the DRP. It has a length of 16 bits. The data transfer is done with the MSB first. The following table shows the bit assignment used in this document.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
msb															lsb

7.2. The I²C-Control Register

The I²C-Control Register is used to set the tasks to switch between different operating modes and to generate a hardware reset.

If the reset bit is set to “1”, the DRP will stay in the “reset” state. This I²C reset will affect all blocks of the DRP but not the I²C-interface itself. Thus, writing a new word into the control register with the reset bit 8 cleared, will restart the processor. If the task bits T0...T3 are set, the corresponding tasks in the DRP are set permanently. The bits C4...C7 must always be set to “0”. If no bit is set, the DRP will work in its default mode, which is ADR-decoding. Task 3 corresponds to the Layer 2 only decoder.

C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
reserved bits							Re-set	0	0	0	0	T3	T2	T1	T0

7.3. The I²C Protocol

A data transfer via I²C is always initiated by an external controller with a start condition on the I²C bus. Then, the controller sends the device address and the subaddress. The value of the subaddress specifies the direction of the following data transfer. The subaddresses $68 and $6A indicate a transfer from the controller to the DRP, the subaddress $69 indicates a transfer from the DRP to the controller. The transfer is continued until a stop condition is transmitted by the controller.

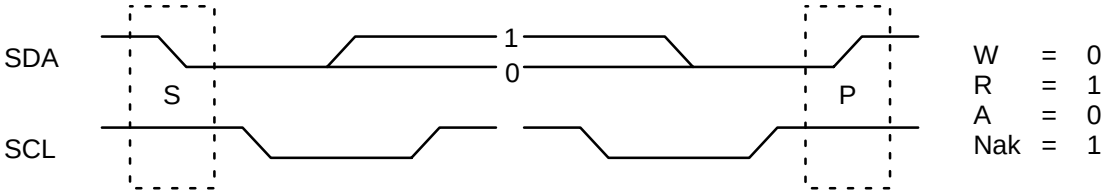


Fig. 7–2: Timing of start (S) and stop (P) condition of the I²C protocol

7.3.1. Controller Writes to the DRP Control Register

S	dev_write ($D4)	A	control_adr ($6a)	A	control_high (8)	A	control_low (8)	A	P

Fig. 7–3: Writing a control word into the control register

7.3.2. Controller Writes to the DRP Data Register

S	dev_write ($D4)	A	data_write ($68)	A	data_high (8)	A	data_low (8)	A	P

Fig. 7–4: Writing a 16-bit word into the data register

7.3.3. Controller Reads from the DRP Data Register

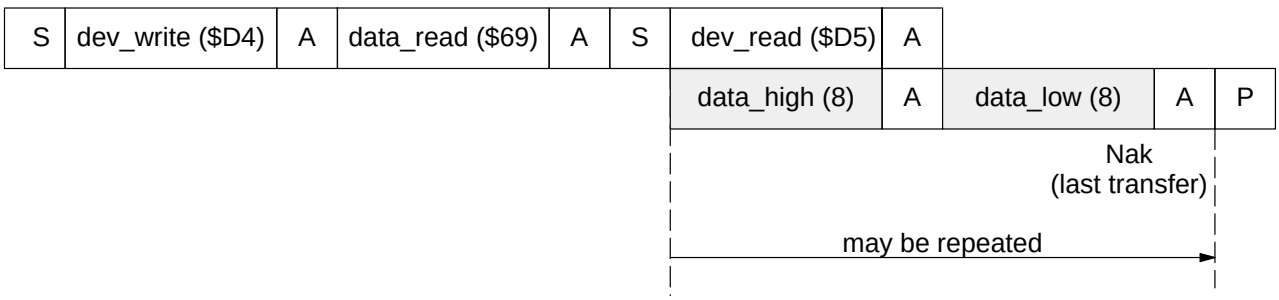


Fig. 7–5: Reading 16-bit data word(s) from the data register

7.4. The I²C Commands

The following commands are used to communicate with the DRP-firmware. The commands are executed by the DRP during the normal operation without any interruptions of the audio signal. These I²C commands do allow an external system controller to access all internal states, RAM contents, and even the internal hardware control registers. This may be very useful for special purpose application and non standard operation modes. Note: Writing values into not documented internal DRP registers or RAM-cells may corrupt the decoding process and may lead to unpredictable processor states, which can be left only by a hardware reset of the whole system.

The description of the various I²C commands uses the following formalism: A value is split into nibbles, which are numbered beginning with 0 for the least significant nibble. The data values or the nibbles are written in hexadecimal notation indicated by a preceding $ character. A hexadecimal number is written, for example, as d=$17C63. The 5 nibbles of this number are d0=$3, d1=$6, d2=$C, d3=$7, d4=$1. Register addresses are called **r**, data values are called **d**, addresses **a,** and a count value is called **n**. If a fixed number is to be used, it is listed directly preceded by a $-sign.

7.4.1. Write into a DRP Register

S	dev_write ($D4)	A	data_write ($68)	A	$9 r1	A	r0 d0				
				A	d4 d3	A	d2 d1	A	P		

Fig. 7–6: Write a 20-bit value **d**=(d4,d3,d2,d1,d0) into register **r** = (r1,r0)

The DRP has an address space of 256 registers, 128 of them in the D0-area and 128 in the D1-area. Some of the registers are direct control inputs for various hardware blocks, others do control the internal program flow. In the next section, those registers that may be changed by the system controller are described in detail.

∆ *Writing random values into undocumented registers may corrupt the execution of the program.*

7.4.2. Default Read Command

S	dev_write ($D4)	A	data_read ($69)	A	S	dev_read ($D5)	A				
						status	A	index	Nak	P	

Fig. 7–7: Default read of a 16-bit word (**status** and **index**) from the DRP

The status and index values are described in section 8.1.

7.4.3. Read From a DRP Register

1. send command

S	dev_write ($D4)	A	data_write ($68)	A	$d r1	A	r0 $0	A	P

2. get register value

S	dev_write ($D4)	A	data_read ($69)	A	S	dev_read ($D5)	A			
						d3 d2	A	d1 d0	A	
						$xx	A	$x d4	Nak	P

Fig. 7–8: Reading a 20-bit value from a DRP register

7.4.4. Get ADR Data

1. send command

S	dev_write ($D4)	A	data_write ($68)	A	$60	A	offset count	A	P

2. get data

S	dev_write ($D4)	A	data_read ($69)	A	S	dev_read ($D5)	A			
						status	A	index	A	
						adr0	A	adr1	A	
						adr2	A	adr3	A	
						adr4	A	adr5	A	
						adr6	A	adr7	A	
						adr8	A	adr9	A	
						adr10	A	adr11	A	
						adr12	A	adr13	A	
						adr14	A	adr15 (ctrl 0)	A	
						adr16 (ctrl 1)	A	adr17 (ctrl 2)	Nak	P

offset: first value to be read ($0...$9)
count: number of words to be read ($1...$a)

Read the complete data field:
offset = 0, count = $a

Read only control data:
offset = 8, count = 2

Fig. 7–9: Reading the status, index, and the 18 bytes of ADR-data from the DRP

The 18 bytes of the ADR data will be updated every 24 ms. The content of this data field is documented in the ADR-specification. These data are already deinterleaved and error corrected. The last three bytes do always keep the control data. The meaning of the first 15 bytes may change due to different services. In order to optimize the access to the ADR data, a simple selection mechanism has been implemented where the offset and the number of word to be read could be selected. It is important that this command is always completed, i.e. the number of words passed by “count” to the DRP has to be read by the controller, otherwise the operation system may crash. The MSB of control byte 1, which indicates that the auxiliary and RDS data in the frame are complemented, will be processed internally according to the “free to air” standard. Thus, this bit is always set to

zero, indicating that the inversion of the control data must not be done by the controller. In case of DMX, the meaning of the MSB of control byte 1 is inverted, so that the controller always has to complement the auxiliary and RDS data.

7.4.5. Write DMX Data

S	dev_write ($D4)	A	data_write ($68)	A	$50	A	$00	A	
					dmx1	A	dmx0	A	
					dmx3	A	dmx2	A	
					dmx5	A	dmx4	A	
					dmx7	A	dmx6	A	P

Note: 8 dmx bytes (dmx0...dmx7) are received from the verifier IC. When writing these bytes to the DRP, start with dmx1 before writing dmx0 etc.

Fig. 7–10: Send 8 bytes to DRP for DMX data decryption

7.4.6. Write Data into the D0-Memory of the DRP

S	dev_write ($D4)	A	data_write ($68)	A	$a0	A	$00	A	
					n3 n2	A	n1 n0	A	*count 'n'*
					a3 a2	A	a1 a0	A	*address 'a'*
					d3 d2	A	d1 d0	A	*data 'd'*
					$00	A	$0 d4	A	
					repeat n times				
					d3 d2	A	d1 d0	A	
					$00	A	$0 d4	A	P

n3..n0 = number of words
a3..a0 = start address in drp memory
d4..d0 = data value

Fig. 7–11: Write data to the D0 area

Writing data into memory areas may be used for controlling the program execution (see section 8.) and for downloading purposes. Before downloading, it is recommended to freeze the program execution. Otherwise, the internal program may override the downloaded values instantly.

Δ *Writing data into undocumented memory areas may corrupt the execution of the internal program.*

7.4.7. Write Data into the D1-Memory of the DRP

S	dev_write ($D4)	A	data_write ($68)	A	$b0	A	$00	A		
					n3 n2	A	n1 n0	A		*count 'n'*
					a3 a2	A	a1 a0	A		*address 'a'*
					d3 d2	A	d1 d0	A		*data 'd'*
					$00	A	$0 d4	A		
					repeat n times					
					d3 d2	A	d1 d0	A		
					$00	A	$0 d4	A	P	

n3..n0 = number of words
a3..a0 = start address in drp memory
d4..d0 = data value

Fig. 7–12: Write data to the D1 area

Writing data into memory areas may be used for controlling the program execution (see section 8.) and for downloading purposes. Before downloading, it is recommended to freeze the program execution. Otherwise, the internal program may override the downloaded values instantly.

∆ *Writing data into undocumented memory areas may corrupt the execution of the internal program.*

7.4.8. Read Data from the D0-Memory of the DRP

1. send command

S	dev_write ($D4)	A	data_write ($68)	A	$e0	A	$00	A		
					n3 n2	A	n1 n0	A		*count 'n'*
					a3 a2	A	a1 a0	A	P	*address 'a'*

n3..n0 = number of words
a3..a0 = start address in drp memory
d4..d0 = data value

2. get data

S	dev_write ($D4)	A	data_read ($69)	A	S	dev_read ($D5)	A			
						d3 d2	A	d1 d0	A	*data 'd'*
						$00	A	$0 d4	A	
						repeat for n data values				
						d3 d2	A	d1 d0	A	
						$00	A	$0 d4	Nak	P

Fig. 7–13: Read 20-bit data from the D0-memory of the DRP

7.4.9. Read Data From the D1-Memory of the DRP

1. send command

S	dev_write ($D4)	A	data_write ($68)	A	$f0	A	$00	A			
					n3 n2	A	n1 n0	A	*count 'n'*		
					a3 a2	A	a1 a0	A	P	*address 'a'*	

n3..n0 = number of words
a3..a0 = start address in drp memory
d4..d0 = data value

2. get data

S	dev_write ($D4)	A	data_read ($69)	A	S	dev_read ($D5)	A				
						d3 d2	A	d1 d0	A	*data 'd'*	
						$00	A	$0 d4	A		

repeat for n data values

						d3 d2	A	d1 d0	A		
						$00	A	$0 d4	Nak	P	

Fig. 7–14: Read 20-bit data from the D1-memory of the DRP

7.4.10. Freeze

S	dev_write ($D4)	A	data_write ($68)	A	$00	A	$00	A	P

Fig. 7–15: The Freeze command should be executed before download of the new code to avoid noise signals at the output interfaces. Before using the freeze command, it is recommended to mute the output.

7.4.11. The Run Command

S	dev_write ($D4)	A	data_write ($68)	A	a3 a2	A	a1 a0	A	P

Fig. 7–16: The Run command starts the execution at the program address **a** = (a3,a2,a1,a0).

8. Internal Registers and Memory Areas

The following section describes internal registers and memory areas, that are accessible by the controller, in order to control or watch the internal operation of the DRP.

8.1. Default Read (Index and Status)

If a value is read from the DRP without a previously given command, the 16-bit index and status value is returned by default. The index value can be used in a polling loop to synchronize the system controller with the transmitted Layer 2 frame. The lower byte of the index/status always contains an odd number (if the DRP is decoding) and is incremented by 2 after each update of the ADR-data block. The upper byte indicates the status of the decoder as described in Table 8–1.

8.2. Digital Volume and Channel Mapping (Write)

Four memory cells in the D1 area are used to control the digital volume of the DRP output lines. These memory cells simply keep coefficients the stereo input signals are multiplied with. These coefficients are represented in a 20-bit fixed point notation (e.g. $80000 = –1.0 or $20000 = 0.25.) In order to achieve the corresponding fixed point value, divide the hex-value read from a register by 524288 = $80000. The 4 coefficients are located in the memory cells. This mapping may be used for volume control, channel mapping, and for special stereo bandwidth effects. The default coefficients are negative in order to compensate a previous signal negation.

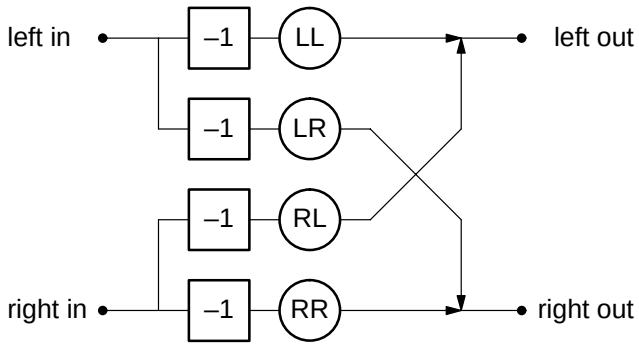


Fig. 8–1: Digital volume matrix

Table 8–1: Index and status word

C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
M	x	x	J	W	S	F	E	**i7**	**i6**	**i5**	**i4**	**i3**	**i2**	**i1**	L

Bit Number	Name	Value	Description
0	L	0	not counting, not decoding
0	L	1	synchronized and counting
1..7	I(1..7)	0..127	index (counts module 128), increment after each ADR-data update
8	E	1	error in ancillary data field (probably corrected)
9	F	1	scale factor CRC-error
10	S	1	carrier detect (does not work properly in E4 – see bit0 for this purpose)
11	W	1	weak carrier (does not work properly in E4 – see the AGC register instead)
12	J	1	MPEG signal does not use 50 µs preemphasis
13	x	0	
14	x	0	
15	M	1	MPEG Layer 2 CRC-error

Table 8–2: Digital volume matrix coefficients

Memory Location:	**D1:$120**	**D1:$121**	**D1:$122**	**D1:$123**
Cell Name	LL	LR	RL	RR
Default (stereo)	–1.0 ($80000)	0	0	–1.0 ($80000)
Dual Ch. (left)	–1.0 ($80000)	–1.0 ($80000)	0	0
Dual Ch. (right)	0	0	–1.0 ($80000)	–1.0 ($80000)
Description	maps left input to left output	maps left input to right output	maps right input to left output	maps right input to right output

9. Handling of the DRP via Internal Registers

The execution of the firmware ADR-decoder in the DRP can be monitored by reading internal registers. Writing to registers allows a modification of the internal operation, which may be useful for specific applications. All registers in the DRP are accessible from the controller via I^2C bus. The most useful registers that may be accessed by the controller are listed in this paragraph. This allows detailed control and monitoring of many internal processes within the DRP for any controller. Writing into registers that are not listed below is possible, but it may cause unpredictable results or even a crash of the DRP program. Many of the readable register values may change very rapidly. Smoothing, for example, by using a sliding average technique may be helpful.

9.1. The Internal Fixed Point Number Format

In many cases it is useful to convert the register or memory values “v” into a fixed number representation “r”. This is done easily by using the following algorithm:

```
if (v ≥ 524288) {
v = v – 1048576;
}
r = v / 524288.0;
```

Vice versa, a real number “r” in the range from –1.0 to 1–524287/524288 can be converted into the DRP 20-bit two’s complement representation “v” by using the algorithm:

```
v = r*524288.0 + 0.5;
if (v<0) {
v = v + 1048576;
}
```

9.2. Main Configuration Register 96 (Write)

The main configuration register controls the operation of the ADR decoder firmware.

C 19	C 18	C 17	C 16	C 15	C 14	C 13	C 12	C 11	C 10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
FR	G2	G1	G0	r	r	r	r	PD	M1	r	CP	AI	FS	SP	C	J	r	Q	D

Bit Number	Name	Value	Description
0	D	0	no decryption
	D	1	do DMX-decryption
1	Q	0	18.432 MHz crystal is used (must be equal to PI0 setting)
	Q	1	24.576 MHz crystal is used
2	r	0	reserved bits must always be set to “0”
3	J	0	do digital deemphasis, if requested by MPEG L2-header
	J	1	no deemphasis
4	C	0	use SP bit to enable scalefactor protection
	C	1	use transmitted bit stream info to enable scalefactor protection
5	SP	0	if (C=0), disable scalefactor protection
	SP	1	if (C=0), always enable scalefactor protection
6	FS	0	set FSI automatically (see section 11.3.)
	FS	1	disable setting FSI (FSI is low)
7	AI	0	default ancillary data handling (ADR: deinterleaving, L2: no deinterl.)
	AI	1	invert default ancillary data handling (ADR: no deinterl., L2: deinterl.)
8	CP	0	use copy protection setting of MPEG bit stream
	CP	1	force copy prohibited (recording the program is allowed, not copying)
9	r	0	reserved bits must always be set to “0”
10	M1	0	enable outputs
	M1	1	mute all outputs
11	PD	0	PIO used for CRC and FSI signals
	PD	1	disable FSI and CRC and send undecoded L2-bit stream to PIO
12...15	r	0	reserved bits must always be set to “0”

Bit Number	Name	Value	Description
18, 17, 16	G2 G1 G0		gain adjustment for the incoming ADR-data stream
	G2 G1 G0	100 101 110 111 000 001 010 011	–24 dB –18 dB –12 dB –6 dB 0 dB (default value) +6 dB +12 dB +18 dB
19	FR	1	force a restart (similar to a “soft-reset”)

9.3. AGC Register 115 (Read)

The DRP automatic gain control can be watched by reading the AGC register (115). The AGC value indicates if the gain of the single ADR-carrier coming from the MSP has a sufficient value. For proper operation, the AGC value should be somewhere between $a0000 (= –0.75) and $e0000 (= –0.25). If the AGC value is constantly showing $80000, the AGC is out of its control range. This indicates that the video carrier of the MSP input signal is not suppressed sufficiently or that the IF input signal does not have a sufficient level. If the value is too small, the DRP input gain should be reduced by adjusting the bits G2, G1, G0 in the main configuration register.

9.4. Viterbi Min-distance Register 210 (Read)

The viterbi min-distance register content gives information about the bit error rate of the decoded signal. A smoothing of subsequent viterbi distance values will stabilize the result. If the viterbi min-distance is less than 5000, the channel quality is excellent. Larger values indicate worse signal quality. Bit errors can be expected, if the mean value of the viterbi min-distance exceeds **5300**. The value given by the viterbi min-distance register is only valid if the AGC is working properly (see section 9.3.). The AGC register value should not be at its limitation at **$8000**.

9.5. Clock-deviation Register 244 (Read, Write)

The clock deviation register holds a value that indicates the clock deviation of the DRP-clock, which is set by the timing recovery algorithm with respect to the crystal reference. If this value is set to ‘0’, the DRP-clock exactly mirrors the XTI (crystal) clock. A negative value indicates that the DRP-clock is slower, a positive clock indicates a higher internal clock frequency. The output clock frequency can be derived from the clock-deviation register value by the following formula, where δf stands for the fixed point representation of the clock deviation register content.

f_c = (39936 + 37.1613*δ*f*) *kHz*
for f_q = 18.432 *MHz;* –1.0 < δ*f* <+1.0

f_c = (36684 + 33.0323*δ*f*) *kHz*
for f_q = 24.576 *MHz;* –1.0 < δ*f* <+1.0

9.6. Timing Recovery Control Register 168 (Write)

If the DRP is running with an 18.432 MHz clock, the crystal may be omitted, and the AUD_CL_OUT (signal of the MSP, which is a 18.432 MHz clock) may be connected via 10 nF with the XTI input signal of the DRP. However, this mode of operation does affect the timing recovery of the system, which now has different behavior than using a separate crystal for the DRP. In order to avoid an instable timing recovery, the value $200 has to be written into the register 168 after each reset of the DRP.

9.7. SP/DIF Configuration Register 83 (Write)

The SP/DIF configuration register SP0C can be used to disable the SP/DIF output for special copy protection. This is done by writing the value $80 into this register. The only way of enabling the SP/DIF output again, is a reset.

9.8. SDO0 Configuration Register 67 (Write)

This SDO0 configuration register can be used to control the format of the outgoing I^2S signal. For some DACs, it is necessary to delay the data values by one clock vs. the wordstrobe signal. This can be achieved by writing the value $821 into this register (Default content of the register $21).

9.9. SO0AUXA Register 69 (Write)

The 12 LSBs of the register content of this register are placed into the 12 trailing bits of the left word of the I^2S data stream. These bits can be used to send control information to some DACs.

9.10. SO0AUXB Register 70 (Write)

The 12 LSBs of the register content of this register are placed into the 12 trailing bits of the right word of the I^2S data stream. These bits can be used to send control information to some DACs.

9.11. SDI1 Input Configuration Register 187 (Write)

For Layer 2 decoding, some applications do generate an inverted clock signal with respect to the data. The inversion can be compensated by writing the value $1004 into this register.

9.12. SDI1 Input Selection Register 79 (Write)

Switching between the standard SDI1 input (which is the default) and the alternative SDI1* input is possible. The alternative input is selected by writing a '2' into this register. Writing a '0' into the register will reset the input to the SDI1 lines.

9.13. Actual MPEG Header Register 117 (Read)

Register 117 contains a mirror of the actual MPEG header that has been read out from the incoming bit stream.

Table 9–1: MPEG status bits

Bit Number	Name	Comment
19	ID	always 1
18, 17	layer	10 = Layer 2
16	protection bit	0 = CRC protection included 1 = no CRC protection included
15, 14, 13, 12	bit rate index	1010 for 192 kbit/s
11, 10	sampling frequency	01 = 48 kHz
9	padding bit	only for 44.1 kHz f_S
8	private bit	for private use
7, 6	mode	00 = stereo, 01 = joint stereo, 10 = dual– , 11 = single channel
5, 4	mode extension	controls bit allocation for subbands
3	copyright	0 = no, 1 = copyright protected
2	original/copy	0: copy, 1: original
1, 0	emphasis	should be 00 (no preemphasis) or 01 (50/15 µs)

10. Downloading of Programs

Alternative software modules can be downloaded to the DRP. The downloaded programs are either available by Micronas or they can be developed by using the Micronas MASC 3500 software development package. The download can easily be done via the I^2C bus. Thus, additional functionality may be added to the DRP even if kept in the original ADR-application. Download modules are or will be available for:

– I^2S to SP/DIF conversion

– test signal generation

– Dolby Prologic

– Panorama Sound

– concert hall effects

The download procedure is done the following way:

1. Mute the audio outputs
2. Freeze the operation
3. Download the new program into the data memory
4. Start the new program with the “run” command at the start address of the downloaded program

Now, the DRP executes the new program. In order to switch back to normal operation, a simple “reset” is sufficient. After downloading, the original ADR or MPEG software will not be disabled in the new program. Tables and subroutines of the firmware are still available and executable. 0.75 kWord of program code and 1.25 kWord of data can be downloaded.

11. Application Recommendations

11.1. MSP 3400C Parameter Setting

For MSP related parameters, please refer to the MSP data sheet.

11.1.1. Input Gain and Differences between the MSP 3400C Versions C6 and C7

For new development of ADR receivers, the MSP 3400C-C7 or later versions are recommended. This version includes an additional gain factor in the ADR BUS interface output to the DRP, to enable optimal signal resolution also with ADR Stations in “Full Transponder Mode”.

In “Full Transponder Mode”, the frequency band normally used for video transmission is used by ADR carriers. With such signals, the level of one ADR carrier is much lower than with a TV program with, for example, 5 sound carriers. Note: The MSP 3400C-C7 and later versions are compatible to the MSP 3410D, regarding the ADR-Mode.

If the MSP 3400C-C7 or later versions, or the MSP 3410D are used, together with the DRP 3510A/E4 or later versions, the MSP AGC gain reference should be set to the value 20 dec (instead of 40 dec with the C6 version).

With this, clipping at the MSP input is avoided, especially with multi sound carrier programs. Normally, the clipping of the MSP input will cause no problems with ADR synchronization but will reduce the viterbi distance value. All other settings remain as with the MSP 3400C-C6 (see Table 11–1).

Together with these settings, it is recommended for the MSP 3400C-C7, to limit the overall composite IF input signal of the MSP to a peak-to-peak level of about 0.7 Vpp.

It is recommended that the controller software check the MSP version registers to set the MSP AGC gain reference according to the MSP version (see Table 11–2).

This version check can be done by reading Product and ROM Code only.

The MSP AGC reference gain is set to 20 dec if the product code is “0” and the the ROM code is smaller than “7”.

Table 11–1: Gain settings

Address	Meaning	with MSP 3400C-C6	with MSP 3400C-C7 and MSP 3410D[1)]
MSP AD_CV[6:1]	AGC gain reference	40 dec	20 dec
MSP AD_CV[7]	AGC on/off	1 = on	1 = on
MSP AD_CV[9]	Carrier mute	0 = off	0 = off
MSP Mode_Reg[12]	FIR Filter gain	0 = + 6 dB	0 = + 6 dB
DRP 3510A/E4... Register 96[18...16]	gain adjust	0 = 0 dB	0 = 0 dB
1) and all later versions			

Table 11–2: Version codes

Version Code	Address	Value for MSP 3400C-C6	Value for MSP 3400C-C7	Value for MSP 3410D
Hardware	1e hex high byte	3	3	1
Major revision	1e hex low byte	3	3	4
Product	1f hex high byte	**0**	**0**	**10 dec**
ROM	1f hex low byte	**6**	**7**	**34 dec**

11.1.2. Mode Register

Table 11–3: Control word ‘MODE_REG’: All bits are “0” after power-on-reset, settings for ADR mode

Bit	Function	Comment	Definition	Recom-mendation for ADR Mode
[0]	DMA_SYNC[1)]	Synchronization to DMA	0 : off 1 : on	0
[1]	DCTR_TRI	Digital control out 0/1 tristate	0 : active 1 : tristate	1/0
[2]	I2S_TRI	I^2S outputs tristate (I2S_CL, I2S_WS, I2S_DA_OUT)	0 : active 1 : tristate	0
[3]	I^2S Mode[1)]	Master/Slave mode of the I^2S bus	0 : Master 1 : Slave	1 (Slave)
[4]	I^2S_WS Mode	WS due to the Sony or Philips-Format	0 : Sony 1 : Philips	0 (Sony)
[5]	Audio_CL_OUT	switch Audio_Clock_Output to tristate	0 : on 1 : tristate	0 (if used)
[6]	not used		must be 0	0
[7]	FM1 FM2	MSPC-channel 1 mode		1
[8]	AM	MSPC-channel 1/2 mode	0 : FM 1 : AM	0
[9]	HDEV	High Deviation Mode (channel matrix must be sound A)	0 : normal mode 1 : high deviation mode	0
[10]	not used		must be 1	1
[11]	S-Bus Mode[2)]	mode of Pins S_CL and S_ID	0 : Tristate 1 : Active	1
[12]	FM2 FIR Filter Gain (FM2 = Ch1)		0 : Gain = 6 dB 1 : Gain = 0 dB	0 (+ 6 dB)
[13]	FM2 FIR Filter Coeff. Set (FM2 = Ch1)		0 : use FIR_REG_1 1 : use FIR_REG_2	0
[14]	ADR	Mode of ADR Interface	0 : normal mode 1 : ADR mode	1
[15]	reserved	reserved	must be 0	0

1) In case of synchronization to DMA, no I^2S-slave mode possible.
In case of I^2S-slave mode, no synchronization to DMA allowed. I^2S-Slave mode dominates.
2) The normal operation mode is ‘Tristate’; SBUS is only used in conjunction with DMA.

11.1.3. FIR Coefficients for FIR_REG1

Coefficient	Decimal	Hex
C(0)	7	7
C(1)	23	17
C(2)	52	34
C(3)	84	54
C(4)	112	70
C(5)	127	7F

11.1.4. DCO Increment Setting with SAT Carriers

The following is an example of DCO increment calculation (Fcarrier = 6200 kHz):

For the DCO high part:

DCO_H
= int [2*Fcarrier [KHz] / 9]
= int [2*6200,0 / 9]
= int [1377,77]
= 1377 => **DCO_H = 561 hex**

For the DCO low part:

DCO_L
= 455 * int [2*Fcarrier [kHz] – 9 x DCO_H]
= 455 * int [12400,0 – 12393]
= 455 * 7
= 3185 => **DCO_L = C71 hex**

Table 11–4: DCO increment settings

Frq. MHz	DCO_HI (Hex)	DCO_LO
6.120 6.300 6.480 6.660 6.840	550 578 5A0 5C8 5F0	0 0 0 0 0
7.380 7.560 7.740 7.920	668 690 6B8 6E0	0 0 0 0
8.100 8.280 8.460	708 730 758	0 0 0

11.2. Pure ADR Music Decoding

The DRP processor always tries to synchronize itself to an incoming ADR data stream as it is generated by the MSP. As soon as the synchronization is done and a frame has been decoded correctly, the FSI signal (or the counting of the index value) indicates that the IC is decoding properly and the corresponding status bits are set.

Without any additional adjustments from the controller, the serial outputs SDO0, SDO1, and SP/DIF will generate the digital music bit stream at 48, 32, and 48 kHz sampling frequency.

For the elementary free to air ADR music decoding operation, no additional adjustments have to be done.

11.3. Receiving the ADR Data

The DRP 3510A is controlled completely by the use of a controller with an I^2C interface. The DRP I^2C interface is of the slave type. In addition to the I^2C-device address, subaddresses are used.

There are two ways of communicating with the DRP:

1. Reading or writing internal DRP registers via special register read/write commands.
This may be useful for configuration purposes, e.g. for configuring an interface or for reading the status register of the receiver (CRC-check error, DMX, no input available, ...).

2. Reading the ADR status and data block.
The ADR-status and data block consist of a16-bit status word plus 9 words à 16-bit (ADR ancillary data) as documented in the ASTRA/DMX specification. The error correction for these data values is already performed within the DRP. In order to read out these values, the controller has to send a specific I^2C command to the DRP, which initiates the DRP to send these 10 data values. There are two ways to check whether a new data block is available. In the normal mode (PIO used for FSI, FSI automatic), the FSI is low when new data are available. After readout by the controller, but at the latest before these data become invalid, the FSI becomes high. Otherwise, the incremented index of the 16-bit status word is to check. The FSI signal (see section 3.) or the incremented index of the 16-bit status word may be used to check whether a new data block is available.

11.4. Receiving FM / TV Sound with MSP

When the MSP is configured for receiving analog FM/TV sound, the internal PLL of the DRP has to be switched off. This is to prevent frequency deviation caused by the DRP timing recovery, which tries to receive ADR further on. There are two options available. First, is to use the download program I^2S to SP/DIF. This gives the advantage of having the FM/TV sound at the digital interface and at the 48 kHz DAC as well. The second option is to configure the MSP as master and set its I^2S-Bus to tristate. This can be done with a single I^2C-command (see data sheet of MSP). This latter option will not work in the 24.576 MHz single crystal mode (8.3).

The following download programs are available:

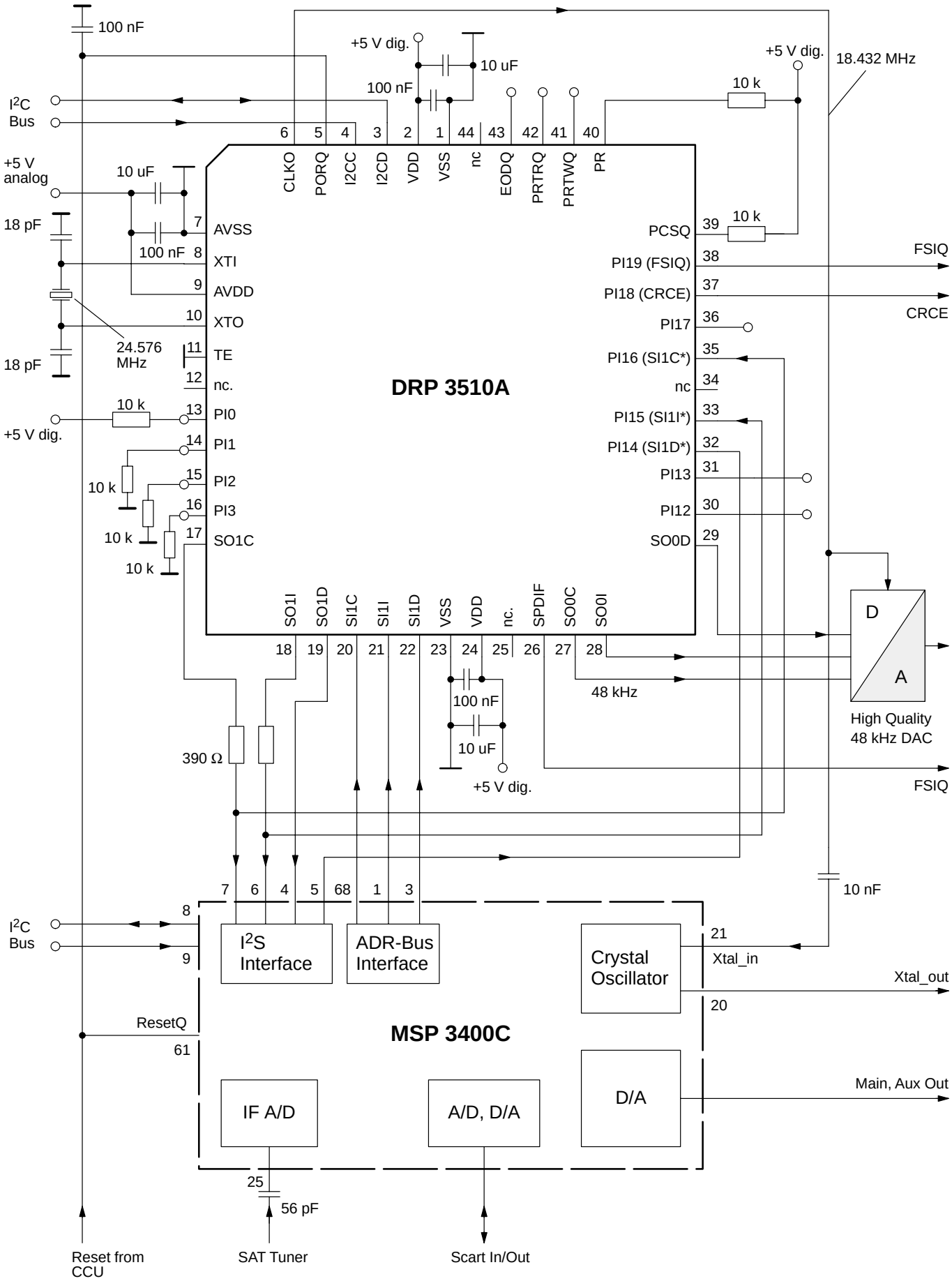
src_e4b.mas:
MSP FM sound via I^2S (32 kHz at SDI1) to:
– SPDIF output (48 kHz)
– HQ DAC output (SDO0 with 48 kHz)
– feed back to the DRP I^2S out (SDO1 with 32 kHz)

spdif_e4.mas :
MSP FM sound via I^2S (32 kHz at SDI1) to:
– SPDIF output (32 kHz)
– HQ DAC output (SDO0 with 32 kHz)
– feed back to the DRP I^2S out (SDO1 with 32 kHz)

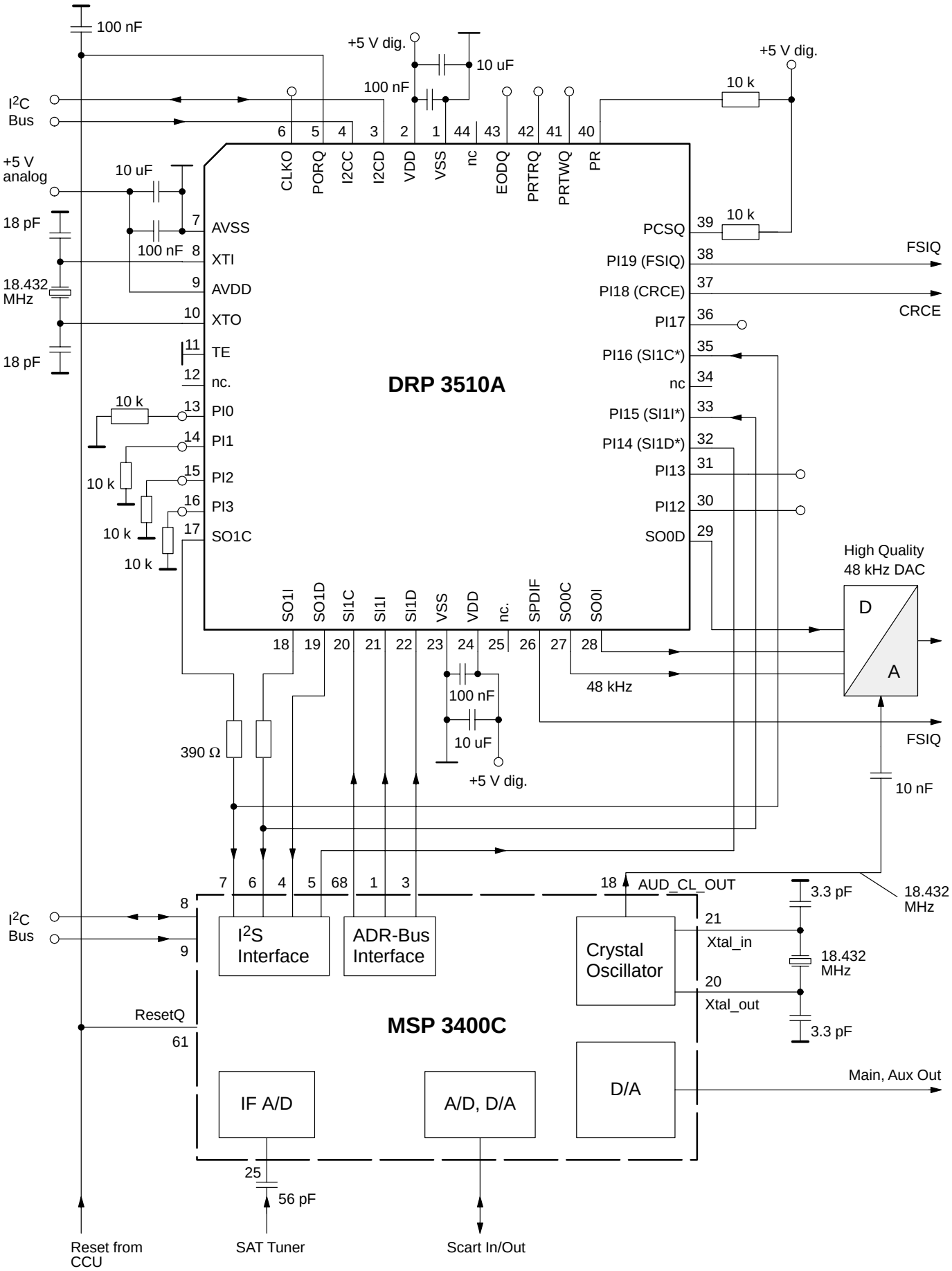
11.5. Receiving of ADR

Once receiving ADR, the content of the clock-deviation register (see 9.5.) is associated with the deviation of the crystal. It is helpful and will speed up the synchronization to re-initialize this register after changing the ADR-station with this value. If the DRP is not receiving ADR within more than 10 seconds (no carrier, device not connected with LNC, ...) it is necessary to re-initialize the clock-deviation register as well. This can be detected by watching the L-bit of the index register (see section 8.1.).

11.6. Typical ADR Application Circuit (DRP Application with 24 MHz Single Crystal Mode)



11.7. Typical ADR Application Circuit (DRP Application with 18 MHz Dual Crystal Mode)



12. Timing Diagrams

12.1. PIO Timing

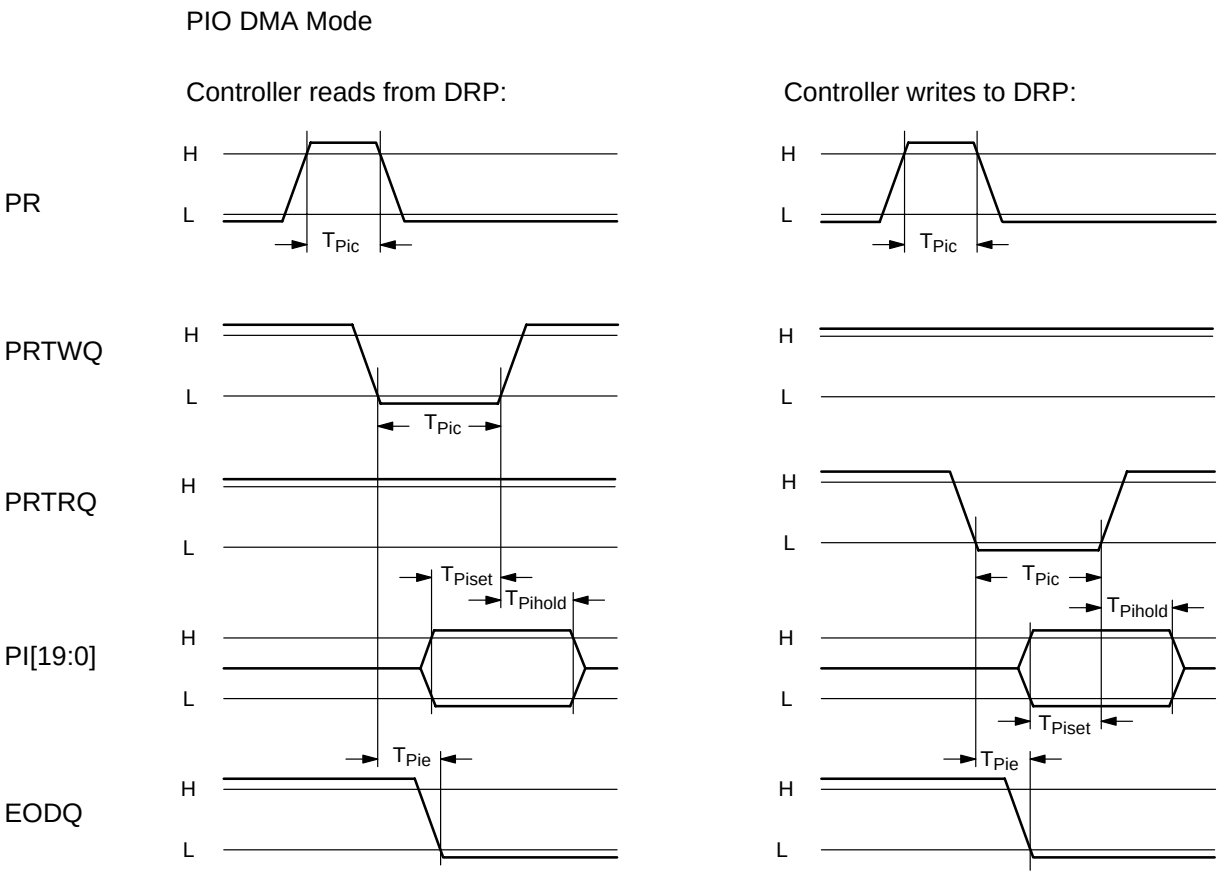


Fig. 12–1: PIO timing

12.2. FSI Timing

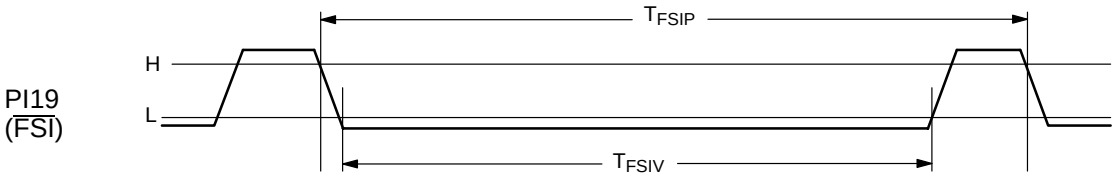


Fig. 12–2: FSI-timing

12.3. SDI Timing

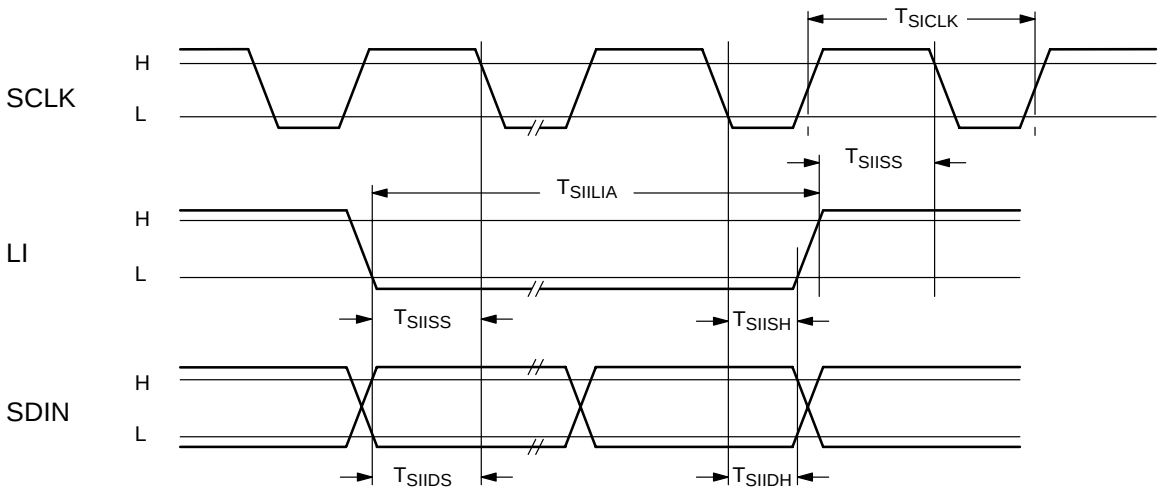


Fig. 12–3: SDI timing

12.4. SDO Timing

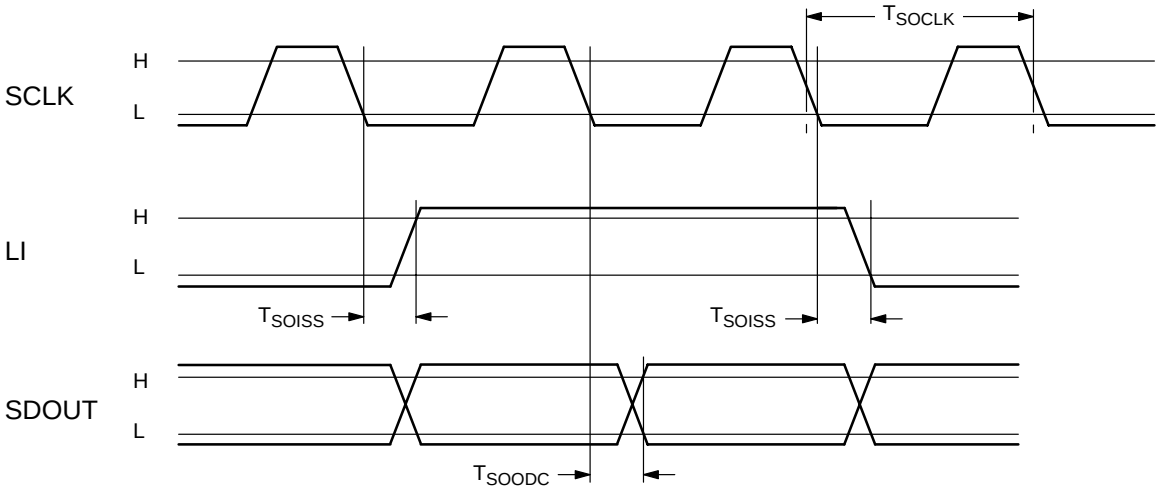


Fig. 12–4: SDO timing

12.5. SPDIF timing

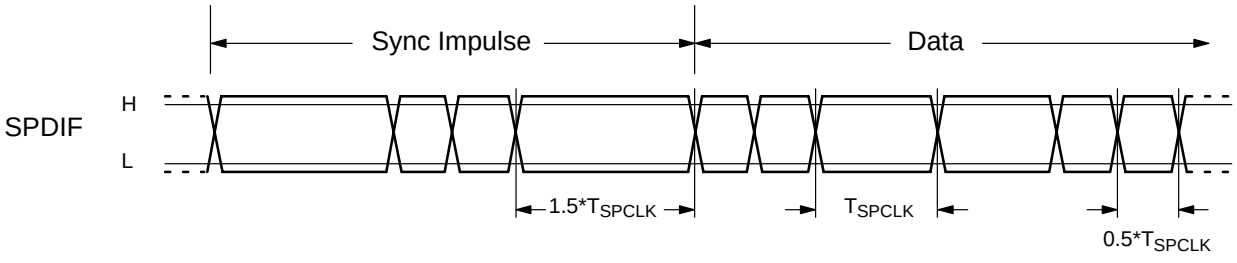


Fig. 12–5: SPDIF timing

12.6. Recommended Power Up Sequence

12.6.1. Power Up Sequence for Dual Crystal Modes

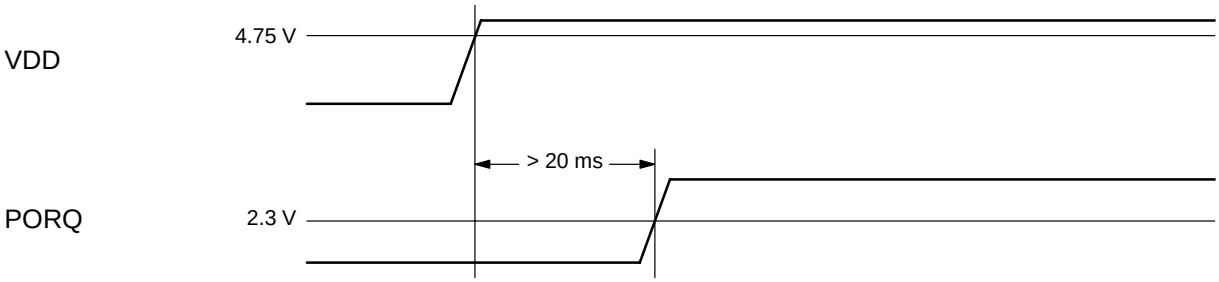


Fig. 12–6: Recommended power up sequence (dual crystal modes)

12.6.2. Power Up Sequence for 18.432 MHz Single Crystal Mode

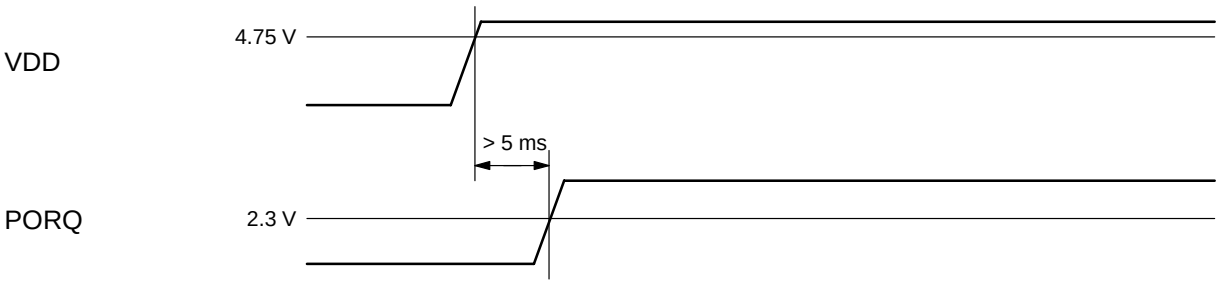


Fig. 12–7: Recommended power up sequence (18 MHz single crystal mode)

12.6.3. Power Up Sequence for 24.576 MHz Single Crystal Mode

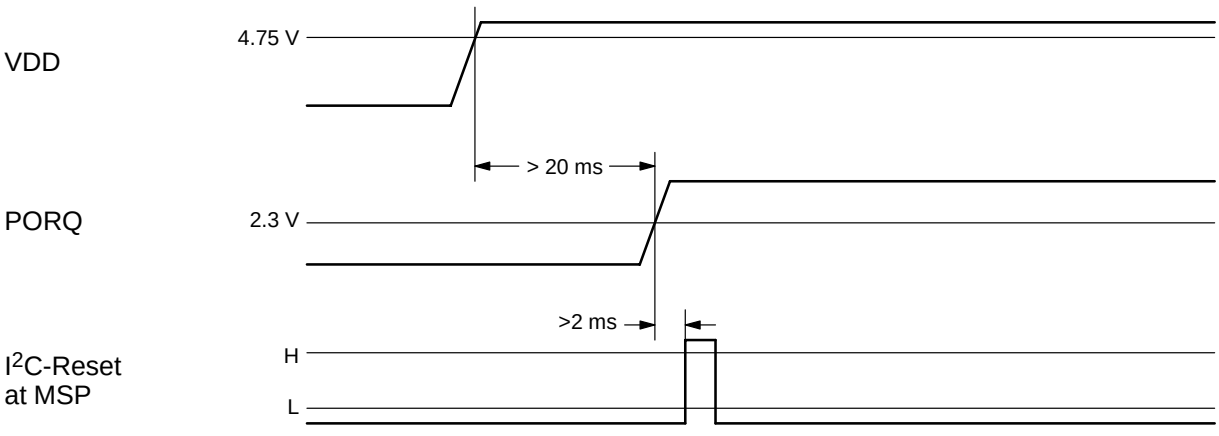


Fig. 12–8: Recommended power up sequence (24 MHz single crystal mode)

13. DRP 3510A Version History

Version D3 (05.03.96)

Improvements and new features:

- single crystal option
- adjustable gain
- SPDIF tristate switchable
- PIO-read mode
- get ADR data modified (with offset)

Known bugs/Status:

- FSI will not set (workaround available)
- inverted SDO-clock delay (workaround available)
- L2 PLL does not work
- Layer 2 decoder does not synchronize to all bitstreams with fs = 44, 1 kHz

Version E4 (12.06.96)

Improvements and new features:

- fast synchronization, better C/N
- setup of sample rate converter (to MSP) improved
- SP/DIF holds synchronization even in “channel hopping”
- “force restart” (bit 19 at main configuration register) works at anytime
- delay bit removed from FSI off-bit added to main configuration register
- SDO0 wordstrobe inverted (according to the DA converters)
- download program I^2S to SPDIF with sample rate conversion to 48 kHz available
- Layer 2 decoder: 44.1 kHz bug fixed, PLL works

Known bugs/Status:

- Status: “weak carrier” does not work properly (workaround available)
- Status: “carrier detect” does not work properly (workaround available
- PIO-mode with disturbances

14. Data Sheet History

1. Advance Information: “DRP 3510A Digital Radio Processor”, Jan. 16, 1997, 6251-410-1AI.
First release of the advance information.

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