

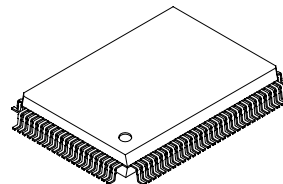
CMOS 8-bit Single Chip Microcomputer

Description

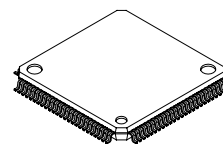
The CXP740056/740096/740010 is a CMOS 8-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, remote control receive circuit, PWM output, and the like besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP740056/740096/740010 also provides the sleep/stop functions that enables lower power consumption.

100 pin QFP (Plastic)



100 pin LQFP (Plastic)



Structure

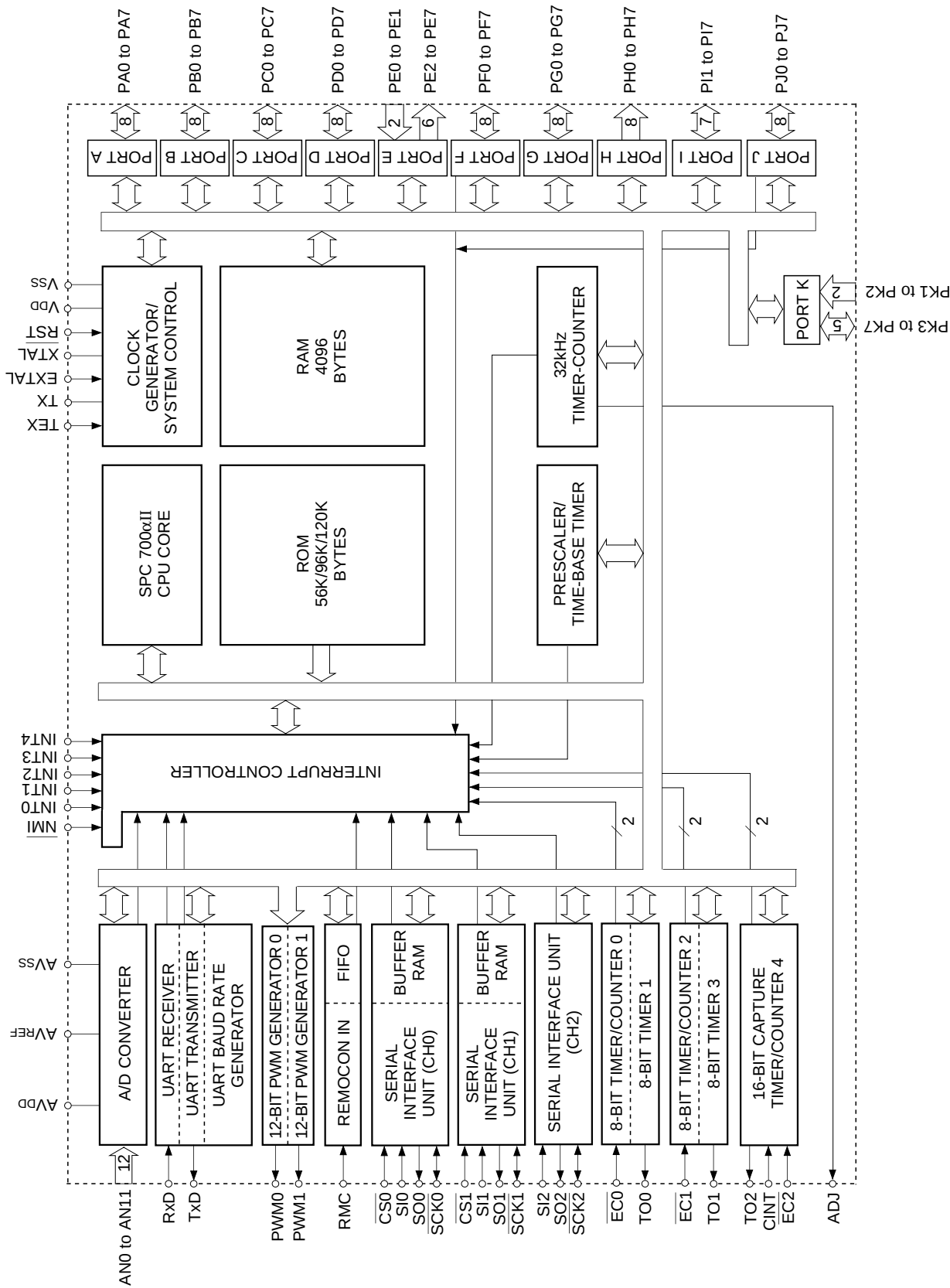
Silicon gate CMOS IC

Features

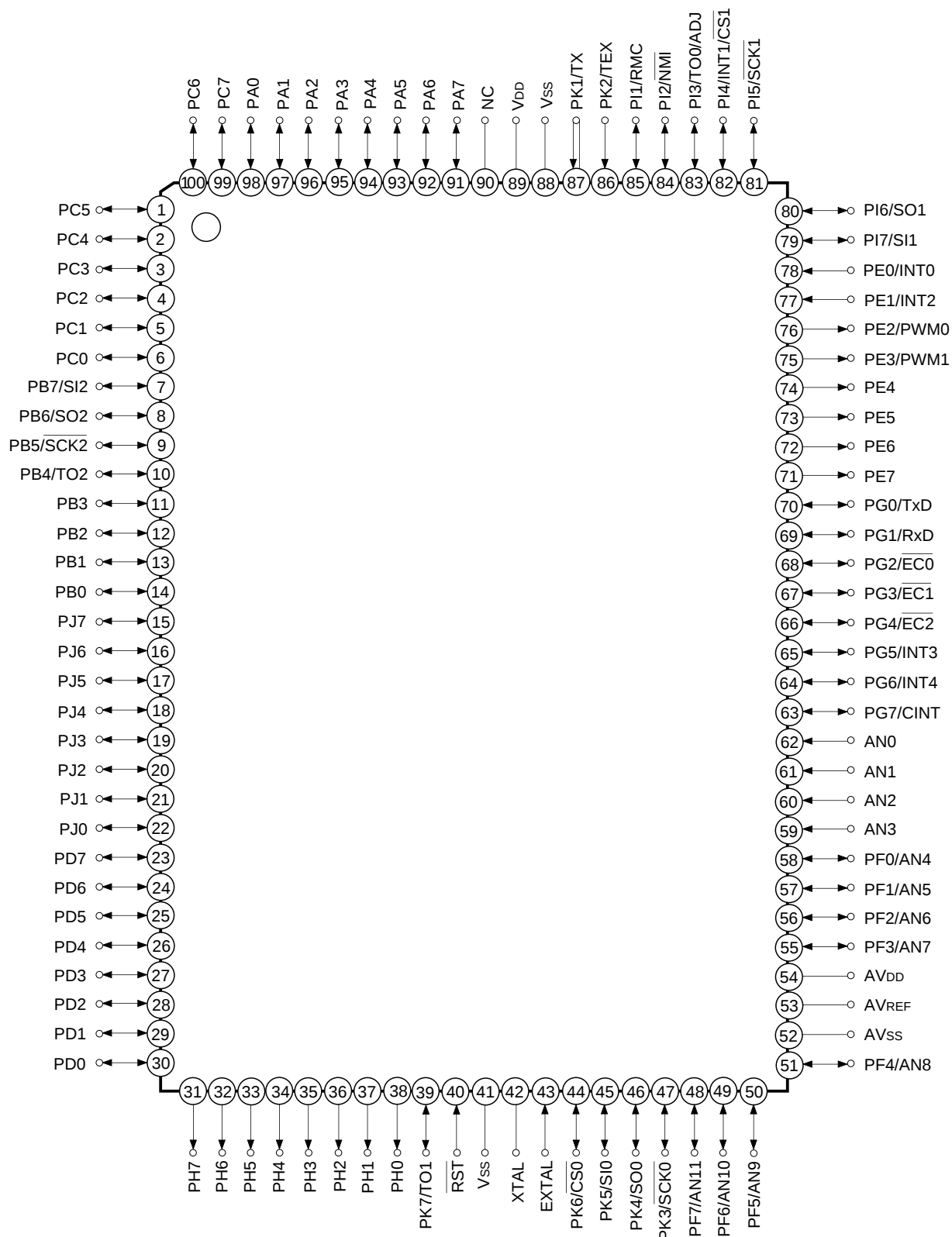
- A wide instruction set (211 instructions) which covers various types of data.
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 167ns at 24MHz operation (4.5 to 5.5V)
 - 333ns at 12MHz operation (2.7 to 5.5V)
 - 122μs at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity
 - 56K bytes (CXP740056)
 - 96K bytes (CXP740096)
 - 120K bytes (CXP740010)
- Incorporated RAM capacity
 - 4096 bytes
- Peripheral functions
 - A/D converter
 - 8 bits, 8 channels, successive approximation method (Conversion time 10.3μs at 24MHz)
 - Serial interface
 - Start-stop synchronization (UART), 1 channel
 - Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 2 channels
 - 8-bit clock synchronization (MSB/LSB first selectable), 1 channel
 - Timer
 - 8-bit timer 2 channels, 8-bit timer/counter 2 channels,
 - 19-bit time-base timer, 16-bit capture timer/counter
 - 32kHz timer/counter
 - Remote control receive circuit
 - Noise elimination circuit
 - 8-bit pulse measuring counter, 6-stage FIFO
 - PWM output
 - 12 bits, 2 channels
- Interruption
 - 22 factors, 15 vectors, multi-interruption possible
- Standby mode
 - Sleep/stop
- Package
 - 100-pin plastic QFP/LQFP
- Piggy/evaluation chip
 - CXP740000

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



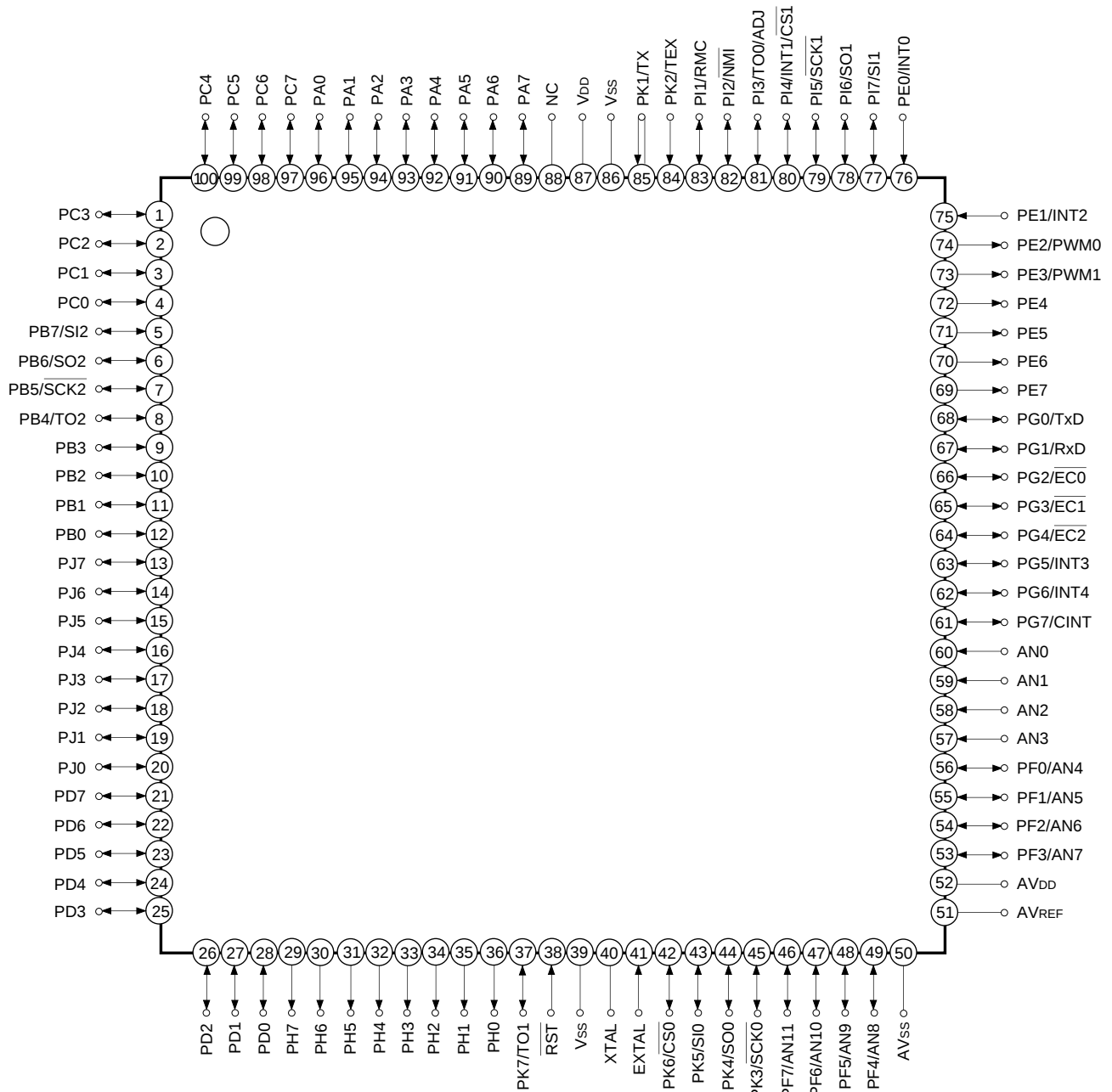
Pin Assignment (Top View) 100-pin QFP package



Note) 1. NC (Pin 90) is left open.

2. Vss (Pins 41 and 88) are both connected to GND.

Pin Assignment (Top View) 100-pin LQFP package



- Note)** 1. NC (Pin 88) is left open.
 2. Vss (Pins 39 and 86) are both connected to GND.

Pin Description

Symbol	I/O	Description	
PA0 to PA7	I/O	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PB0 to PB3	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	16-bit timer/counter rectangular wave output.
PB4/TO2	I/O/Output		Serial clock I/O (CH2).
PB5/SCK2	I/O/I/O		Serial data output (CH2).
PB6/SO2	I/O/Output		Serial data input (CH2).
PB7/SI2	I/O/Input		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PE0/INT0	Input/Input	(Port E) 8-bit port. Lower 2 bits are for input; upper 6 bits are for output. (8 pins)	External interrupt inputs. (2 pins)
PE1/INT1	Input/Input		
PE2/PWM0	Output/Output		12-bit PWM outputs. (2 pins)
PE3/PWM1	Output/Output		
PE4 to PE7	Output		
PF0/AN4 to PF7/AN11	I/O	(Port F) 8-bit I/O port. PF4 to PF7 can be set in a unit of single bits as standby release inputs. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (8 pins)

Symbol	I/O	Description	
PG0/TxD	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	UART transmission data output.
PG1/RxD	I/O/Input		UART reception data input.
PG2/ $\overline{\text{EC0}}$	I/O/Input		External event input for 8-bit timer/counter 0.
PG3/ $\overline{\text{EC1}}$	I/O/Input		External event input for 8-bit timer/counter 2.
PG4/ $\overline{\text{EC2}}$	I/O/Input		External event input for 16-bit timer/counter.
PG5/INT3	I/O/Input		External interrupt inputs. (2 pins)
PG6/INT4	I/O/Input		
PG7/CINT	I/O/Input		External capture input to 16-bit timer/counter.
PH0 to PH7	Output	(Port H) 8-bit I/O port. Operated as N-ch open drain output for medium voltage drive (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (7 pins)	Remote control receiver circuit input.
PI2/ $\overline{\text{NMI}}$	I/O/Input		Non-maskable interrupt input.
PI3/TO0/ ADJ	I/O/Output/ Output		Output for the 8-bit timer/counter 1 rectangular waves and 32-kHz oscillation frequency demultiplication.
PI4/INT1/ $\overline{\text{CS1}}$	I/O/Input/ Input		External interrupt input.
PI5/ $\overline{\text{SCK1}}$	I/O/I/O		Chip select input for serial interface (CH1).
PI6/SO1	I/O/Output		Serial clock I/O (CH1).
PI7/SI1	I/O/Input		Serial data output (CH1).
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. I/O can be set in a unit of single bits. Standby release input can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PK1/TX	Input	(Port K) 7-bit port. lower 2 bits are for input; upper 5 bits are for I/O. I/O can be set in a unit of single bits. For PK3 to PK7, incorporation of pull-up resistor can be set through the program in a unit of single bits. (7 pins)	Crystal connectors for 32-kHz timer/counter clock oscillation circuit.
PK2/TEX	Input/Input		For usage as event count, connect clock oscillation source to TEX, and leave TX open.
PK3/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).
PK4/SO0	I/O/Output		Serial data output (CH0).
PK5/SI0	I/O/Input		Serial data input (CH0).
PK6/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).
PK7/TO1	I/O/Output		8-bit timer/counter 3 rectangular wave output.

Symbol	I/O	Description
AN0 to AN3	Input	Analog inputs to A/D converter. (4 pins)
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input it to EXTAL pin and input a reversed phase clock to XTAL pin.
XTAL		
$\overline{\text{RST}}$	Input	System reset; active at Low level.
NC		Not connected. Leave this pin open for normal operation.
AVDD		Positive power supply of A/D converter.
AVREF	Input	Reference voltage input of A/D converter.
AVSS		GND of A/D converter.
VDD		Positive power supply.
VSS		GND. Connect both Vss pins to GND.

I/O Circuit Format for Pins

Pin	Circuit format		After a reset
PA0 to PA7 PB0 PB2 PC0 to PC7 18 pins	Port A Port B Port C	Pull-up resistor "0" after a reset Ports A, B, C data Ports A, B, C direction "0" after a reset Internal data bus RD (Ports A, B, C) * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
PB1 PB3 2 pins	Port B	Pull-up resistor "0" after a reset Port B data Port B direction "0" after a reset Internal data bus RD (Port B) Schmitt input * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
PB4/TO2 PI3/TO0/ADJ PK7/TO1 3 pins	Port B Port I Port K	Pull-up resistor "0" after a reset TO0/ADJ, TO1 Ports B, I, K function select "0" after a reset Ports B, I, K data Ports B, I, K direction "0" after a reset Internal data bus RD (Ports B, I, K) * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z

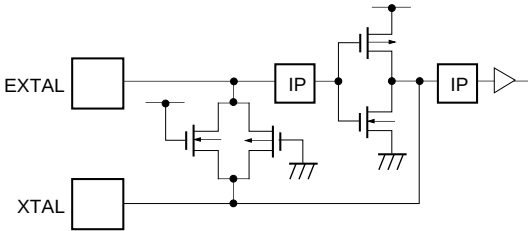
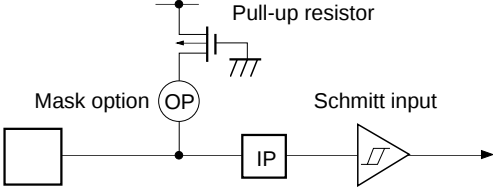
Pin	Circuit format	After a reset
Port B Port I Port K PB5/SCK2 PI5/SCK1 PK3/SCK0 3 pins	* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
Port B Port G Port I Port K PB6/SO2 PG0/TxD PI6/SO1 PK4/SO0 4 pins	* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z

Pin	Circuit format	After a reset
PB7/SI2 PG1/RxD PG2/EC0 PG3/EC1 PG4/EC2 PG5/INT3 PG6/INT4 PG7/CINT PI1/RMC PI2/NMI PI4/INT1/ $\overline{\text{CS}}1$ PI7/SI1 PK5/SIO PK6/ $\overline{\text{CS}}0$	Pull-up resistor “0” after a reset Ports B, G, I, K data Ports B, G, I, K direction “0” after a reset Internal data bus ← RD (Ports B, G, I, K) Schmitt input SI2, RxD, $\overline{\text{EC}}0$, $\overline{\text{EC}}1$, $\overline{\text{EC}}2$, INT3, INT4, CINT, RMC, MNI, INT1/$\overline{\text{CS}}1$, SI1, SIO, $\overline{\text{CS}}0$ * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
PD0 to PD7	Pull-up resistor “0” after a reset Port D data Port D direction Internal data bus ← RD (Port D) *1 Large current 12mA (V_{DD} = 4.5 to 5.5V) 4.5mA (V_{DD} = 2.7 to 3.3V) *2 Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
PE0/INT0 PE1/INT2	Schmitt input IP RD (Port E) INT0, INT2 Internal data bus	Hi-Z

Pin	Circuit format	After a reset
PE2/PWM0 PE3/PWM1 2 pins	Port E PWM0, PWM1 Port E function select "0" after a reset Port E data Internal data bus RD (Port E) Hi-Z by writing to Port E data register or Port E function select register → Output active	Hi-Z
PE4 PE5 2 pins	Port E Port E data Internal data bus RD (Port E) Hi-Z by writing to Port E data register → Output active	Hi-Z
PE6 1 pin	Port E Port E data "1" after a reset Internal data bus RD (Port E)	High level
PE7 1 pin	Port E Internal reset signal Port E data "1" after a reset Internal data bus RD (Port E) * Pull-up transistors approx. 150kΩ (VDD = 4.5 to 5.5V) approx. 200kΩ (VDD = 2.7 to 3.3V)	"H" level "H" level at ON resistance of pull-up transistor during a reset.
AN0 to AN3 4 pins	Input multiplexer A/D converter	Hi-Z

[illegible]

Pin	Circuit format	After a reset
PH0 to PH7 8 pins	Port H Port H data "1" after a reset Internal data bus RD (Port H) * High tension proof 12V Large current 12mA ($V_{DD} = 4.5$ to $5.5V$) 4.5mA ($V_{DD} = 2.7$ to $3.3V$)	Hi-Z
PJ0 to PJ7 8 pins	Port J Pull-up resistor "0" after a reset Port J data Port J direction "0" after a reset Internal data bus RD (Port J) Standby release Edge detection Polarity select "0" after a reset * Pull-up transistors approx. 100kΩ ($V_{DD} = 4.5$ to $5.5V$) approx. 150kΩ ($V_{DD} = 2.7$ to $3.3V$)	Hi-Z
PK1/TX PK2/TEX 2 pins	Port K TEX oscillation circuit control "1" after a reset Internal data bus RD (Port K) Internal data bus RD (Port K) Schmitt input Clock input	Oscillation stop port input

Pin	Circuit format	After a reset
EXTAL XTAL 2 pins	 • Diagram shows circuit configuration during oscillation. • When program stops the oscillation, the feedback register disconnects, and XTAL is driven at "H" level.	Oscillation
$\overline{\text{RST}}$ 1 pin	 Pull-up resistor Mask option Schmitt input	"L" level (during a reset)

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	−0.3 to +0.3	V	
	AV _{REF}	AV _{SS} to +7.0	V	
Input voltage	V _{IN}	−0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ²	V	
High level output current	I _{OH}	−5	mA	Output (value per pin)
High level total output current	ΣI _{OH}	−50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	All pins excluding large current outputs (value per pin)
	I _{OLC}	20	mA	Large current outputs (value per pin) * ³
Low level total output current	ΣI _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	−20 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package
		380		LQFP package

*¹ AV_{DD} and V_{DD} must be set to the same voltage.

*² V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*³ The large current output pins are Port D and H (PD, PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V _{DD}	4.5	5.5	V	fc = 24MHz or less	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock.
		2.7	5.5	V	fc = 12MHz or less	
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode	
		2.7	5.5	V	Guaranteed operation range for TEX	
		2.5	5.5	V	Guaranteed data hold operation range during stop mode	
Analog voltage	AV _{DD}	2.7	5.5	V	*1	
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2, *6	
		0.8V _{DD}	V _{DD}	V	*2, *7	
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*3	
	V _{IHEX}	V _{DD} − 0.4	V _{DD} + 0.3	V	EXTAL pin*4, *6, TEX pin*5, *6	
		V _{DD} − 0.2	V _{DD} + 0.2	V	EXTAL pin*4, *7, TEX pin*5, *7	
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *6	
		0	0.2V _{DD}	V	*2, *7	
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*3	
	V _{ILEX}	−0.3	0.4	V	EXTAL pin*4, *6, TEX pin*5, *6	
		−0.3	0.2	V	EXTAL pin*4, *7, TEX pin*5, *7	
Operating temperature	Topr	−20	+75	°C		

*1 AV_{DD} and V_{DD} must be set to the same voltage.

*2 Normal input port (PA, PB0, PB2, PB4, PB6, PC, PD, PF, PG0, PI3, PI6, PJ, PK1, PK2, PK4, PK7)

*3 RST, PB1, PB3, PB5/SCK2, PB7/SI2, PE0/INT0, PE1/INT2, PG1/RxD, PG2/EC0, PG3/EC1, PG4/EC2, PG5/INT3, PG6/INT4, PG7/CINT, PI1/RMC, PI2/NMI, PI4/INT1/CS1, PI5/SCK1, PI7/SI1, PK3/SCK0, PK5/SIO, PK6/CS0

*4 Specifies only when the external clock is input.

*5 Specifies only when the external event count is input.

*6 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*7 This case applies to the range of 2.7 to 5.5V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)($T_a = -20$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 4.5V$, $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$, $I_{OH} = -1.2mA$	3.5			V
		PB5, PB6* ¹ , PG0* ¹ , PI5, PI6* ¹ , PK3, PK4* ¹	$V_{DD} = 4.5V$, $I_{OH} = -1.0mA$	4.0			V
			$V_{DD} = 4.5V$, $I_{OH} = -2.4mA$	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 4.5V$, $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$, $I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V$, $I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-0.5		-40	μA
	I_{IHT}	TEX	$V_{DD} = 5.5V$, $V_{IL} = 5.5V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}	$\overline{RST}^{*2}$	$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-1.5		-400	μA
	I_{IL}	PA to PD* ³ , PF to PG* ³ , PI to PK* ³				-45	μA
I/O leakage current	I_{IZ}	PA to PD* ³ , PF to PG* ³ , PI to PK* ³ , PE, AN0 to AN3 $\overline{RST}^{*2}$	$V_{DD} = 5.5V$ $V_I = 0, 5.5V$			± 10	μA
Open drain output leakage current (N-ch Tr off state)	$LLOH$	PH	$V_{DD} = 5.5V$ $V_{OH} = 12V$			50	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I _{DD1}	V _{DD}	24MHz crystal oscillation (C ₁ = C ₂ = 15pF)		27	47	mA
			V _{DD} = 5V ± 0.5V				
	I _{DDs1}		Sleep mode		1.0	5.0	mA
			V _{DD} = 5V ± 0.5V				
	I _{DD2}		32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		30	75	μA
			V _{DD} = 3V ± 0.3V				
	I _{DDs2}		Sleep mode		12	40	μA
			V _{DD} = 3V ± 0.3V				
I _{DDs3}	Stop mode (Termination of EXTAL and TEX pins crystal oscillation)				10	μA	
	V _{DD} = 5V ± 0.5V						
Input capacity	C _{IN}	PA to PD, PE0 to PE1, PF to PG, PI to PK, AN0 to AN3, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 This case applies that Port B buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") and Ports G/I/K buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4, 3 and 0 = "1, 1, 1, 1, 1") are ON.

*2 RST pin specifies the input current when the pull-up resistor is selected, and specifies the leakage current when no resistor is selected.

*3 PA to PD, PF to PG and PI to PK pins specify the input current when the pull-up resistor is selected, and specify the leakage current when no resistor is selected.

*4 When all pins are open.

Electrical Characteristics

DC Characteristics ($V_{DD} = 2.7$ to $3.3V$)($T_a = -20$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 2.7V$, $I_{OH} = -0.12mA$	2.5			V
			$V_{DD} = 2.7V$, $I_{OH} = -0.45mA$	2.1			V
		PB5, PB6* ¹ , PG0* ¹ , PI5, PI6* ¹ , PK3, PK4* ¹	$V_{DD} = 2.7V$, $I_{OH} = -0.24mA$	2.5			V
			$V_{DD} = 2.7V$, $I_{OH} = -0.9mA$	2.1			V
Low level output voltage	V_{OL}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 2.7V$, $I_{OL} = 1.0mA$			0.25	V
			$V_{DD} = 2.7V$, $I_{OL} = 1.4mA$			0.4	V
		PD, PH	$V_{DD} = 2.7V$, $I_{OL} = 4.5mA$			0.9	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 3.3V$, $V_{IH} = 3.3V$	0.3		20	μA
	I_{ILE}		$V_{DD} = 3.3V$, $V_{IL} = 0.3V$	-0.3		-20	μA
	I_{IHT}	TEX	$V_{DD} = 3.3V$, $V_{IL} = 3.3V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 3.3V$, $V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}	$\overline{RST}^{*2}$	$V_{DD} = 3.3V$, $V_{IL} = 0.3V$	-0.9		-200	μA
	I_{IL}	PA to PD* ³ , PF to PG* ³ , PI to PK* ³				-20	μA
I/O leakage current	I_{IZ}	PA to PD* ³ , PF to PG* ³ , PI to PK* ³ , PE, AN0 to AN3 $\overline{RST}^{*2}$	$V_{DD} = 3.3V$ $V_i = 0, 3.3V$			± 10	μA
	I_{LOH}	PH	$V_{DD} = 3.3V$ $V_{OH} = 12V$			50	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I _{DD1}	V _{DD}	12MHz crystal oscillation (C ₁ = C ₂ = 15pF)		8	20	mA
			V _{DD} = 3.0V ± 0.3V*3				
	I _{DDS1}		Sleep mode		0.3	1.5	mA
			V _{DD} = 3.0V ± 0.3V				
	I _{DDS3}		Stop mode (Termination of EXTAL and TEX pins crystal oscillation)			10	μA
V _{DD} = 3.0V ± 0.3V							
Input capacity	C _{IN}	PA to PD, PE0 to PE1, PF to PG, PI to PK, AN0 to AN3, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 This case applies that Port B buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") and Ports G/I/K buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4, 3 and 0 = "1, 1, 1, 1, 1") are ON.

*2 $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistor is selected, and specifies the leakage current when no resistor is selected.

*3 PA to PD, PF to PG and PI to PK pins specify the input current when the pull-up resistor is selected, and specify the leakage current when no resistor is selected.

*4 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, V_{DD} = 2.7 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f _c	XTAL EXTAL	Fig. 1, Fig. 2 V _{DD} = 4.5 to 5.5V	1		24	MHz
				1		12	
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive V _{DD} = 4.5 to 5.5V	28			ns
				37.5			
System clock input rise time, fall time	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	$\overline{\text{EC}}$	Fig. 3	t _{sys} + 50* ¹			ns
Event count input clock rise time, fall time	t _{ER} , t _{EF}	$\overline{\text{EC}}$	Fig. 3			20	ms
System clock frequency	f _c	TEX TX	V _{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise time, fall time	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 000FEh).

t_{sys} [ns] = 2000/f_c (upper two bits = "00"), 4000/f_c (upper two bits = "01"), 16000/f_c (upper two bits = "11")

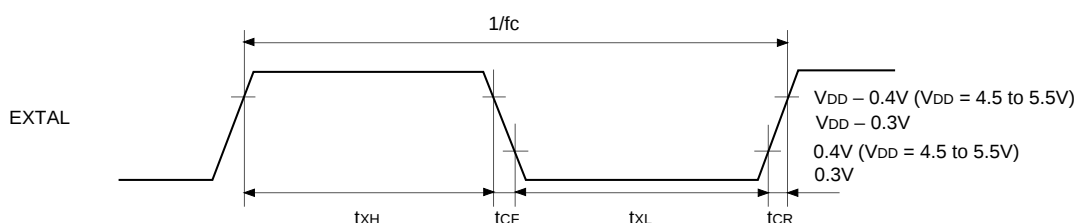


Fig. 1. Clock timing

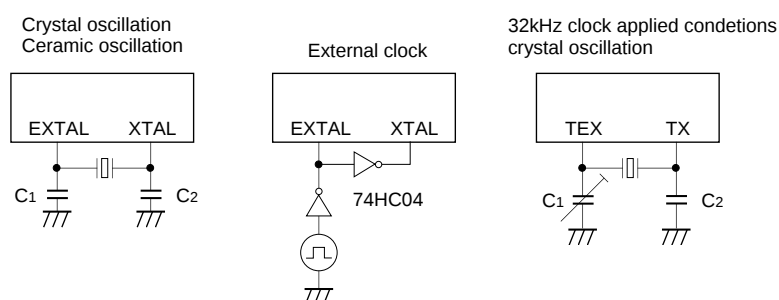


Fig. 2. Clock applied conditions

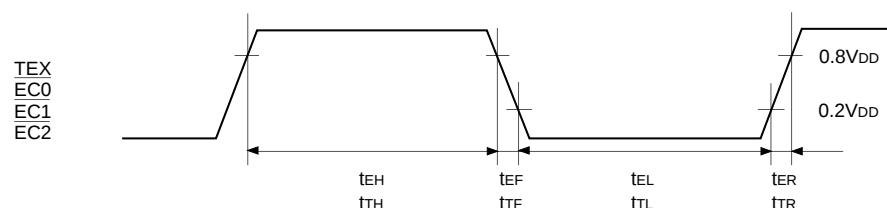


Fig. 3. Event count clock timing

(2) Serial transfer (CH0, CH1)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t _{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{DCSO}	SO0 SO1	Chip select transfer mode		1.5t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow SO$ floating delay time	t _{DCSOF}	SO0 SO1	Chip select transfer mode		1.5t _{sys} + 200	ns
$\overline{CS}$ High level width	t _{WHCS}	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK}$ cycle time	t _{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level width	t _{KH} t _{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	t _{sys} + 100		ns
			Output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t _{SIK}	SI0 SI1	$\overline{SCK}$ input mode	-t _{sys} + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t _{KSI}	SI0 SI1	$\overline{SCK}$ input mode	2t _{sys} + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0 SO1	$\overline{SCK}$ input mode		2t _{sys} + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0 for CH0; they represent $\overline{CS1}$, $\overline{SCK1}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Note 4) This case applies that Port I/K output buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4 and 3 = "0, 0, 0, 0") is OFF.

Serial transfer (CH0, CH1)

(Ta = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{CS}}\downarrow \rightarrow \overline{\text{SCK}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$ $\overline{\text{SCK1}}$	Chip select transfer mode (SCK = output mode)		$1.5t_{\text{sys}} + 250$	ns
$\overline{\text{CS}}\uparrow \rightarrow \overline{\text{SCK}}$ floating delay time	t_{DCSKF}	$\overline{\text{SCK0}}$ $\overline{\text{SCK1}}$	Chip select transfer mode (SCK = output mode)		$1.5t_{\text{sys}} + 250$	ns
$\overline{\text{CS}}\downarrow \rightarrow \text{SO}$ delay time	t_{DCSO}	SO0 SO1	Chip select transfer mode		$1.5t_{\text{sys}} + 250$	ns
$\overline{\text{CS}}\uparrow \rightarrow \text{SO}$ floating delay time	t_{DCSOF}	SO0 SO1	Chip select transfer mode		$1.5t_{\text{sys}} + 250$	ns
$\overline{\text{CS}}$ High level width	t_{WHCS}	$\overline{\text{CS0}}$ $\overline{\text{CS1}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$ $\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK}}$ High and Low level widths	t_{KH} t_{KL}	$\overline{\text{SCK0}}$ $\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$4000/f_c - 100$		ns
SI input setup time (for $\overline{\text{SCK}}\uparrow$)	t_{SIK}	SI0 SI1	$\overline{\text{SCK}}$ input mode	$-t_{\text{sys}} + 100$		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}}\uparrow$)	t_{KSI}	SI0 SI1	$\overline{\text{SCK}}$ input mode	$2t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}}\downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO0 SO1	$\overline{\text{SCK}}$ input mode		$2t_{\text{sys}} + 250$	ns
			$\overline{\text{SCK}}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (upper 2 bits = "00"), 4000/ f_c (upper 2 bits = "01"), 16000/ f_c (upper 2 bits = "11")

Note 2) $\overline{\text{CS}}$, $\overline{\text{SCK}}$, SI and SO represent $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, SI0 and SO0 for CH0; they represent $\overline{\text{CS1}}$, $\overline{\text{SCK1}}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of $\overline{\text{SCK}}$ output mode and SO output delay time is 50pF.

Note 4) This case applies that Port G/I/K output buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4 and 3 = "1, 1, 1, 1") is ON.

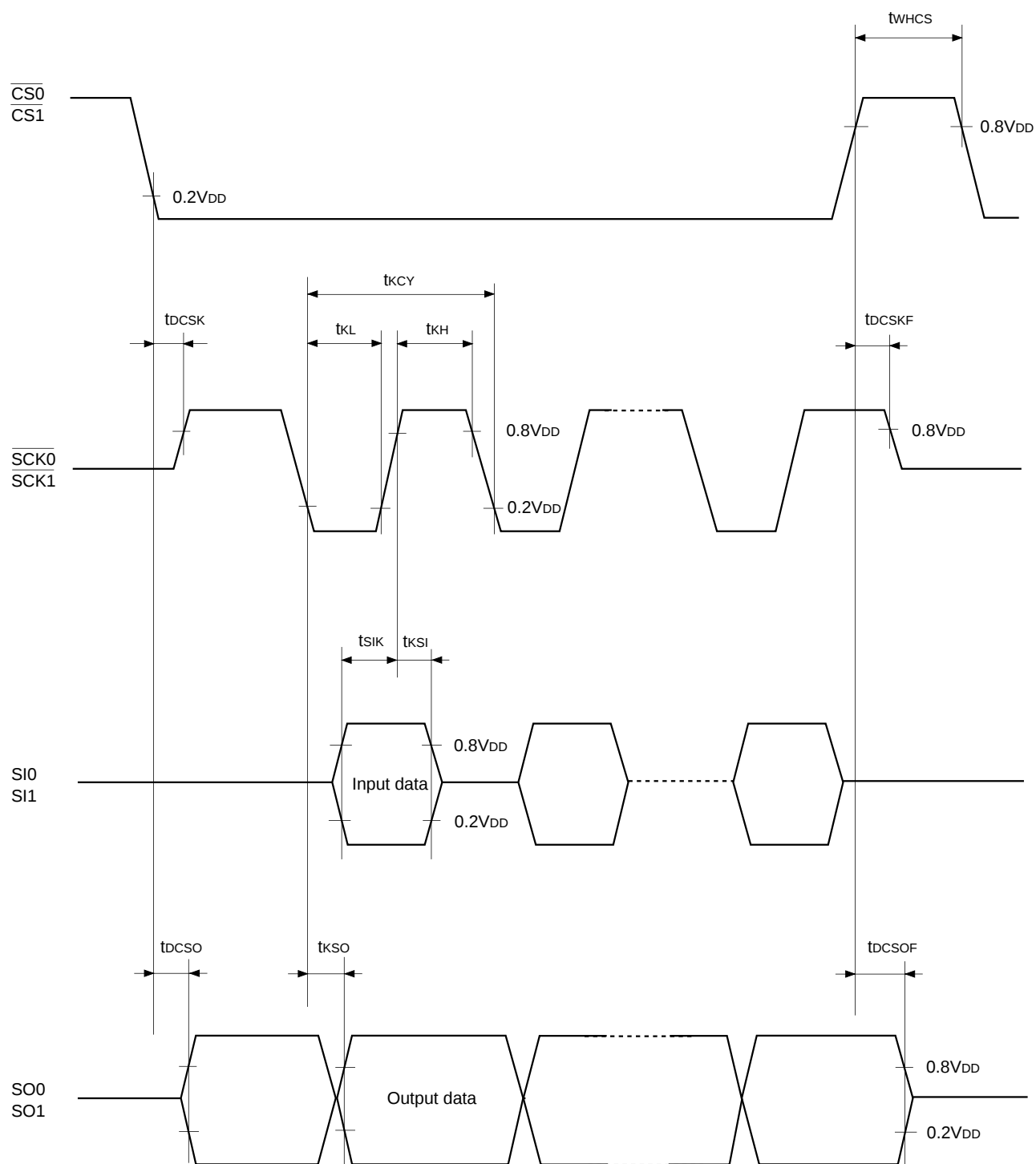


Fig. 4. Serial transfer CH0, CH1 timing

Serial transfer (CH2)(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK2}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level widths	t_{KH} t_{KL}	$\overline{\text{SCK2}}$	Input mode	400		ns
			Output mode	4000/fc – 50		ns
SI input setup time (for $\overline{\text{SCK}}\uparrow$)	t_{SIK}	SI2	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}}\uparrow$)	t_{KSI}	SI2	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\text{SCK}\downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO2	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

Note 2) $\overline{\text{SCK}}$, SI and SO represent $\overline{\text{SCK2}}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{\text{SCK2}}$ output mode and SO2 output delay time is 50pF+1TTL.

Note 4) This case applies that Port B output buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "0, 0") is OFF.

Serial transfer (CH2)(Ta = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK2}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level widths	t_{KH} t_{KL}	$\overline{\text{SCK2}}$	Input mode	400		ns
			Output mode	4000/fc – 100		ns
SI input setup time (for $\overline{\text{SCK}}\uparrow$)	t_{SIK}	SI2	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}}\uparrow$)	t_{KSI}	SI2	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\text{SCK}\downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO2	$\overline{\text{SCK}}$ input mode		250	ns
			$\overline{\text{SCK}}$ output mode		125	ns

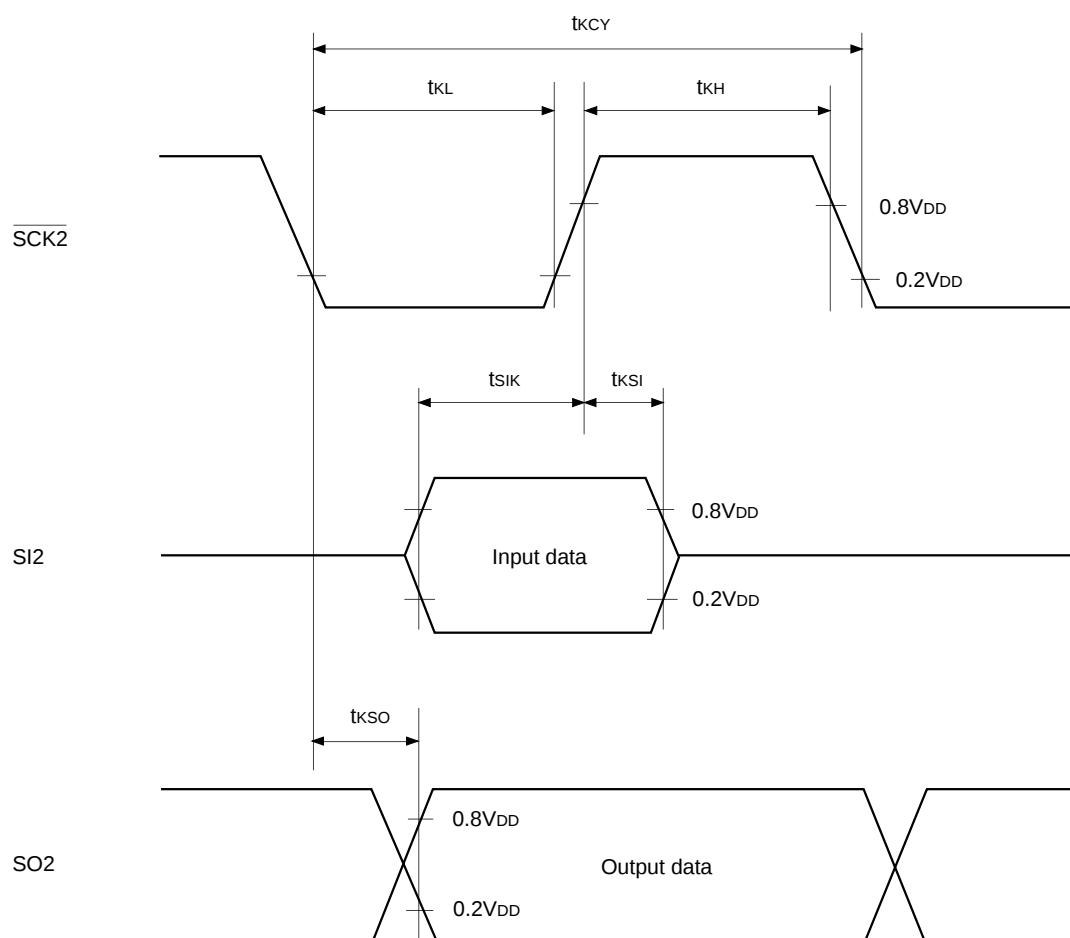
Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

Note 2) $\overline{\text{SCK}}$, SI and SO represent $\overline{\text{SCK2}}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{\text{SCK2}}$ output mode and SO2 output delay time is 50pF.

Note 4) This case applies that Port B output buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") is ON.

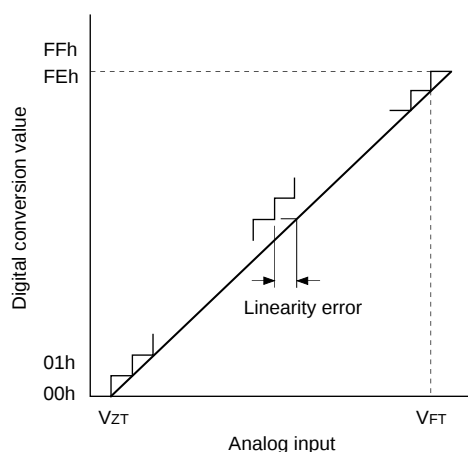
**Fig. 5. Serial transfer CH2 timing**

(3) A/D converter characteristics(Ta = -20 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V _{DD} = AV _{DD} = AV _{REF} = 5.0V V _{SS} = AV _{SS} = 0V			±2	LSB
Absolute error						±3	LSB
Conversion time	t _{CONV}			31/f _{ADC} *3, *4			μs
Sampling time	t _{SAMP}			10/f _{ADC} *3, *4			μs
Reference input voltage	V _{REF}	AV _{REF}	V _{DD} = AV _{DD} = 4.5 to 5.5V	AV _{DD} - 0.5			V
Analog input voltage	V _{IAN}	AN0 to AN11		0			V
AV _{REF} current	I _{REF}	AV _{REF}	Operation mode		0.6	1.0	mA
	I _{REFS}		Sleep mode Stop mode 32kHz operation mode			10	μA

(Ta = -20 to +75°C, V_{DD} = AV_{DD} = 2.7 to 3.3V, AV_{REF} = 2.7 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V _{DD} = AV _{DD} = AV _{REF} = 3.0V V _{SS} = AV _{SS} = 0V			±2	LSB
Absolute error						±3	LSB
Conversion time	t _{CONV}			31/f _{ADC} *3, *4			μs
Sampling time	t _{SAMP}			10/f _{ADC} *3, *4			μs
Reference input voltage	V _{REF}	AV _{REF}	V _{DD} = AV _{DD} = 2.7 to 3.3V	AV _{DD} - 0.3			V
Analog input voltage	V _{IAN}	AN0 to AN11		0			V
AV _{REF} current	I _{REF}	AV _{REF}	Operation mode		0.4	0.7	mA
	I _{REFS}		Sleep mode Stop mode 32kHz operation mode			10	μA



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 000F9h).

PS3 selected f_{ADC} = f_c/4

PS4 selected f_{ADC} = f_c/8

However, when PS3 is selected, f_c is 12MHz or less.

*4 Sub clock operated t_{CONV} = 34/f_{TEX}

t_{SAMP} = 10/f_{TEX}

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 2.7 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t _{IH} t _{IL}	INT0 INT1 INT2 INT3 <u>INT4</u> <u>NMI</u>		1		μs
Reset input Low level width	t _{RSL}	<u>RST</u>		32/f _c		μs

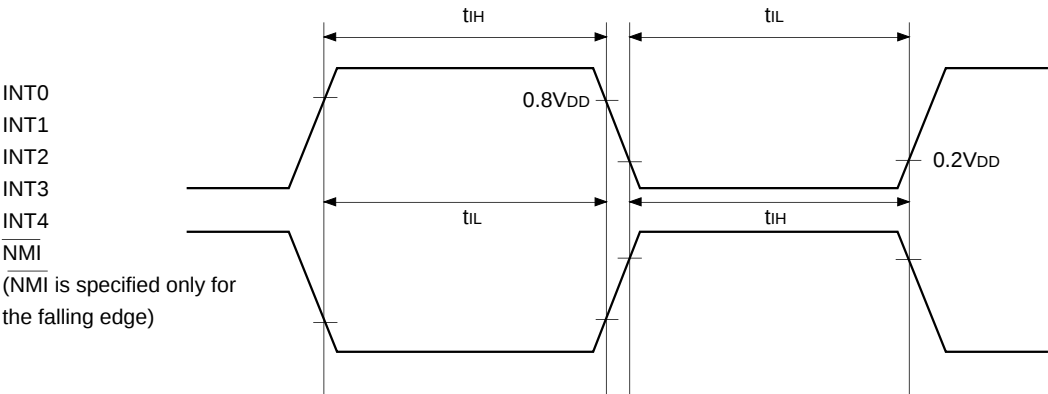


Fig. 7. Interruption input timing

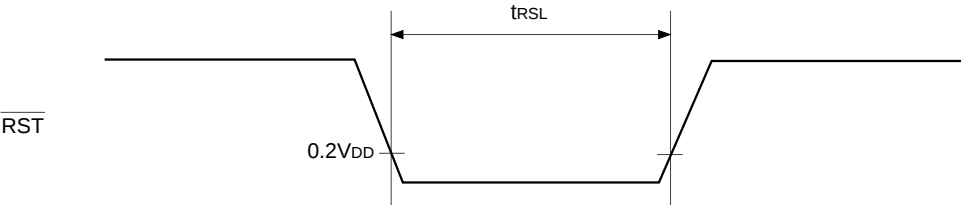
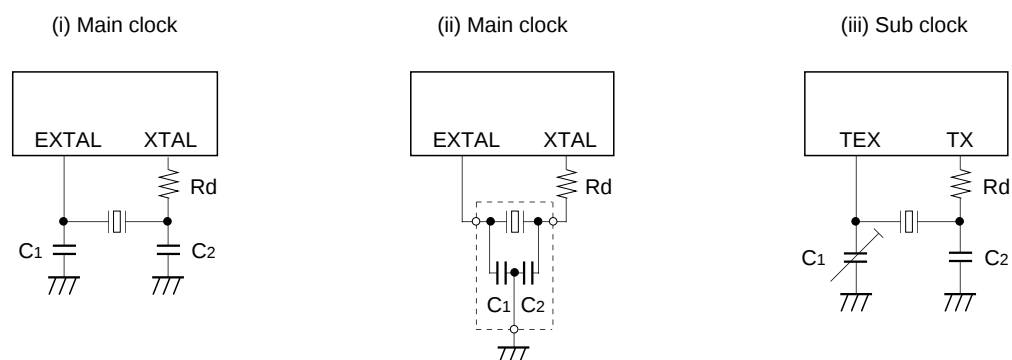


Fig. 8. RST input timing

Appendix

Fig. 9. Recommended oscillation circuit

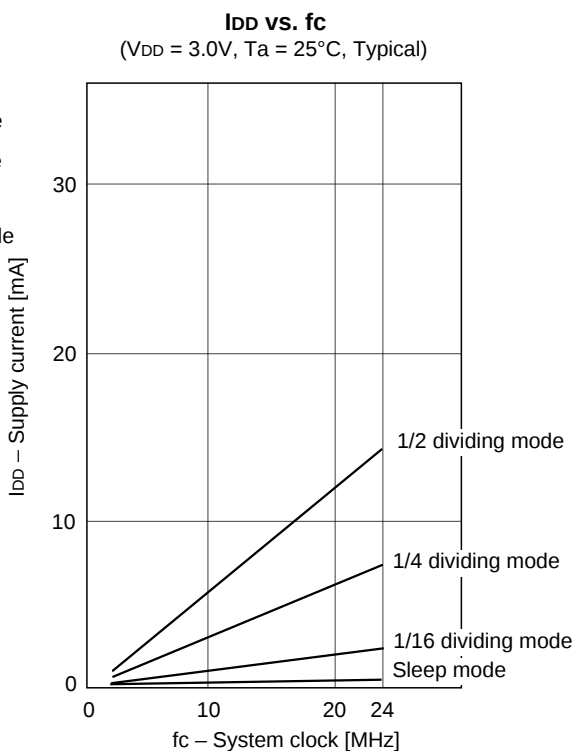
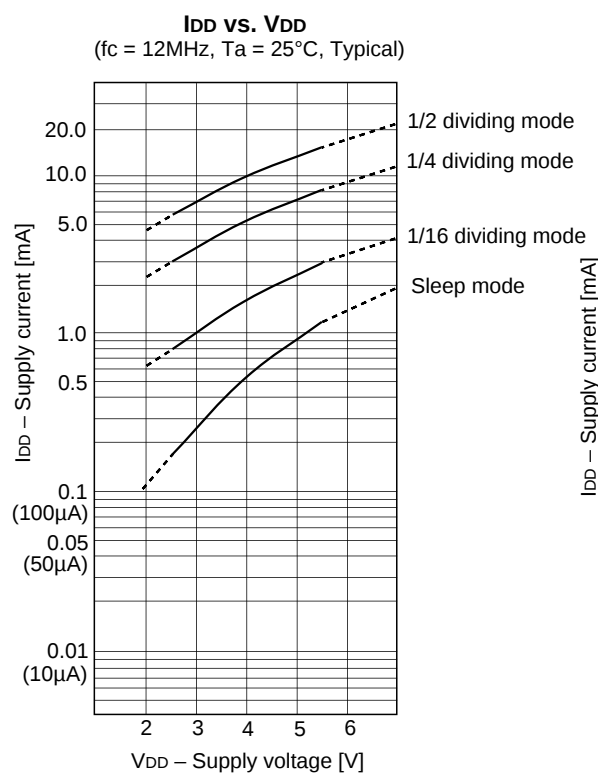
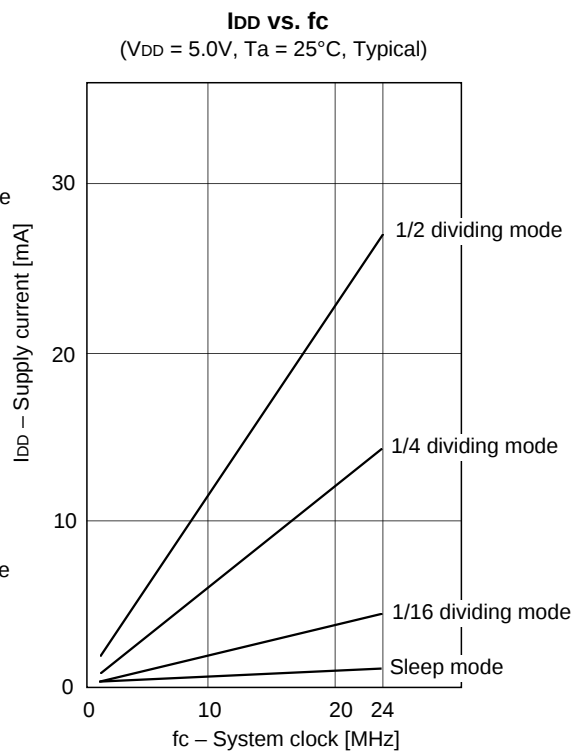
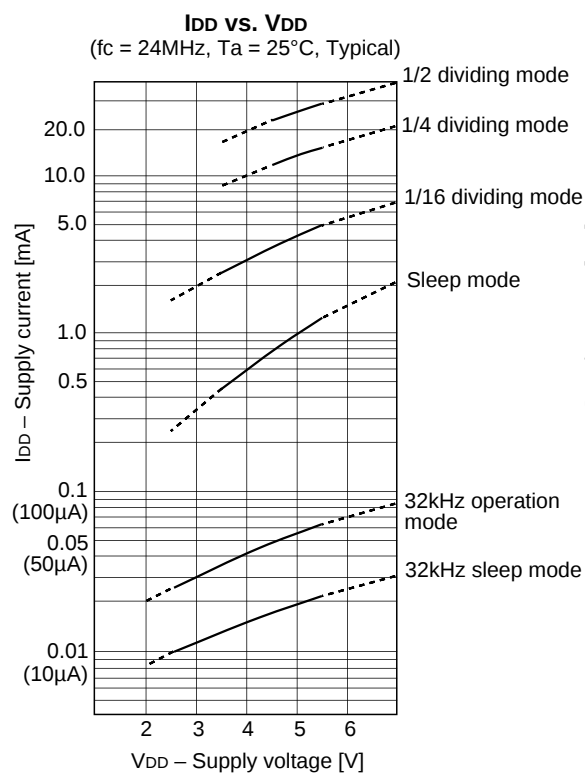


Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	Rd (Ω)	Circuit example	Remarks		
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0 *1	(i)			
	CSA12.0MTZ	12.0							
	CSA16.00MXZ040	16.0	5	5		(ii)			
	CST10.0MTW*	10.0	30	30					
	CST12.0MTW*	12.0							
	CST16.00MXW0C1*	16.0	5	5					
RIVER ELETEC CO., LTD.	HC-49/U03	8.0	18	18	330 *1	(i)			
		12.0	12	12					
		16.0	10	10					
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0 *1			(iii)	
		12.0	5	5					
		16.0	Open	Open					
	P3	32.768kHz	30	33	120k				
Seiko Instruments Inc.	VTC-200 SP-T	32.768kHz	18	18	330k	(iii)	CL = 12.5pF		

* Indicates types with on-chip grounding capacitor (C₁, C₂).

*¹ XTAL series resistor (R_d = 500Ω or less) is hard to affect noise by ESD.

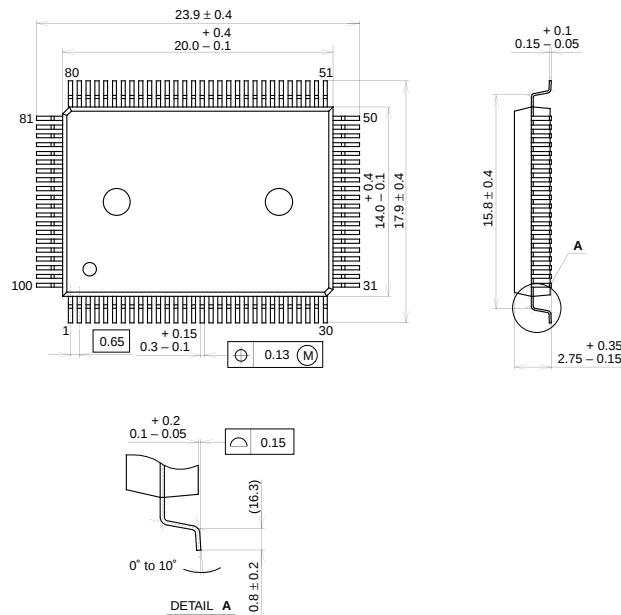
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

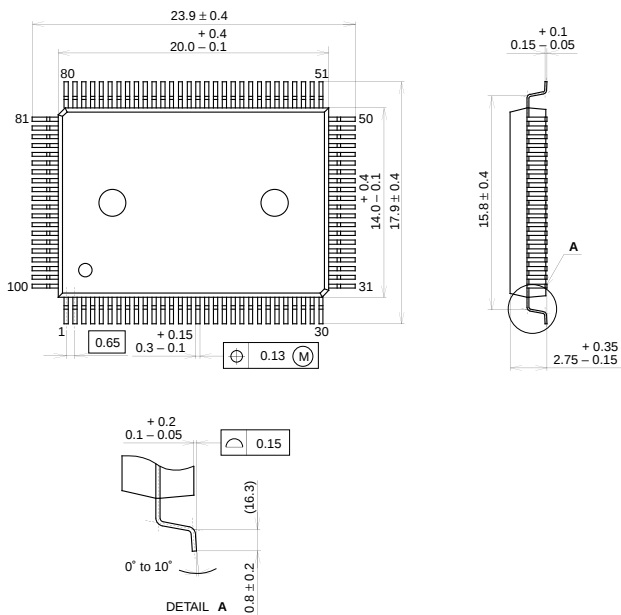


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

Unit: mm

Technical drawing of a square mold with dimensions and details.

Main Dimensions:

- Overall width: 16.0 ± 0.2
- Overall height: 14.0 ± 0.1
- Top edge: 75 (left), 51 (right)
- Right edge: 50
- Bottom edge: 26 (right), 25 (bottom center)
- Left edge: 76 (top), 100 (bottom)
- Bottom-left corner: 1 (radius), 0.5 (width of protrusion)
- Bottom-right corner: 0.13 (M) (width of protrusion)

Details:

- DETAIL A:** A circular detail showing a cross-section of the mold wall. Dimensions include a radius of 0.5, a wall thickness of 0.13 (M), and a height of 15.0. The detail is labeled with 'A' and 'B'.
- DETAIL B:** A rectangular detail showing a cross-section of the mold wall. Dimensions include a width of 0.18, a height of 0.127, and a wall thickness of 0.0127. The detail is labeled with 'B'.

Notes:

- Dimension "a" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

Technical drawing of a square mold assembly. The main view shows a square mold with dimensions: overall width 16.0 ± 0.2 , overall height 14.0 ± 0.1 , and a central square area of 14.0 ± 0.1 . The mold has four circular holes, one on each side, with diameters of 76, 51, 26, and 100. The mold is made of a material with a thickness of 0.5. The mold is shown in a perspective view, with a detail view of the corner labeled "DETAIL A" showing a fillet radius of 0.1 ± 0.1 and a fillet height of 0.5 ± 0.2 . The mold is shown in a perspective view, with a detail view of the corner labeled "DETAIL A" showing a fillet radius of 0.1 ± 0.1 and a fillet height of 0.5 ± 0.2 . The mold is shown in a perspective view, with a detail view of the corner labeled "DETAIL A" showing a fillet radius of 0.1 ± 0.1 and a fillet height of 0.5 ± 0.2 .

DETAIL A

NOTE: Dimension "s" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.