DATA SHEET

CX77140: PA Module for CDMA / AMPS (824–849 MHz)

Applications

- Digital cellular (CDMA)
- Analog cellular (AMPS)
- Wireless local loop (WLL)

Features

- Low voltage positive bias supply
  - 3.2 V to 4.2 V
- Low V_{REF}
  - 2.85 V, nominal
- Good linearity
- High efficiency
- Dual mode operation
- Large dynamic range
- 10-pin package
  - 4 mm x 4 mm x 1.5 mm
- Power down control
- Low power-state control
- InGaP
- IS95/CDMA2000

The CX77140 Power Amplifier Module (PAM) is a dual-mode, fully matched, 10-pin surface mount module developed for Code Division Multiple Access (CDMA) / Advanced Mobile Phone Service (AMPS) cellular handsets and Wireless Local Loop (WLL) applications. This small and efficient power amplifier module packs full coverage of the 824–849 MHz bandwidth into a single compact package. The device meets the stringent IS95 CDMA linearity requirements up to at least 28 dBm output power, and can be driven to levels beyond 31 dBm for high efficiency in FM mode operation. A low current digital pin (VCONT) provides improved efficiency for the low RF power range of operation.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. Output match is realized off-chip and within the module package to optimize efficiency and power performance into a 50 Ω load. This device is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the CX77140 is supplied directly from a three-cell Ni-Cd, a single-cell Li-Ion, or other suitable battery with an output in the range of 3.2 to 4.2 volt. Power down is accomplished by setting the voltage on the low current reference pin to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

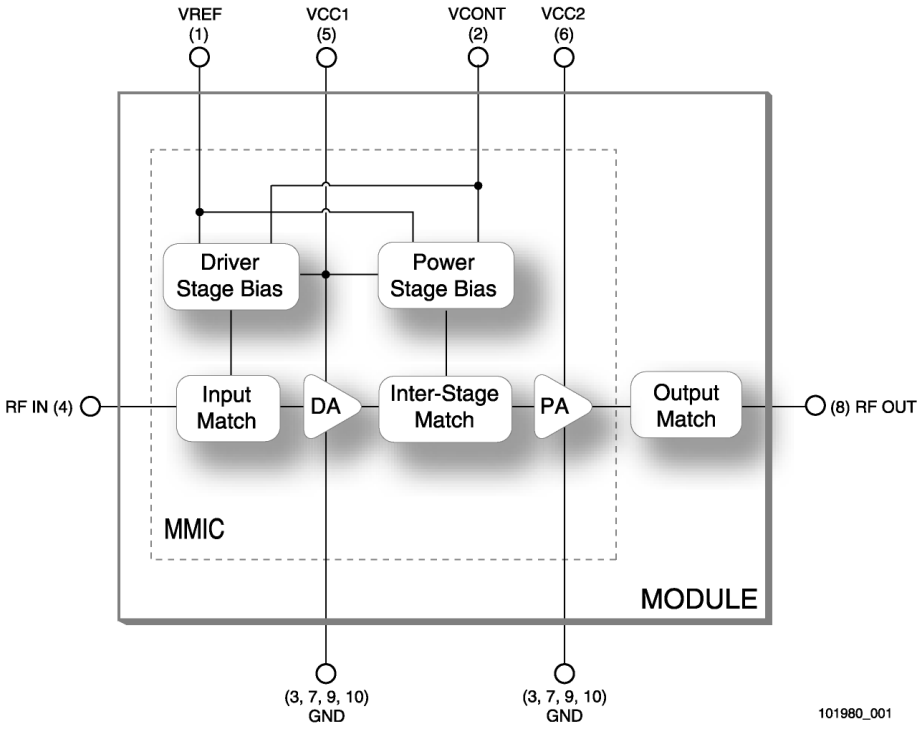


Figure 1. Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the CX77140 Power Amplifier Module. Table 1 lists the absolute maximum ratings. Table 2 specifies the recommended operating conditions for the CX77140 to achieve the electrical performance under the recommended operating conditions listed in Table 4. Table 3 is a power range truth table.

Table 1. Absolute Maximum Ratings [1]

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power	P_{IN}	—	4.0	7.0	dBm
Supply Voltage	V_{CC}	—	3.4	6.0	Volts
Reference Voltage	V_{REF}	—	2.85	3.1	Volts
Case Operating Temperature	T_C	–30	25	+110	°C
Case Storage Temperature	T_{STG}	–55	—	+125	°C

[1] No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.

Table 2. Recommended Operating Conditions

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage		V_{CC}	3.2	3.4	4.2	Volts
Reference Voltage	PA On	V_{REF}	2.75	2.85	2.95	Volts
	PA Off	V_{REF}	—	< 0.5	—	
Mode Input Impedance >2.5 kΩ	High Bias Mode	V_{CONT}	0.0	0.5	1.0	Volts
	Low Bias Mode	V_{CONT}	2.0	2.5	3.0	
Operating Frequency		F_O	824.0	836.5	849.0	MHz
Case Operating Temperature		T_C	–30	—	+85	°C

Table 3. Power Range Truth Table

Power Mode	V_{REF}	V_{CONT}	Range
High Power	2.85 V	0.5 V	16 dBm to 28.0 dBm
Low Power	2.85 V	2.5 V	≤ 16 dBm
Shut Down	0.0 V	0.0 V	—

Table 4. Electrical Specifications for CDMA / AMPS Nominal Operating Conditions [1]

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	V_{CONT} = 2.5 V P_O = 16 dBm	23.0	26.0	27.0	dB
		G_{HIGH}	V_{CONT} = 0.5 V P_O = 28 dBm	27.0	29.0	31.0	
	Analog Mode	G_P	V_{CONT} = 0.5 V P_O = 31 dBm	26.5	28.0	30.0	
Power Added Efficiency	Digital Mode	PAE_{LOW}	V_{CONT} = 2.5 V P_O = 16 dBm	7.0	8.0	—	%
		PAE_{HIGH}	V_{CONT} = 0.5 V P_O = 28 dBm	37.0	40.0	—	
	Analog Mode	PAE_A	V_{CONT} = 0.5 V P_O = 31 dBm	48.0	54.0	—	
Total Supply Current		I_{CC_LOW}	P_O = 16 dBm	—	145	150	mA
		I_{CC_HIGH}	P_O = 28 dBm	—	460	505	
Quiescent Current		I_{Q_LOW}	V_{CONT} = 2.5 V	30	50	65	mA
		I_{Q_HIGH}	V_{CONT} = 0.5 V	65	75	120	
Reference Current		I_{REF}	—	—	4.5	5.0	mA
Control Current		I_{CONT}	V_{CONT} = 2.5 V	—	0.25	0.7	mA
Total Supply current in Power-down Mode		I_{PD}	V_{CC} = 3.4 V V_{REF} = 0 V	—	3.0	5.0	µA
Adjacent Channel Power [2][3]	885 kHz offset	$ACP1_{LOW}$	V_{CONT} = 2.5 V $P_O \leq$ 16 dBm	—	–49.0	–46.0	dBc
		$ACP1_{HIGH}$	V_{CONT} = 0.5 V $P_O \leq$ 28 dBm	—	–50.0	–48.0	
	1.98 MHz offset	$ACP2_{LOW}$	V_{CONT} = 2.5 V $P_O \leq$ 16 dBm	—	–65.0	–59.0	
		$ACP2_{HIGH}$	V_{CONT} = 0.5 V $P_O \leq$ 28 dBm	—	–61.0	–58.5	
Harmonic Suppression	Second	F_O2	$P_O \leq$ 31.0 dBm	—	–35.0	–29.0	dBc
	Third	F_O3	$P_O \leq$ 31.0 dBm	—	–50.0	–35.0	
Noise Power in RX Band 869-894 MHz		RxBN	$P_O \leq$ 28.0 dBm	—	–137	–136	dBm/Hz
Noise Figure		NF	—	—	5.0	—	dB
Input Voltage Standing Wave Ratio [4]		VSWR	—	—	—	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR all phases	—	—	–60.0	dBc
Ruggedness – No damage [5]		Ru	$P_O \leq$ 28.0 dBm	10:1	—	—	VSWR

[1] V_{CC} = +3.4 V, V_{REF} = +2.85 V, Freq = 836.5 MHz, T_C = +25 °C, unless otherwise specified.

[2] ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

[3] CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For CDMA2000, back-off of 0.5 dB output power is required.

[4] For low power mode, VSWR = 2.5:1.

[5] All phases, time = 10 seconds.

Table 5. Electrical Specifications for CDMA / AMPS Recommended Operating Conditions [1]

Characteristics		Symbol	Condition	Minimum	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	V_{CONT} = 2.5 V P_O = 16 dBm	22.5	28.0	dB
		G_{HIGH}	V_{CONT} = 0.5 V P_O = 28 dBm	26.0	32.0	
	Analog Mode	G_P	V_{CONT} = 0.5 V P_O = 31 dBm	24.5	31.0	
Adjacent Channel Power [2][3]	885 kHz offset	$ACP1_{LOW}$	V_{CONT} = 2.5 V $P_O \leq$ 16 dBm	—	–43.5	dBc
		$ACP1_{HIGH}$	V_{CONT} = 0.5 V $P_O \leq$ 28 dBm	—	–44.0	
	1.98 MHz offset	$ACP2_{LOW}$	V_{CONT} = 2.5 V $P_O \leq$ 16 dBm	—	–56.0	
		$ACP2_{HIGH}$	V_{CONT} = 0.5 V $P_O \leq$ 28 dBm	—	–56.0	
Harmonic Suppression	Second	F_O2	$P_O \leq$ 31.0 dBm	—	–28.5	dBc
	Third	F_O3	$P_O \leq$ 31.0 dBm	—	–35.0	
Noise Power in RX Band 869-894 MHz		RxBN	$P_O \leq$ 28.0 dBm	—	–134	dBm/Hz
Noise Figure		NF	—	—	7	dB
Input Voltage Standing Wave Ratio		VSWR	—	—	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR all phases	—	–60.0	dBc
Ruggedness – No damage [4]		Ru	$P_O \leq$ 28.0 dBm	10:1	—	VSWR

[1] Per Table 2, unless otherwise specified.

[2] ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

[3] CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For CDMA2000, 0.5 dB back-off of output power is required.

[4] All phases, time = 10 seconds.

Characterization Data

The graphs in Figure 2 through Figure 8 illustrate the characteristics of a typical CX77140 power amplifier designed for operation in the CDMA/AMPS frequency band (824–849 MHz). This amplifier was selected by characterizing a group of devices and choosing a part with average electrical performance for both nominal and the full range of recommended operating conditions, including worst case limits.

The graphs illustrate the digital signal characteristics of the CX77140. Shown are power sweep characteristics for key performance parameters over temperature and frequency, up to 28 dBm output power. The data was taken up to and including 16 dBm output power with the bias mode control pin setting of V_{CONT} = 2.5 volts. Beyond 16 dBm output power, the V_{CONT} was set to 0 volts.

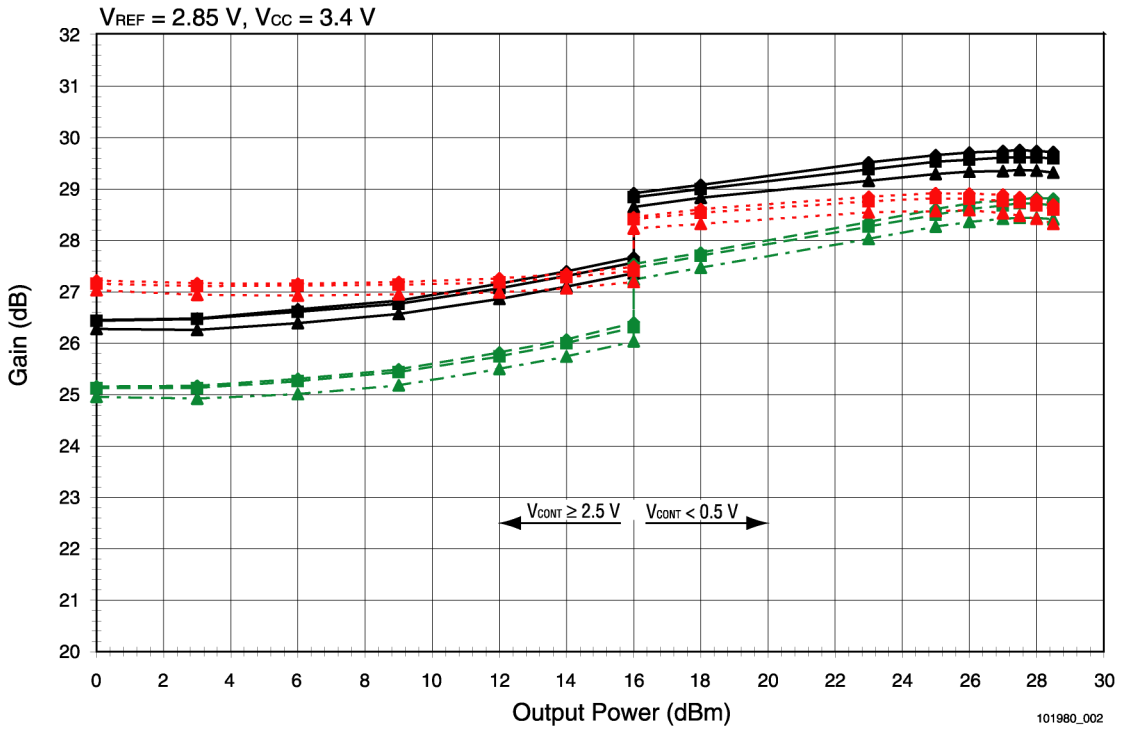
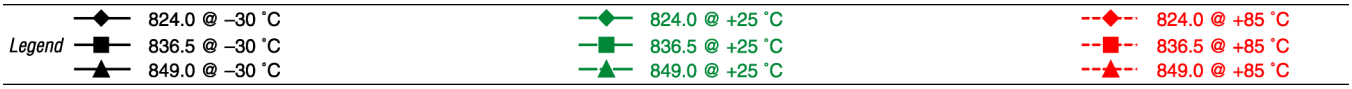


Figure 2. Digital Mode Gain vs. Output Power



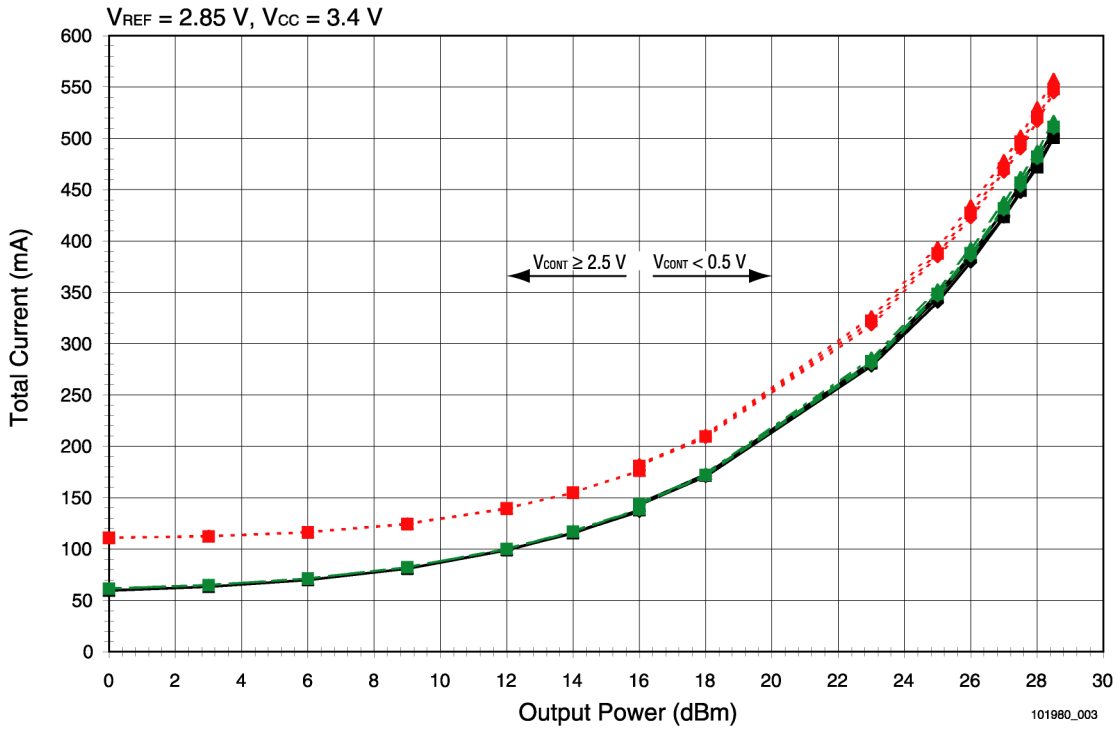


Figure 3. Primary Bias Current vs. Output Power

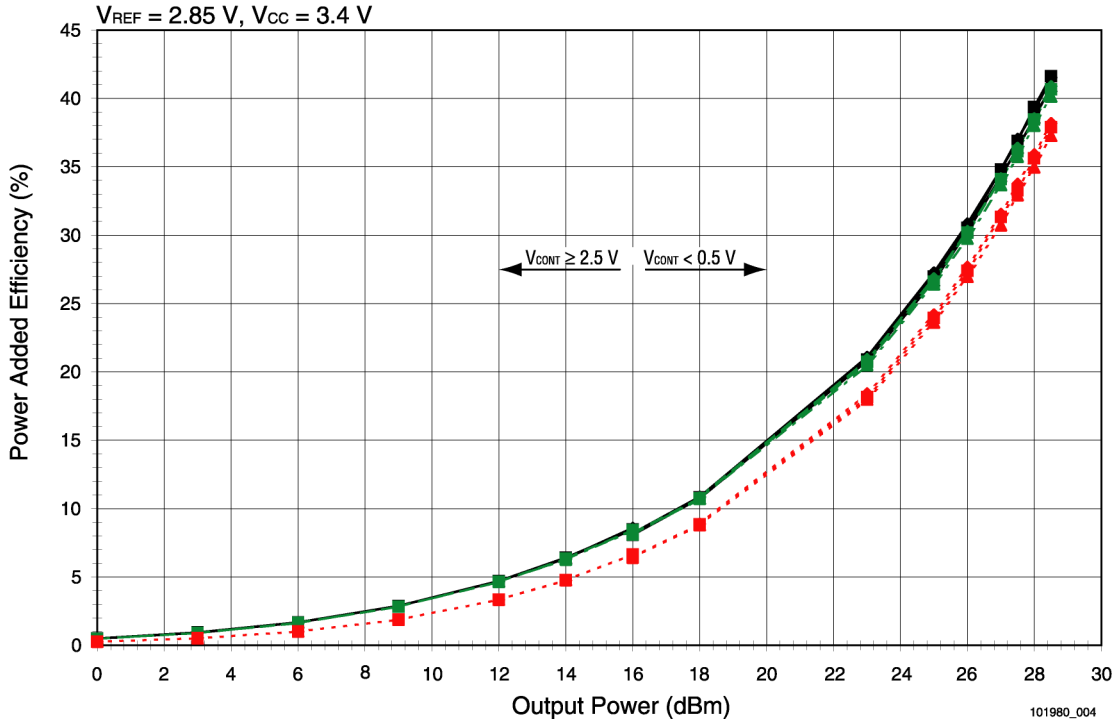


Figure 4. Power Added Efficiency vs. Output Power

Legend	824.0 @ –30 °C	824.0 @ +25 °C	824.0 @ +85 °C
	836.5 @ –30 °C	836.5 @ +25 °C	836.5 @ +85 °C
	849.0 @ –30 °C	849.0 @ +25 °C	849.0 @ +85 °C

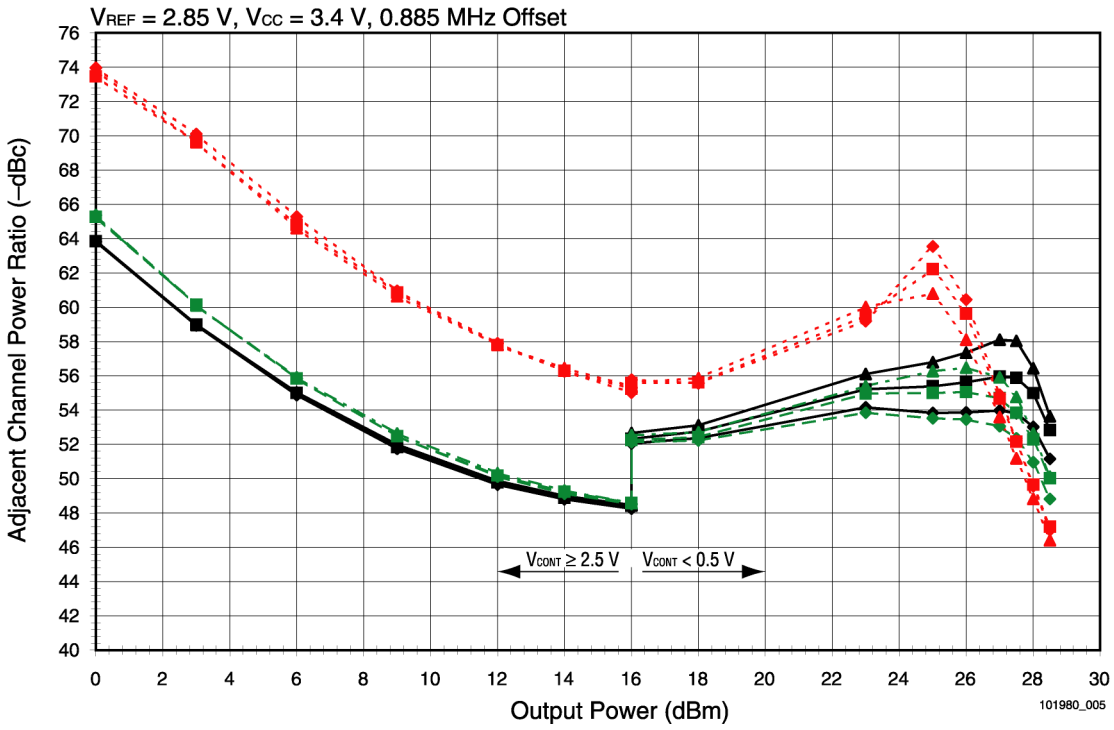


Figure 5. Adjacent Channel Power for 0.885 MHz Offset vs. Output Power

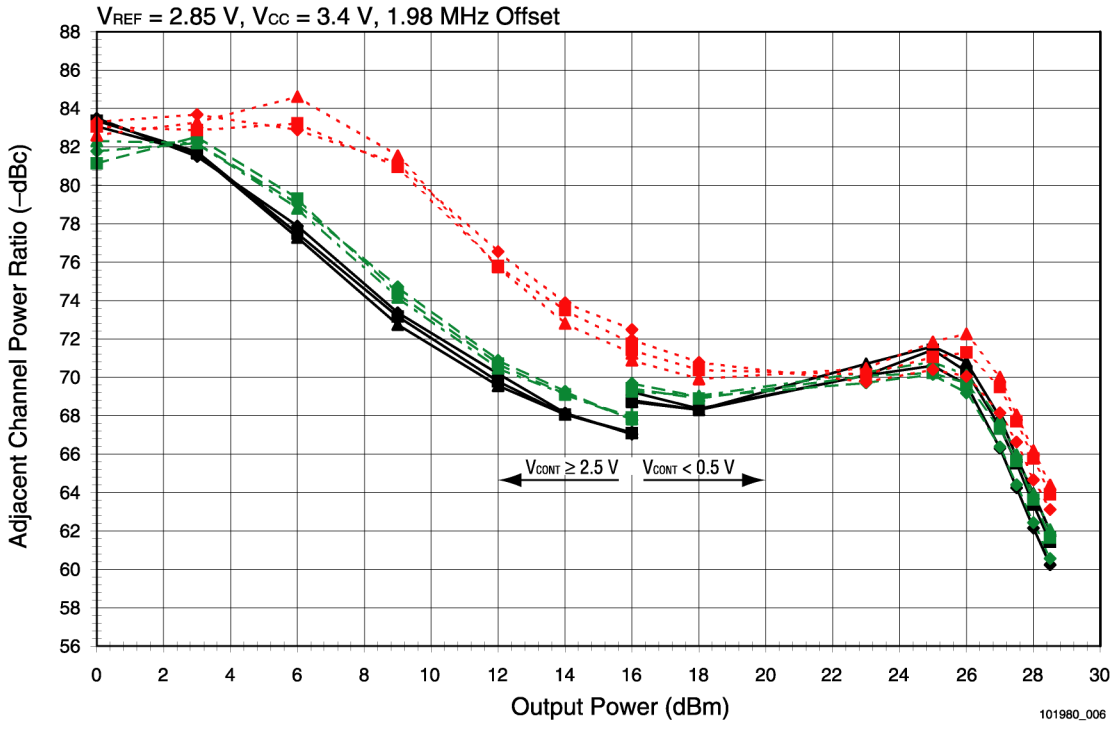


Figure 6. Adjacent Channel Power for 1.98 MHz Offset vs. Output Power

Legend	824.0 @ –30 °C	824.0 @ +25 °C	824.0 @ +85 °C
	836.5 @ –30 °C	836.5 @ +25 °C	836.5 @ +85 °C
	849.0 @ –30 °C	849.0 @ +25 °C	849.0 @ +85 °C

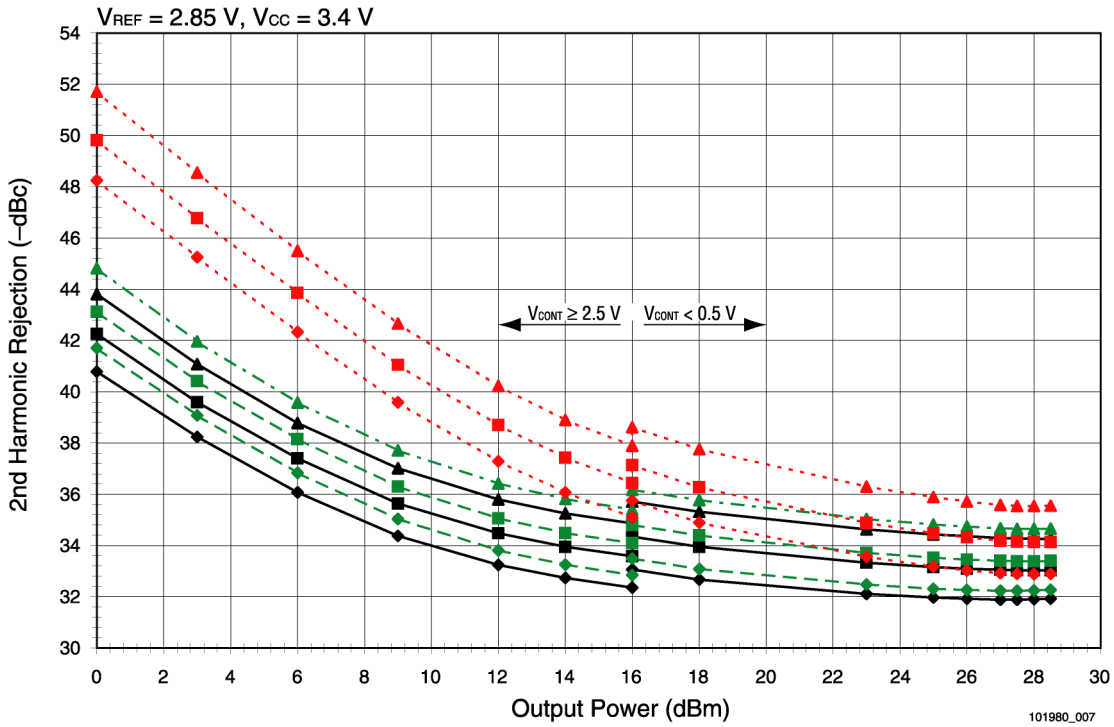


Figure 7. Second Harmonic Rejection vs. Output Power

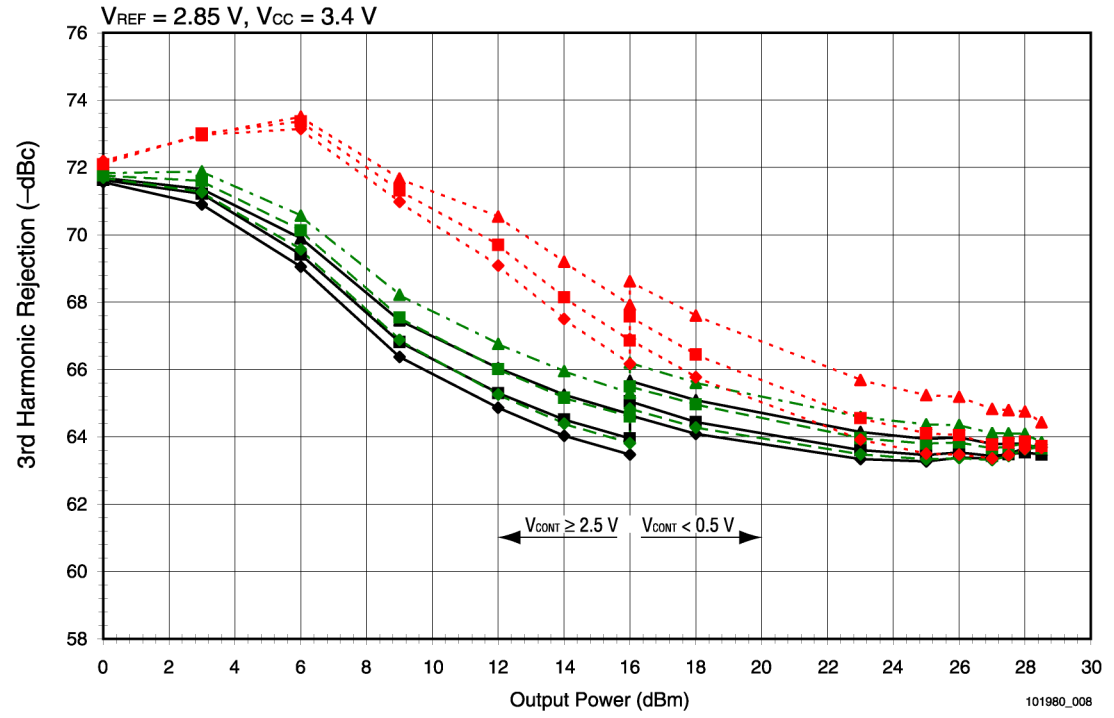


Figure 8. Third Harmonic Rejection vs. Output Power

Legend	824.0 @ –30 °C	824.0 @ +25 °C	824.0 @ +85 °C
	836.5 @ –30 °C	836.5 @ +25 °C	836.5 @ +85 °C
	849.0 @ –30 °C	849.0 @ +25 °C	849.0 @ +85 °C

Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the CX77140, the evaluation board schematic and diagrams are included for preliminary analysis and design. Figure 9 shows the basic schematic of the board for the 824 MHz to 849 MHz range and Figure 10 shows the layout of the board assembly.

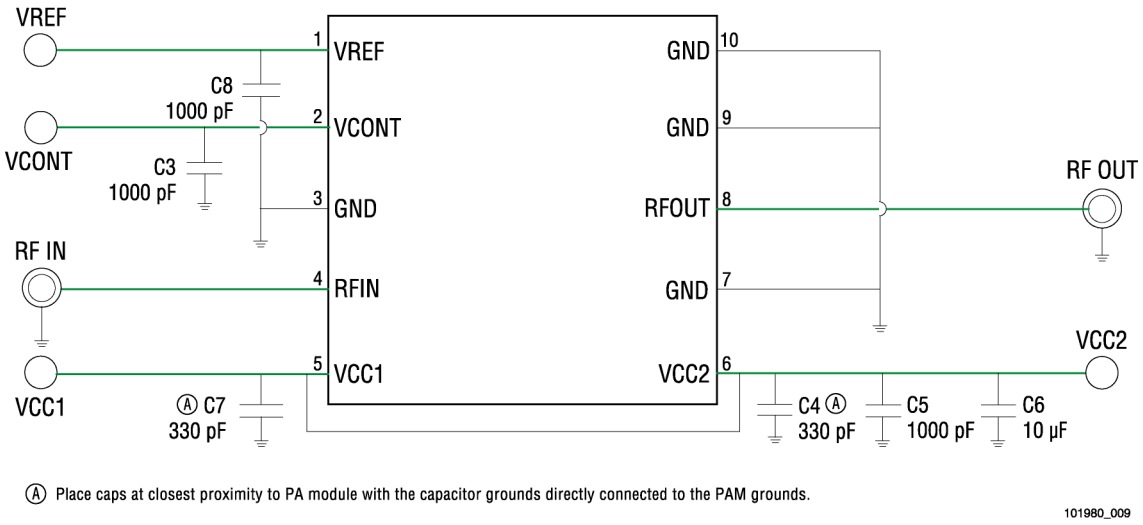


Figure 9. Evaluation Board Schematic

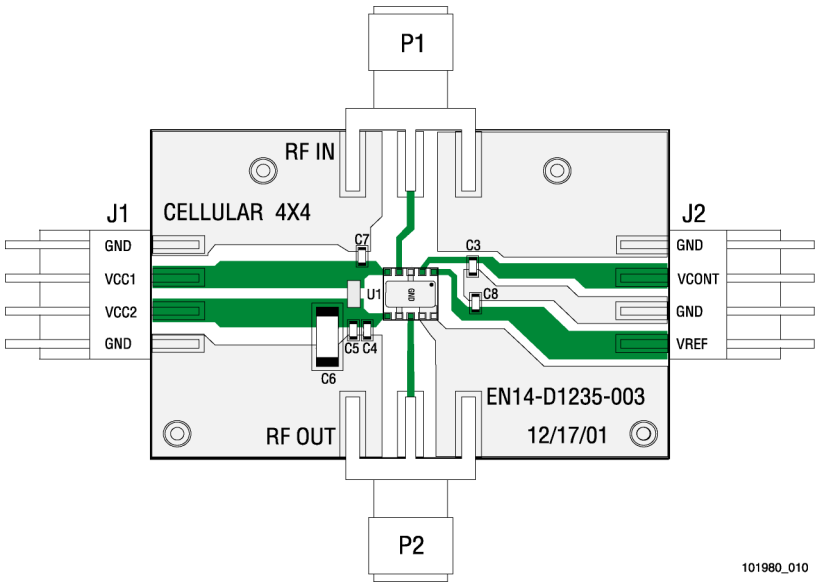
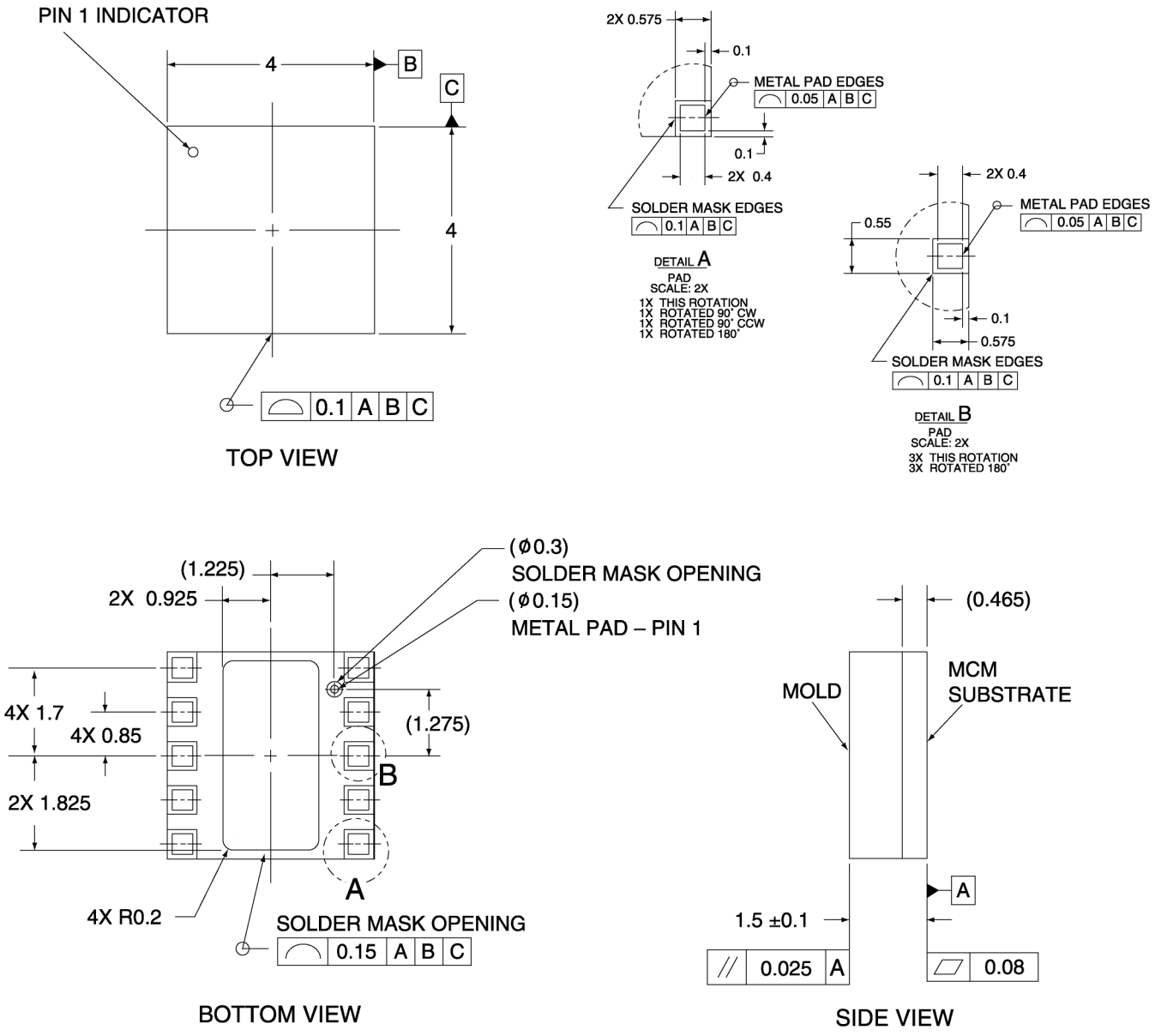


Figure 10. Evaluation Board Assembly Diagram

Package Dimensions and Pin Descriptions

The CX77140 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 11 is a mechanical drawing of the pad layout for this package. Figure 12 shows the pin names and numbering convention, which starts with pin 1 in the upper left, as indicated, and increments counter-clockwise around the package. Figure 13 illustrates typical case markings.



NOTES: unless otherwise specified
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M–1994.
3. SEE APPLICABLE BONDING DIAGRAM AND DEVICE ASSEMBLY DRAWING FOR DIE AND COMPONENT PLACEMENT.
4. PADS ARE METAL DEFINED; THE CENTER PAD IS SOLDER MASK DEFINED.

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Figure 11. CX77140 Package Dimensional Drawing

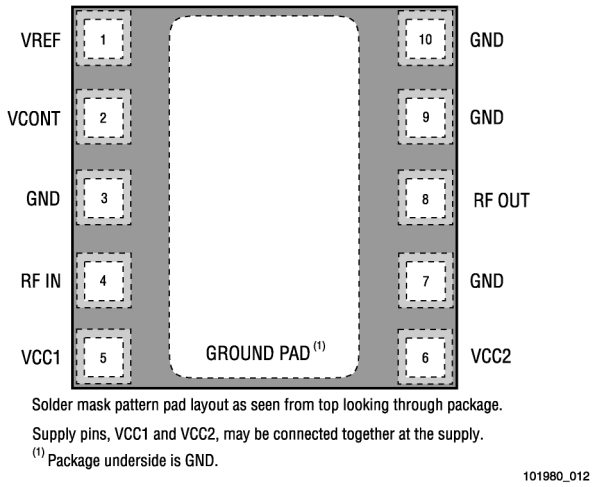

Figure 12. Pin Configuration and Pin Names (Top View)

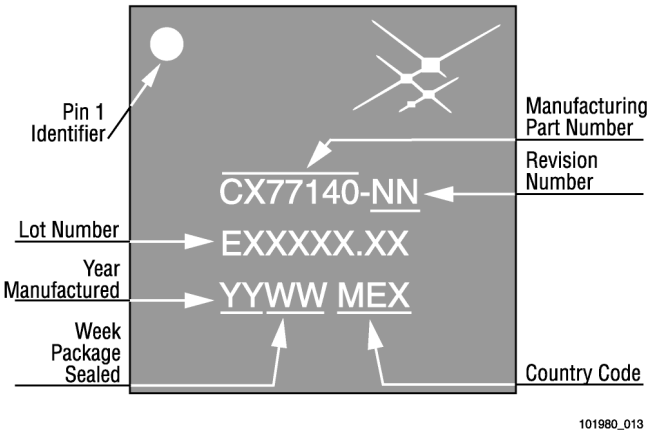

Figure 13. Typical Case Markings

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CX77140 is capable of withstanding an MSL3/240 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 240 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 240 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Skyworks Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J–STD–020B*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Skyworks Application Note: Tape and Reel, Document Number 101568.*

Electrostatic Discharge Sensitivity

The CX77140 is a Class 2 device. Figure 14 lists the Electrostatic Discharge (ESD) immunity level for each pin of the CX77140 product. The numbers in Figure 14 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation.

ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

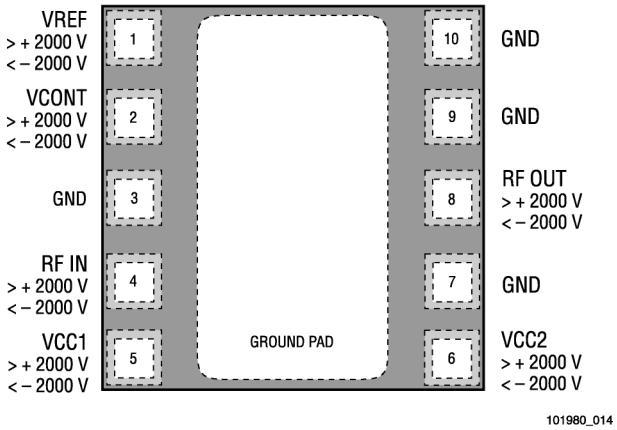

Figure 14. ESD Sensitivity Areas (Top View)

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in Table 5.

Table 5. Precautions for Handling GaAs IC-based Products to Avoid Induced Damage

Personnel Grounding	Facility
Wrist Straps	Relative Humidity Control and Air Ionizers
Conductive Smocks, Gloves and Finger Cots	Dissipative Floors (less than 10^9 Ω to GND)
Antistatic ID Badges	
Protective Workstation	**Protective Packaging & Transportation**
Dissipative Table Tops	Bags and Pouches (Faraday Shield)
Protective Test Equipment (Properly Grounded)	Protective Tote Boxes (Conductive Static Shielding)
Grounded Tip Soldering Irons	Protective Trays
Conductive Solder Suckers	Grounded Carts
Static Sensors	Protective Work Order Holders

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77140	CX77140		4x4LM	–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
A		September 8, 2003	Initial Release
B		December 3, 2003	Revise: Figure 1

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.

Application Note: Tape and Reel, Document Number 101568

Standard SMT Reflow Profiles: JEDEC Standard J–STD–020B.