CHRONTEL

CH7203

MPEG to TV Encoder with 16-bit Input

Features

- Outputs to NTSC, PAL (B, D, G, H, I) and PAL-60
- 16-bit YCrCb (4:2:2) input format
- Simultaneous composite/S-video outputs
- Triple 9-bit video DACs
- 27 MHz DAC operating frequency eliminates the need for 1/sinc(x) correction filter
- Low-jitter phase-locked loop circuitry operates using a low-cost 14.31818 MHz crystal
- 40.5 or 33.9 MHz video decoder clock output
- 16.934 or 11.289 MHz audio decoder clock output
- 13.5 MHz and 27 MHz video pixel clock outputs
- Optimized luminance and chrominance internal filters for NTSC and PAL
- HSYNC* and VSYNC* outputs for master mode operation
- Sleep mode
- CMOS technology in 44-pin PLCC
- 5V single-supply operation

Description

The CH7203 video encoder integrates a dual PLL clock generator and a digital NTSC/PAL video encoder. By generating all essential clock signals for MPEG playback, and converting digital video inputs to either NTSC or PAL video signals, the CH7203 is an essential component of any low-cost solution for video-CD playback machines.

The CH7203 dual PLL clock synthesizer generates all clocks and timing signals from a 14.31818 MHz reference crystal (see application note 19 "Tuning Clock Outputs" for selection and tuning of the 14.31818 MHz crystal). The CH7203 generates a 40.5 or 33.9 MHz video decoder clock, 13.5 MHz and 27 MHz video pixel clocks, and a 16.934 or 11.289 MHz audio decoder clock. Timing signals from the PLLs are used to generate the horizontal and vertical sync signals which enable operating the CH7203 in master mode.

The fully digital video encoder is pin-programmable to generate either a 525-line NTSC or a 625-line PAL compatible video signal. It also features a logic selectable sleep mode which turns the encoder off while leaving both PLL's running.

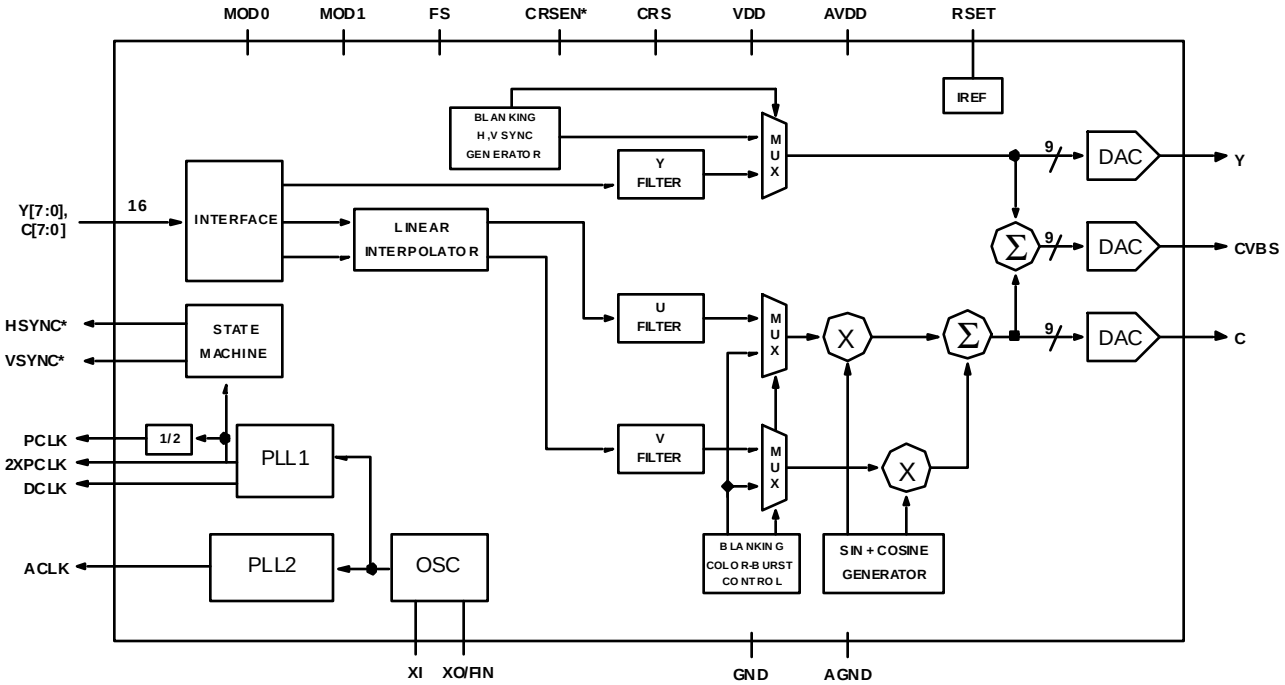


Figure 1: Functional Block Diagram

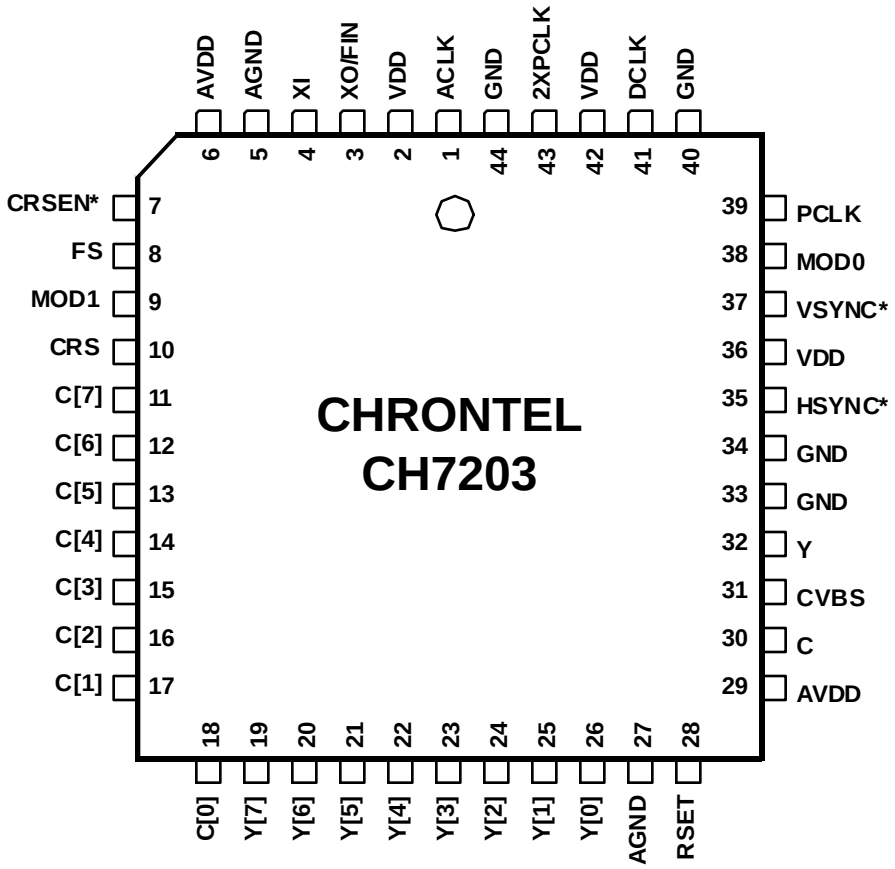


Figure 2: CH7203 Pinout Diagram

Table 1. Pin Descriptions

Pin	Type	Symbol	Description
1	Out	ACLK	**Audio Decoder Clock Output** 16.934 MHz or 11.289 MHz clock output (selectable by FS) for MPEG audio decoder operation. The output swing is 5V.
2, 36, 42	Power	VDD	**Digital Supply Voltage** These pins supply the 5V power to the digital section of the CH7203.
3	In	XO/FIN	**Crystal Output or External F_{REF} Input[1]** A 14.31818 MHz (± 50 ppm) parallel resonance crystal may be attached between XO/FIN and XI. An external CMOS compatible clock can be connected to XO/FIN as an alternative.
4	In	XI	**Crystal Input [1]** A 14.31818 MHz (± 50 ppm) parallel resonance crystal should be attached between XI and XO/FIN. However, if an external CMOS clock is attached to XO/FIN, XI should be connected to ground.
5, 27	Power	AGND	**Analog ground** These pins provide the ground reference for the analog section of the CH7203. These pins MUST be connected to the system ground to prevent latchup.
6,29	Power	AVDD	**Analog Supply Voltage** These pins supply the 5V power to the analog section of the CH7203.
7	In	CRSEN*	**Cr Select Enable.** Internally pulled-up. CRSEN*=0, Cr, Cb data sequence is specified by the CRS pin. CRSEN*=1, Cr, Cb data sequence is specified by the CH7203's internal default condition: Horizontal count = even, data is Cb; data is Cr otherwise. State of CRS is ignored when CRSEN*=1. See **Figure 6** on page 7.
8	In	FS	**Frequency Select.** Internally pulled-up FS = 1 (default), then DCLK = 40.5 MHz, ACLK = 16.934 MHz FS = 0, then DCLK = 33.9 MHz, ACLK = 11.289 MHz
9	In	MOD1	**Mode bit 1 -** Internally pulled-up This input works in conjunction with the MOD0 input to select NTSC, PAL, or Sleep mode functions. Refer to **Table 3, "Video Encoder Modes," on page 6** for details.
10	In	CRS	**Cr Select.** When CRSEN*=0, CRS specifies the CrCb data sequence. CRS is an alternating signal. CRS=1 indicates that C[7:0] carry the Cr data. C[7:0] carry the Cb data otherwise. See **Figure 7** on page 8.
11 – 18	In	C[7:0]	**Video Input** These pins accept the "CrCb" data of the YCrCb (4:2:2) digital video format. The Cb & Cr data appear alternately. The sequence of the Cb, Cr data is either predefined by the internal horizontal counter (even = Cb, odd = Cr) or as specified by pin CRS (data is Cr for CRS=1 and Cb otherwise. For more details, please refer to the timing diagram shown in **Figure 6** on page 7. Cb & Cr have a nominal range of 16–240, with 128 equal to zero.

Note: 1. Please refer to crystal manufacturer specifications for proper load capacitances. The optional variable tuning capacitor is required only if the crystal oscillation frequency cannot be controlled to the required accuracy. The capacitance value for the tuning capacitor should be obtained from the crystal manufacturer. For further information, request a copy of **Application Note AN-19, "Tuning Clock Outputs.**"

Table 2. Pin Descriptions (continued)

Pin	Type	Symbol	Description
19-26	In	Y[7:0]	**Video Input** These pins accept the "Y" data of the YCrCb (4:2:2) digital video format. For more details, please refer to the timing diagram shown in **Figure 7** on page 8. Y has a nominal range of 16-235.
28	In	RSET	**Reference Resistor** A 360 Ω resistor with short and wide traces should be attached between RSET and ground. No other connections should be made to this pin.
30	Out	C	**Chrominance Output** A 75 Ω termination resistor with short traces should be attached between C and ground for optimum performance.
31	Out	CVBS	**Composite Output** A 75 Ω termination resistor with short traces should be attached between CVBS and ground for optimum performance.
32	Out	Y	**Luminance Output** A 75 Ω termination resistor with short traces should be attached between Y and ground for optimum performance.
33, 34, 40, 44	Power	GND	**Digital Ground** These pins provide the ground reference for the digital section of the CH7203. These pins MUST be connected to the system ground through ***independent*** ground vias.
35	Out	HSYNC*	**Horizontal Sync Output** The horizontal sync output is generated by the CH7203 for master mode operation. HSYNC* is an active low signal with a 5V output swing. For additional information, please refer to the timing diagrams shown in **Figures 5** and **6** on page 7.
37	Out	VSYNC*	**Vertical Sync Output** The vertical sync output is generated by the CH7203 for master mode operation. VSYNC* is an active low signal with a 5V output swing. For additional information, please refer to the timing diagrams shown in **Figures 5** and **7** on page 7 and 8.
38	In	MOD0	**Mode bit 0** - internally pulled-up This input works in conjunction with the MOD1 input to select NTSC, PAL, or Sleep Mode functions. Refer to **Table 3, "Video Encoder Modes," on page 6** for details.
39	Out	PCLK	**Video Pixel Clock Output** 13.5 MHz clock output. The output swing is 5V.
41	Out	DCLK	**MPEG Decoder Clock Output** 40.5 MHz or 33.9 MHz clock output (selectable by FS). The output swing is 5V.
43	Out	2XPCLK	**Double Pixel Clock Output** 27 MHz clock output. The output swing is 5V.

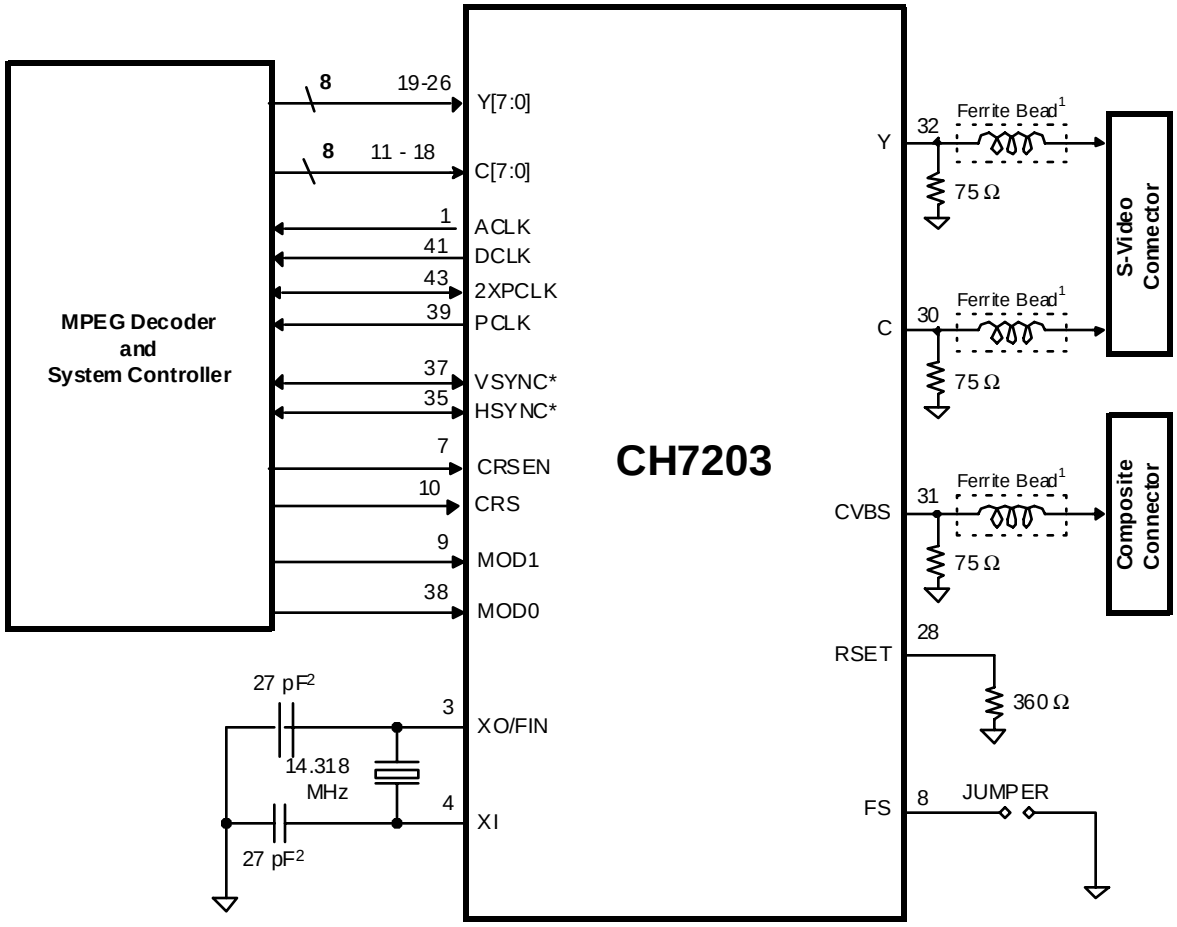


Figure 3: CH7203 Interface Diagram

Note: **1.** Please refer to the Optional Output Filter diagram below

2. The proper value of these capacitors depends on the crystal manufacturer's specifications. Please refer to AN06 for the details of the calculation.

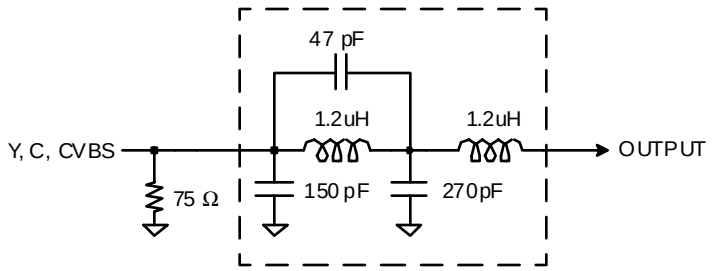


Figure 4: Optional Output Filter

General Description

The CH7203 is a fully integrated solution for converting 16-bit YCrCb (4:2:2) digital video inputs into high-quality NTSC or PAL video signals while generating all essential clock signals for MPEG playback. All essential circuitry for this conversion and clock generation (Dual PLL's, linear interpolator, digital filters, NTSC/PAL encoder, DAC's) are contained in the CH7203 making it an essential component of any low-cost solution for video-CD playback machines. Refer to the Block Diagram on page 1 and the Interface Diagram on page 5.

Functional Description

The encoded luminance (Y) and color-difference (U,V) are interpolated, and filtered through digital filters to minimize aliasing problems. The filtered signals go to the digital encoder where they are transformed to composite and S-video outputs, and then they are converted by the three 9-bit DACs to analog outputs.

16-bit YCrCb (4:2:2) Input

Y data is input through the Y[7:0] inputs and CrCb data is multiplexed through the C[7:0] inputs. When CRSEN* = 1, the Cr Select input, CRS, is ignored, and all even horizontal pixels are Cb data and all odd horizontal pixels are Cr. Refer to **Figure 6** on page 7 for the definition of "even" and "odd" pixels. When CRSEN* = 0, the alternating CRS signal specifies the CrCb sequence. CRS = 1 indicates C[7:0] carries Cr data, and CRS = 0 indicates C[7:0] carries Cb data.

Clock/Data/Synchronization Timing

The CH7203 not only works as an NTSC/PAL encoder, it also supplies the necessary clocks (1X pixel, 2X pixel, video system, and audio) and synchronization (HSYNC* and VSYNC*) signals to other building blocks in the video system. For this reason, the CH7203 works **only** in the Master mode.

It is important to note the CH7203 does not have a "pixel clock" input pin. Therefore, the timing issues related to video pixel data being supplied from, for example, the MPEG decoder, to the CH7203 (pins Y[7:0] and C[7:0]) need to be clarified. Assume the pixel synchronization of a system is based on the 2X pixel clock (2XPLCK). In this type of design, 2XPCLK is distributed across the entire video system, and it is also used to latch the incoming data appearing at pins Y[7:0] and C[7:0]. **Figure 7** on page 8 shows all timing referenced to the 2XPCLK output signal (loaded with 50pF).

Video Encoder Modes

Combinations of the two signals MOD1 and MOD0 select the various power saving modes as shown below.

Table 3 • Video Encoder Modes

MOD1	MOD0	Video Encoder Mode
1	1	NTSC
1	0	PAL
0	1	PAL-60
0	0	Sleep mode (Encoder off, both PLLs running)

Frequency Select Modes

The frequency select input FS affects the DCLK and ACLK outputs as shown below:

FS = 1 (default) DCLK = 40.5 MHz, ACLK = 16.934 MHz

FS = 0 DCLK = 33.9 MHz, ACLK = 11.289 MHz

Timing Diagrams

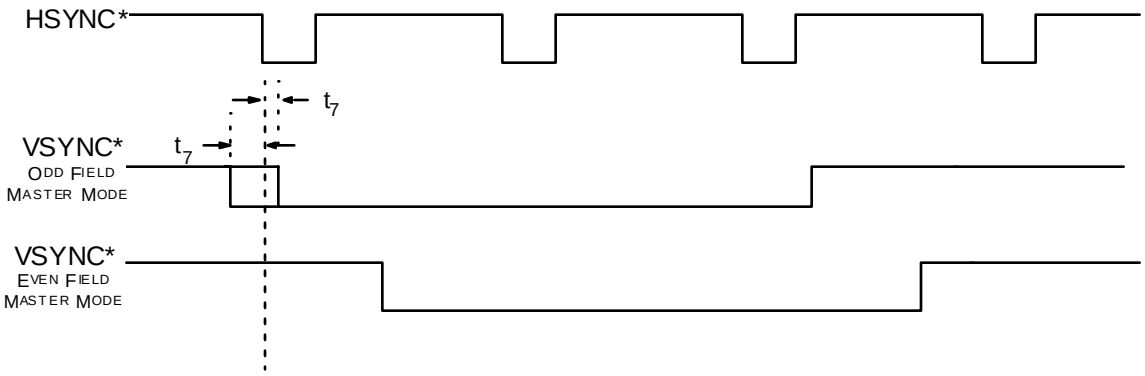


Figure 5: HSYNC* and VSYNC* Timing

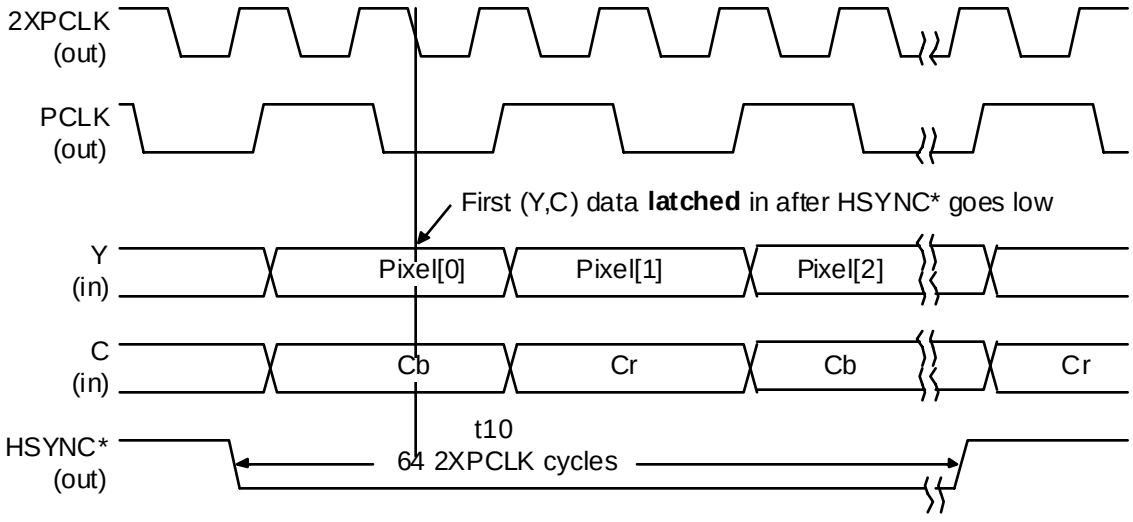


Figure 6: Cb, Cr Sequence Diagram

Data is latched into the device on the falling edge of 2XPCLK, when PCLK is low.

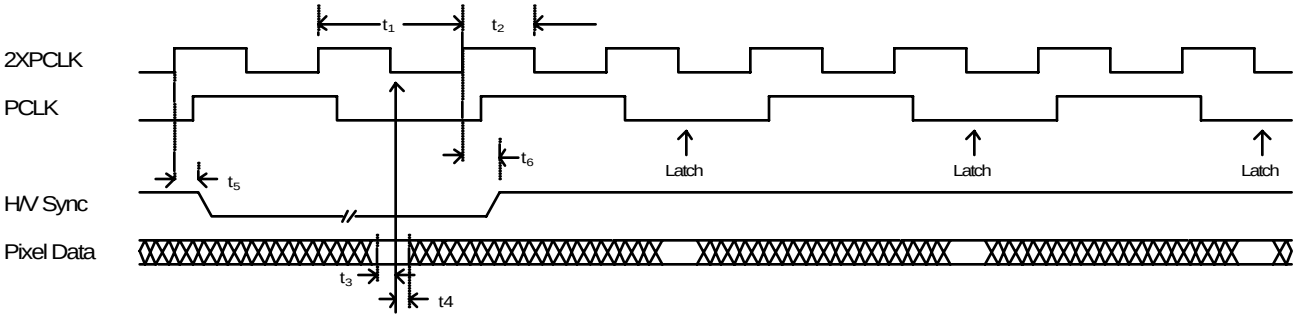


Figure 7: Clock/Data/Synchronization Timing Diagram

Note: Refer to **Table 8** on page 14 for timing values

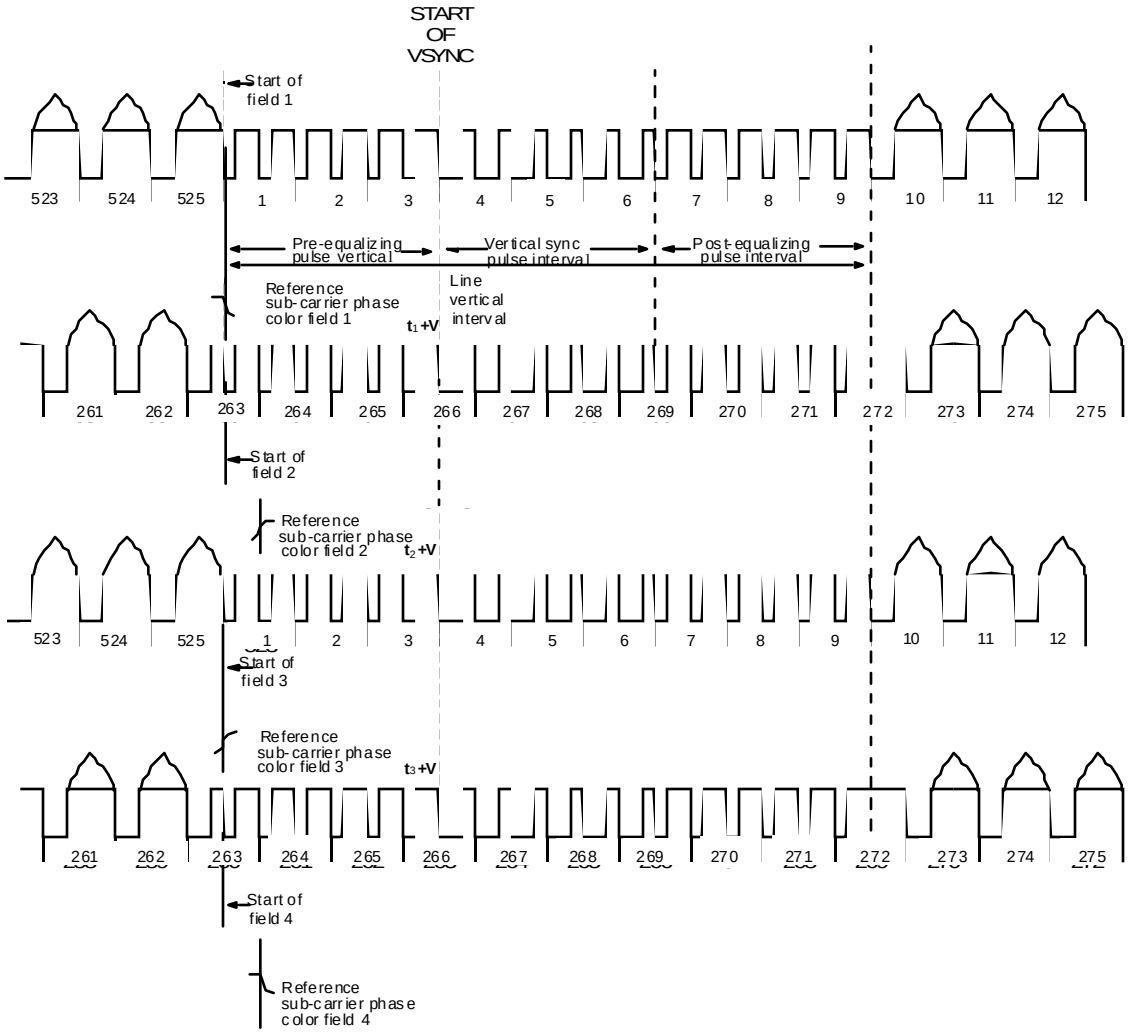


Figure 8: Interlaced NTSC Timing Diagram

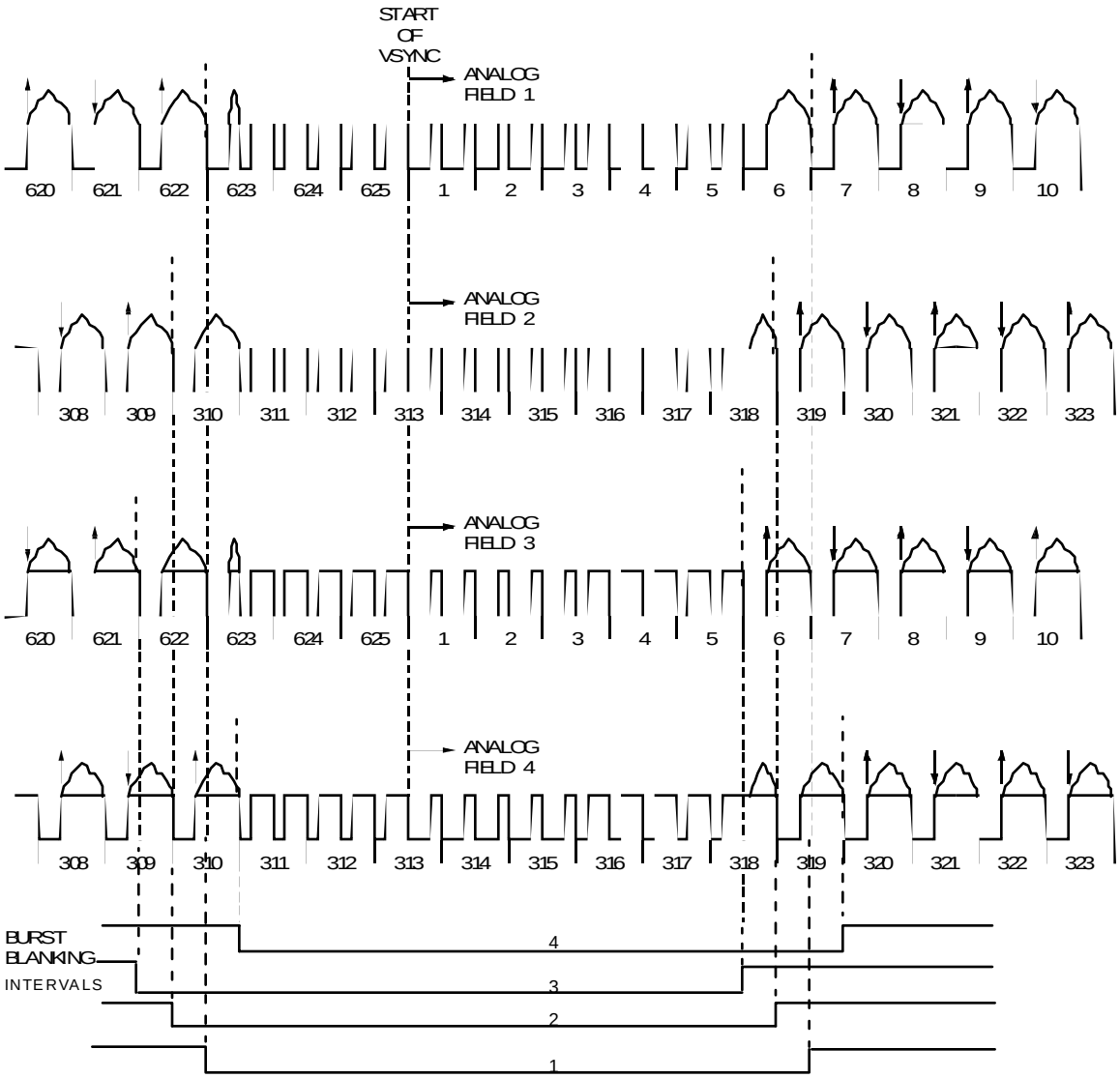
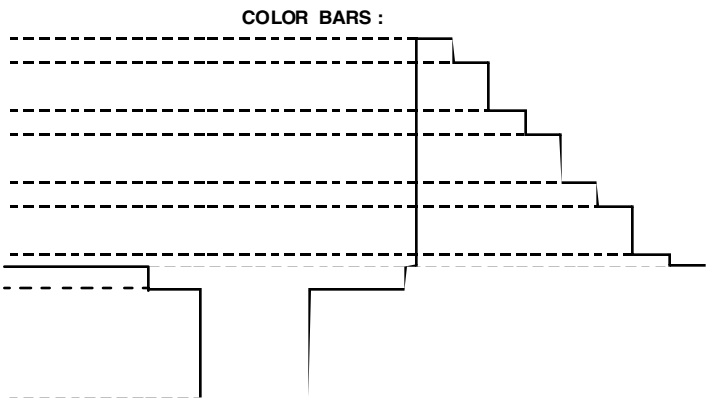


Figure 9: Interlaced PAL Timing Diagram

Color / Level	mA	V
White	26.59	0.997
Yellow	24.59	0.922
Cyan	21.30	0.799
Green	19.30	0.724
Magenta	16.15	0.606
Red	14.15	0.531
Blue	11.00	0.413
Black	9.00	0.338
Blank	7.58	0.284
Sync	0.00	0.000

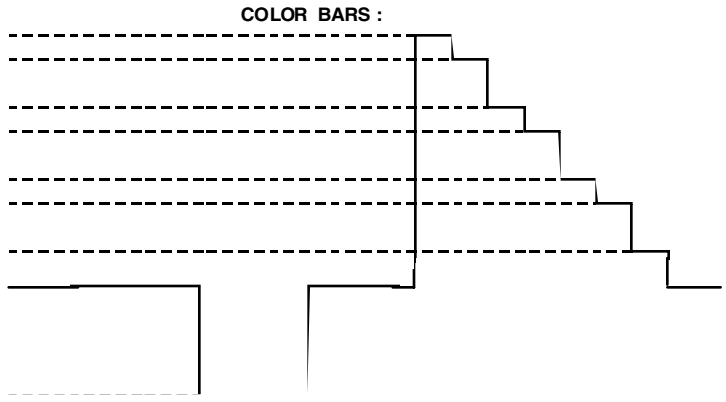


Note: 1 100% amplitude, 100% saturation color bars are shown

Note: 2 Vref = 1.235V, RSET = 360Ω, 75Ω doubly terminated load

Figure 10: NTSC Y (Luminance) Output Waveform

Color / Level	mA	V
White	26.83	1.006
Yellow	24.69	0.926
Cyan	21.19	0.795
Green	19.05	0.715
Magenta	15.70	0.589
Red	13.57	0.509
Blue	10.21	0.383
Blank	8.08	0.303
Sync	0.00	0.000

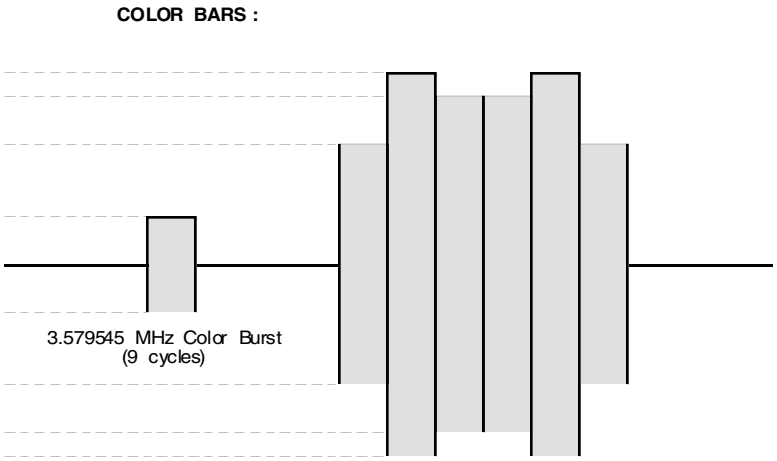


Note: 1 100% amplitude, 100% saturation color bars are shown

Note: 2 Vref = 1.235V, RSET = 360Ω, 75Ω doubly terminated load

Figure 11: PAL Y (Luminance) Video Output Waveform

Color / Level	mA	V
Cyan / Red	25.37	0.951
Green / Magenta	24.59	0.922
Yellow / Blue	22.16	0.831
Peak Burst	18.15	0.681
Blank	14.294	0.536
Peak Burst	10.44	0.391
Yellow / Blue	6.43	0.241
Green / Magenta	4.00	0.150
Cyan / Red	3.21	0.121

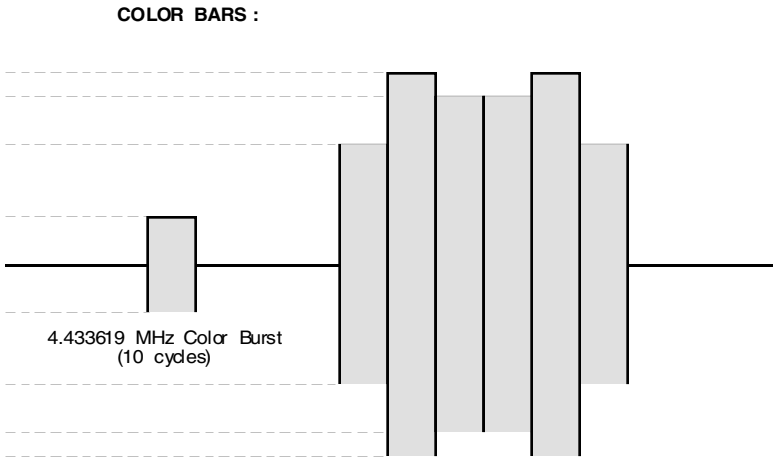


Note: 1 100% amplitude, 100% saturation color bars are shown

Note: 2 Vref = 1.235V, RSET = 360Ω, 75Ω doubly terminated load

Figure 12: NTSC C (Chrominance) Video Output Waveform

Color / Level	mA	V
Cyan / Red	27.06	1.015
Green / Magenta	26.22	0.983
Yellow / Blue	23.63	0.886
Peak Burst	19.21	0.720
Blank	15.24	0.572
Peak Burst	11.28	0.423
Yellow / Blue	6.85	0.257
Green / Magenta	4.27	0.160
Cyan / Red	3.43	0.129



Note: 1 100% amplitude, 100% saturation color bars are shown

Note: 2 Vref = 1.235V, RSET = 360Ω, 75Ω doubly terminated load

Figure 13: PAL C (Chrominance) Video Output Waveform

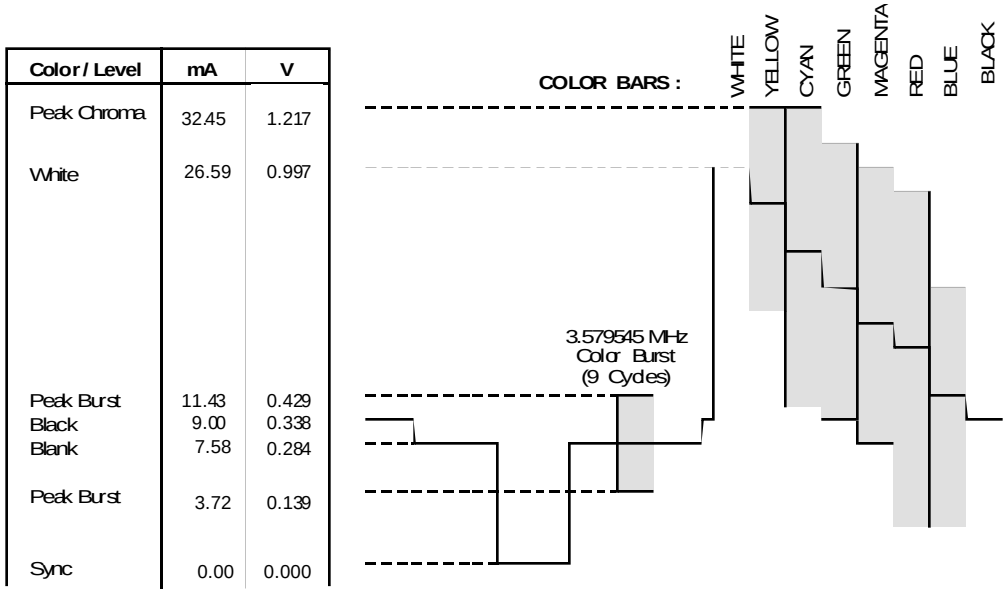


Figure 14: Composite NTSC Video Output Waveform

Note: Vref = 1.235V, RSET = 360Ω, 75Ω doubly terminated load

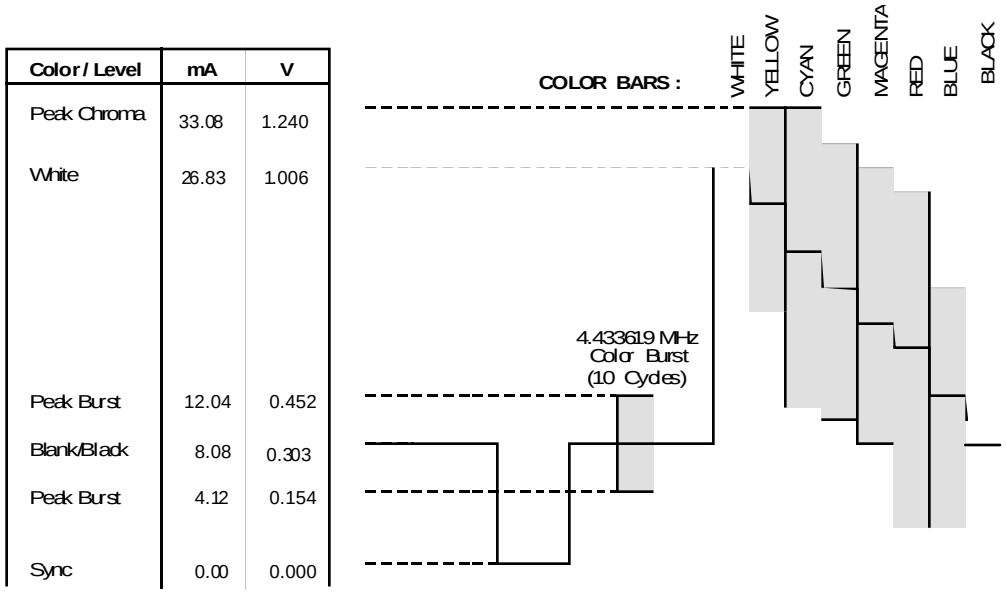


Figure 15: Composite PAL Video Output Waveform

Note: Vref = 1.235V, RSET = 360Ω, 75Ω doubly terminated load

Electrical Specifications

Table 4 • Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	VDD relative to GND	- 0.5		7.0	V
	Input voltage of all digital pins[1]	GND - 0.5		V_{DD} + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	- 55		125	°C
T_{STOR}	Storage temperature	- 65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (one minute)			220	°C
P_{MAX}	Maximum power dissipation			TBD	W

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

The device is fabricated using high-performance CMOS technology. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V can induce destructive latchup.

Table 5 • Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Analog supply voltage		5.00		
DVDD	Digital supply voltage		5.00		
T_A	Ambient operating temperature	0	25	70	°C
R_L	Output load to DAC outputs		37.5		Ω

Table 6 • Electrical Characteristics (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ± 5%)

Symbol	Description	Min	Typ	Max	Unit
	Video D/A resolution	9	9	9	Bits
	Full scale output current		33.08		mA
	Video level error using internal reference			10	%
	Total Current Consumption		135		mA

Note: As applied to Tables 4, 5, and 6, Recommended Operating Conditions are used as test conditions unless otherwise specified. RSET = 360 Ω, and NTSC CCIR601 operation. Typical values are based on 25°C and +5V.

Table 7 • Digital Inputs / Outputs

Symbol	Description	Test Condition @ T_A = 25°C	Min	Typ	Max	Units
V_{OH}	Output high voltage	I_{OH} = - 400 µA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.2 mA			0.4	V
V_{IH}	Input high voltage		2.0		V_{DD} + 0.5	V
V_{IL}	Input low voltage		GND - 0.5		0.8	V
I_{PU}	Input internal pull-up current		5		25	µA
I_{LK}	Input leakage current		-10		10	µA
CD_{IN}	Input capacitance	f = 1 MHz, V_{IN} = 2.4V		7		pF
CD_{OUT}	Output capacitance			10		pF

Electrical Specifications (continued)

Table 8 • AC Characteristics

Symbol	Description	Min	Typ	Max	Units
t_1	2XPCLK		37		ns
t_2	2XPCLK high time	14.8		22.2	ns
t_3	Pixel/Sync setup time	6			ns
t_4	Pixel/Sync hold time	3			ns
t_5	Sync active delay time	3			ns
t_6	Sync inactive delay time			17	ns
t_7	HSYNC* to VSYNC* delay	30		30	ns
t_{10}	HSYNC* pulse width	64 x t_1			ns
	VSYNC* delay time	17		20	ns
	VSYNC* pulse width	2.0			Hor. lines

Test Conditions: Unless otherwise specified, the testing conditions are the same as in Table 5, "Recommended Operating Conditions," on page 13. TTL input values are 0 – 3V, with input rise / fall times < 3 ns, measured between the V_{IL} and V_{IH}. Timing reference points at 50% for non-TTL inputs and outputs. TTL reference points at 1.5V for inputs and outputs. Analog output load < 10 pF.

Since the CH7203 does not have a pixel clock input, all input signal timing is chosen with respect to the output clock timing of 2XPCLK and PCLK. PCLK can be used at the "Qualifying" clock for certain MPEG decoders.

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH7203-V	PLCC	44	5V

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