xDSL Line Driver
3 V to 12 V with Power-Down

AD8391

FEATURES

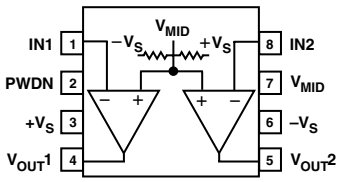
Ideal xDSL Line Driver for VoDSL or Low Power Applications such as USB, PCMCIA, or PCI-Based Customer Premise Equipment (CPE)
High Output Voltage and Current Drive
340 mA Output Drive Current
Low Power Operation
3 V to 12 V Power Supply Range
1-Pin Logic Controlled Standby, Shutdown
Low Supply Current of 19 mA (Typical)
Low Distortion
–82 dBc SFDR, 12 V p-p into Differential 21 Ω @ 100 kHz
4.5 nV/√Hz Input Voltage Noise Density, 100 kHz
Out-of-Band SFDR = –72 dBc, 144 kHz to 500 kHz, Z_{LINE} = 100 Ω, P_{LINE} = 13.5 dBm
High Speed
40 MHz Bandwidth (–3 dB)
375 V/μs Slew Rate

APPLICATIONS

VoDSL Modems
xDSL USB, PCI, PCMCIA Cards
Line Powered or Battery Backup xDSL Modems

PIN CONFIGURATION

8-Lead SOIC
(Thermal Coastline)



AD8391

PRODUCT DESCRIPTION

The AD8391 consists of two parallel, low cost xDSL line drive amplifiers capable of driving low distortion signals while running on both 3 V to 12 V single-supply or equivalent dual-supply rails. It is primarily intended for use in single-supply xDSL systems where low power is essential, such as line powered and battery backup systems. Each amplifier output drives more than 250 mA of current while maintaining –82 dBc of SFDR at 100 kHz on 12 V, outstanding performance for any xDSL CPE application.

The AD8391 provides a flexible power-down feature consisting of a 1-pin digital control line. This allows biasing of the AD8391 to full power (Logic "1"), Standby (Logic "tri-state" maintains low amplifier output impedance), and Shutdown (Logic "0" places amplifier outputs in a high impedance state). PWDN is referenced to $–V_S$.

Fabricated on ADI's high-speed XFCB process, the high bandwidth and fast slew rate of the AD8391 keep distortion to a minimum, while dissipating a minimum of power. The quiescent current of the AD8391 is low; 19 mA total static current draw. The AD8391 comes in a compact 8-lead SOIC "Thermal Coastline" package, and operates over the temperature range –40°C to +85°C.

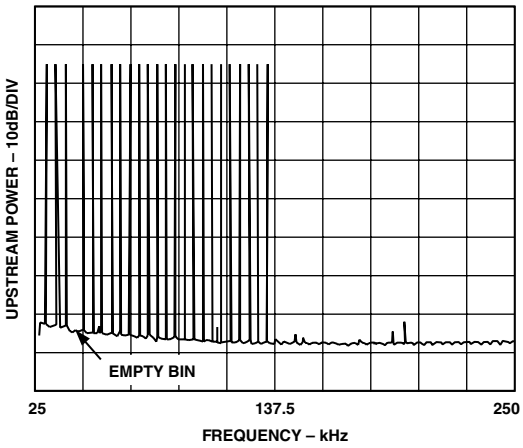


Figure 1. Upstream Transit Spectrum with Empty Bin at 45 kHz; Line Power = 12.5 dBm into 100 Ω

REV. 0

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AD8391–SPECIFICATIONS

(@ 25°C, V_S = 12 V, R_L = 10 Ω, V_{MID} = V_S/2, G = –2, R_F = 909 Ω, R_G = 453 Ω, unless otherwise noted. See TPC 1 for Basic Circuit Configuration.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = –1, V_{OUT} < 0.4 V p-p, R_G = 909 Ω		40		MHz
	G = –2, V_{OUT} < 0.4 V p-p		38		MHz
0.1 dB Bandwidth	V_{OUT} < 0.4 V p-p		4		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		50		MHz
Slew Rate	V_{OUT} = 4 V p-p		375		V/µs
Rise and Fall Time	V_{OUT} = 4 V p-p		8		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		60		ns
NOISE/HARMONIC PERFORMANCE					
Distortion, G = –5 (R_G = 178 Ω)	V_{OUT} = 8 V p-p (Differential)				
2nd Harmonic	100 kHz, R_L = 21 Ω		–82		dBc
3rd Harmonic	100 kHz, R_L = 21 Ω		–95		dBc
MTPR (In-Band)	25 kHz to 138 kHz, R_L = 21 Ω		–70		dBc
SFDR (Out-of-Band)	144 kHz to 500 kHz, R_L = 21 Ω		–72		dBc
Input Noise Voltage	f = 100 kHz Differential		4.5		nV/√Hz
Input Noise Current	f = 100 kHz		9		pA/√Hz
Crosstalk	f = 1 MHz, G = –2, Output to Output		64		dB
DC PERFORMANCE					
Input Offset Voltage	V_{MID} = +V_S/2		±2	±15	mV
	T_{MIN} to T_{MAX}		±3		mV
	V_{MID} = "Float"		±2		mV
Input Offset Voltage Match			±0.25	±2.6	mV
	T_{MIN} to T_{MAX}		±0.35		mV
Transimpedance	ΔV_{OUT} = 5 V		10		MΩ
INPUT CHARACTERISTICS					
Input Resistance			125		Ω
Input Bias Current	In1, In2 pins		2.5	10	µA
Input Bias Current Match	In1 – In2		±0.5	±6	µA
CMRR	V_{MID} = V_{IN} = 5.5 V to 6.5 V, $\Delta V_{OS}/\Delta V_{IN}$, cm		48		dB
Input CM Voltage Range			1.2 to 10.8		V
V_{MID} Accuracy	V_{MID} = "Float" Delta from +V_S/2		±5	±30	mV
V_{MID} Input Resistance			2.5		kΩ
V_{MID} Input Capacitance			10		pF
OUTPUT CHARACTERISTICS					
Output Resistance	Frequency = 100 kHz, PWDN "1"		0.3		Ω
Output Resistance	Frequency = 100 kHz, PWDN "0"		3		kΩ
Output Voltage Swing	R_{LOAD} = 100 Ω	0.1		11.9	V
Linear Output Current	SFDR < –75 dBc, f = 100 kHz, R_L = 21 Ω		340		mA
Short Circuit Current			1500		mA
POWER SUPPLY					
Supply Current	PWDN = "1"	16	19	21	mA
	T_{MIN} to T_{MAX}		22		mA
STBY Supply Current	PWDN = "Open or Three-State"		10		mA
SHUTDOWN Supply Current	PWDN = "0"		4	6	mA
Operating Range	Single Supply	3.0		12	V
Power Supply Rejection Ratio	V_{MID} = V_S/2, ΔV_S = ±0.5 V		55		dB
LOGIC INPUT (PWDN)					
Logic "1" Voltage		–V_S + 2.0			V
Logic "0" Voltage				–V_S + 0.8	V
Logic Input Bias Current			±300		µA
Turn On Time	R_L = 21 Ω, I_S = 90% of Typical		200		ns

Specifications subject to change without notice.

SPECIFICATIONS (@ 25°C, V_S = 3 V, R_L = 10 Ω, V_{MID} = V_S/2, G = –2, R_F = 909 Ω, R_G = 453 Ω, unless otherwise noted. See TPC 1 for Basic Circuit Configuration.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = –1, V_{OUT} < 0.4 V p-p		37		MHz
	G = –2, V_{OUT} < 0.4 V p-p		36		MHz
0.1dB Bandwidth	V_{OUT} < 0.4 V p-p		3.5		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p		30		MHz
Slew Rate	V_{OUT} = 2 V p-p		50		V/µs
Rise and Fall Time	Differential, V_{OUT} = 1 V p-p		15		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		110		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	V_{OUT} = 4 V p-p (Differential)				
2nd Harmonic	100 kHz, R_L = 21 Ω		–81		dBc
3rd Harmonic	100 kHz, R_L = 21 Ω		–97		dBc
Input Noise Voltage	f = 100 kHz Differential		4.5		nV/√Hz
Input Noise Current	f = 100 kHz		9		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	V_{MID} = +V_S/2		±3	±15	mV
	T_{MIN} to T_{MAX}		±4		mV
	V_{MID} = "Float"		±3		mV
Input Offset Voltage Match			±0.1	±2.6	mV
	T_{MIN} to T_{MAX}		±0.2		mV
Transimpedance	ΔV_{OUT} = 1 V		8		MΩ
INPUT CHARACTERISTICS					
Input Resistance			125		Ω
Input Bias Current	In1, In2 pins		1	7	µA
Input Bias Current Match	In1 – In2		±0.5	±4	µA
CMRR	V_{MID} = V_{IN} = 1.3 V to 1.5 V, ΔV_{OS} /ΔV_{IN}, cm		48		dB
Input CM Voltage Range			1.2 to 2.1		V
V_{MID} Accuracy	V_{MID} = "Float," Delta from +V_S/2		±5	±30	mV
V_{MID} Input Resistance			2.5		kΩ
V_{MID} Input Capacitance			10		pF
OUTPUT CHARACTERISTICS					
Output Resistance	Frequency = 100 kHz, PWDN "1"		0.2		Ω
Output Resistance	Frequency = 100 kHz, PWDN "0"		9		kΩ
Output Voltage Swing	R_L = 100 Ω	0.1		2.9	V
Linear Output Current	SFDR < –82 dBc, f = 100 kHz, R_L = 21 Ω		125		mA
Short Circuit Current			1000		mA
POWER SUPPLY					
Supply Current	PWDN = "1"	13	16	18	mA
	T_{MIN} to T_{MAX}		19		mA
STBY Supply Current	PWDN = "Open or Three-State"		8		mA
SHUTDOWN Supply Current	PWDN = "0"		1	2	mA
Operating Range	Single Supply	3.0		12	V
Power Supply Rejection Ratio	V_{MID} = V_S/2, ΔV_S = ±0.5 V		55		dB
LOGIC INPUTS (PWDN [1,0])					
Logic "1" Voltage		–V_S + 2.0			V
Logic "0" Voltage				–V_S + 0.8	V
Logic Input Bias Current			±60		µA
Turn On Time	R_L = 21 Ω, I_S = 90% of Typical		200		ns

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Small Outline Package (R) . . . . . 650 mW
Input Voltage (Common-Mode) . . . . . $\pm V_S$
Logic Voltage, PWDN . . . . . $\pm V_S$
Output Short Circuit Duration
. . . . . Observe Power Derating Curve
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Specification is for device on a four-layer board in free air at 85°C: 8-Lead SOIC package: θ_{JA} = 100°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8391AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD8391AR–REEL	–40°C to +85°C	8-Lead SOIC	SO-8
AD8391AR–REEL7	–40°C to +85°C	8-Lead SOIC	SO-8
AD8391AR–EVAL		Evaluation Board	SO-8

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8391 is limited by the associated rise in junction temperature. The maximum safe junction temperature for a plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

To ensure proper operation, it is necessary to observe the maximum power derating curve.

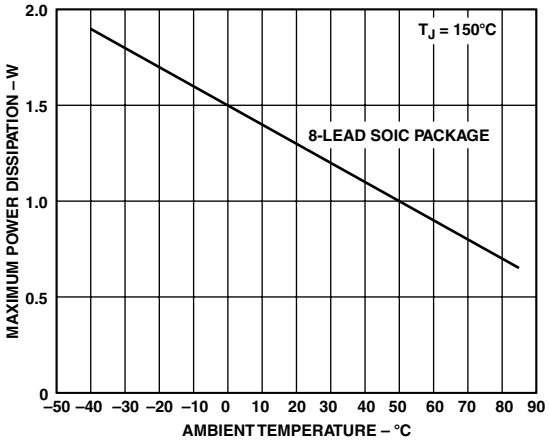
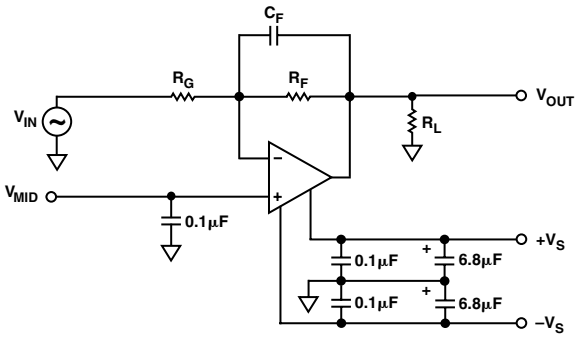


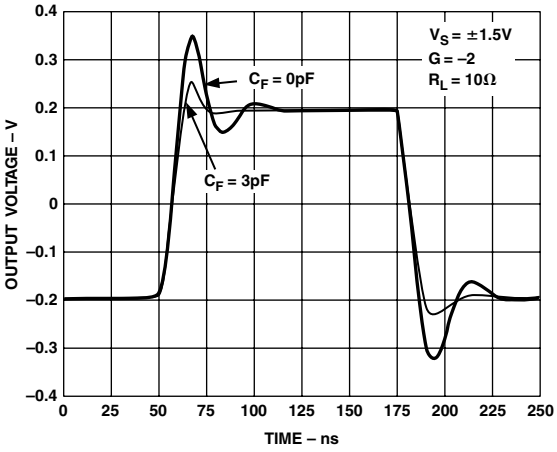
Figure 2. Plot of Maximum Power Dissipation vs. Temperature

CAUTION

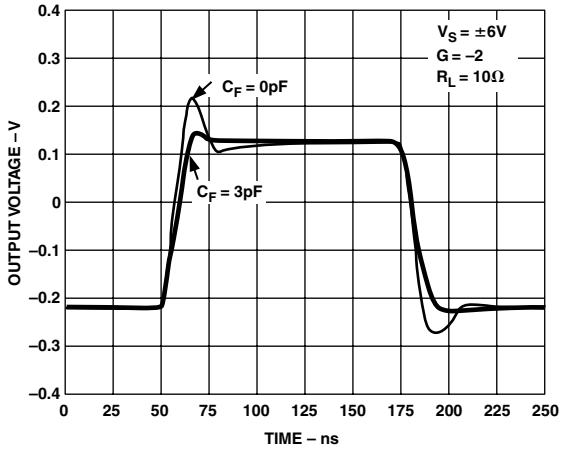
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8391 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



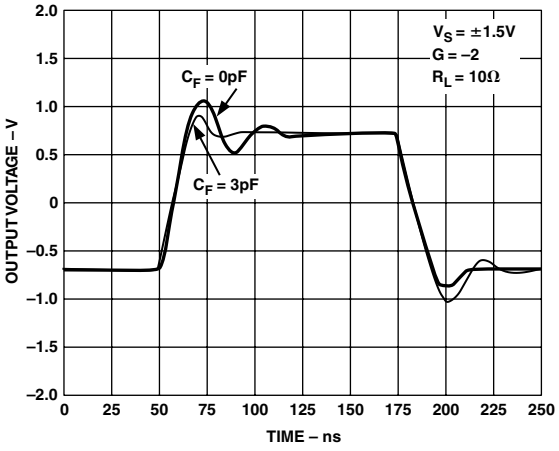
TPC 1. Single-Ended Test Circuit



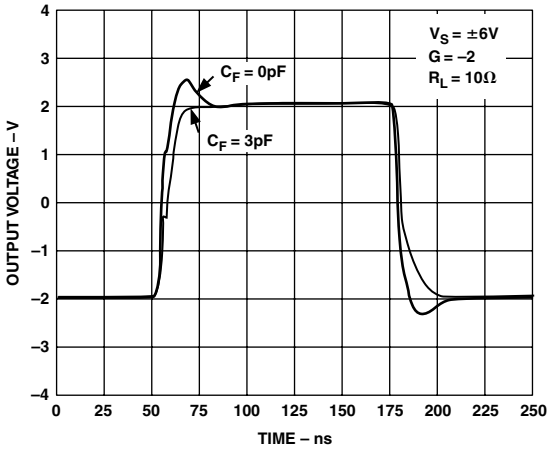
TPC 4. Small Signal Step Response



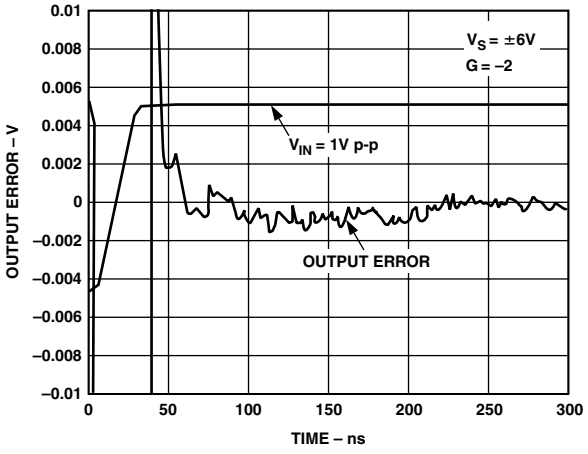
TPC 2. Small Signal Step Response



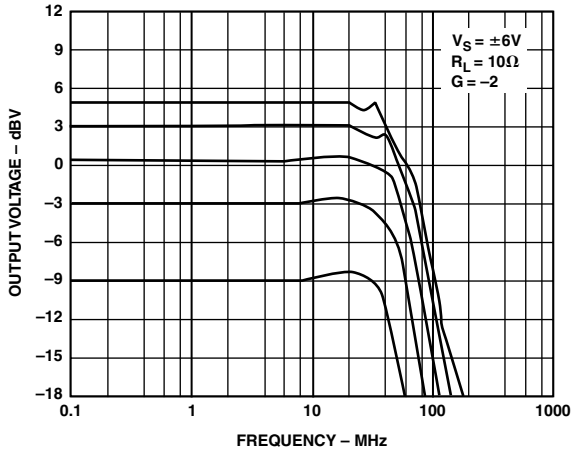
TPC 5. Large Signal Step Response



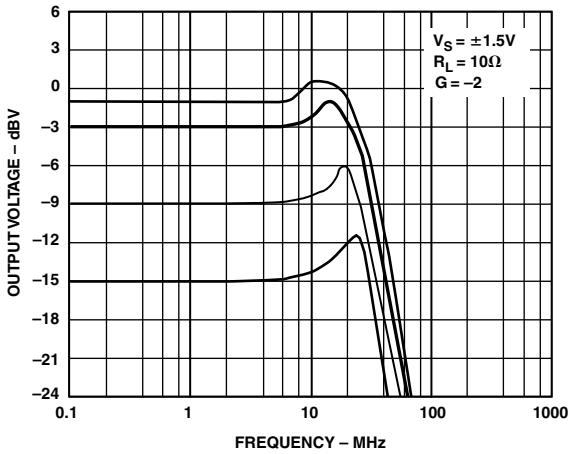
TPC 3. Large Signal Step Response



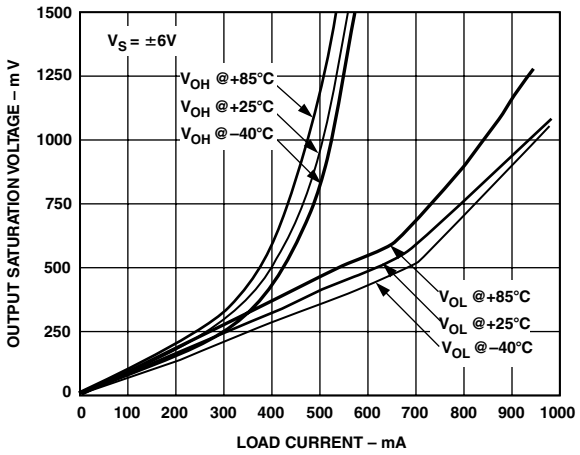
TPC 6. 0.1% Settling Time



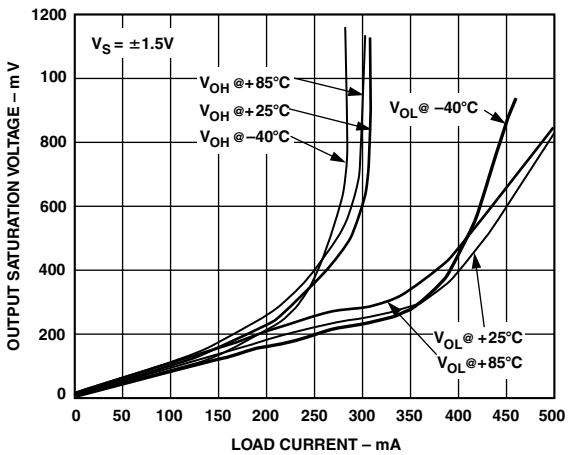
TPC 7. Output Voltage vs. Frequency



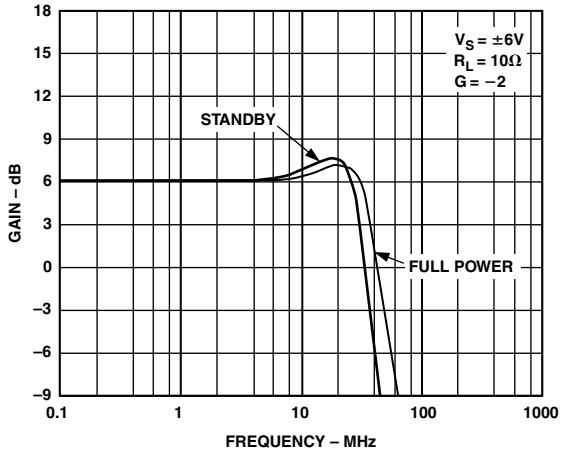
TPC 10. Output Voltage vs. Frequency



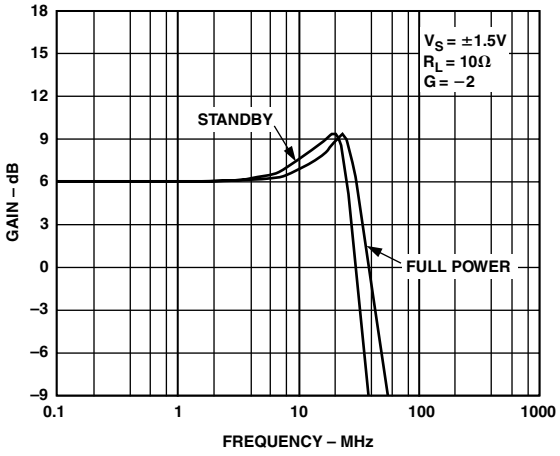
TPC 8. Output Saturation Voltage vs. Load



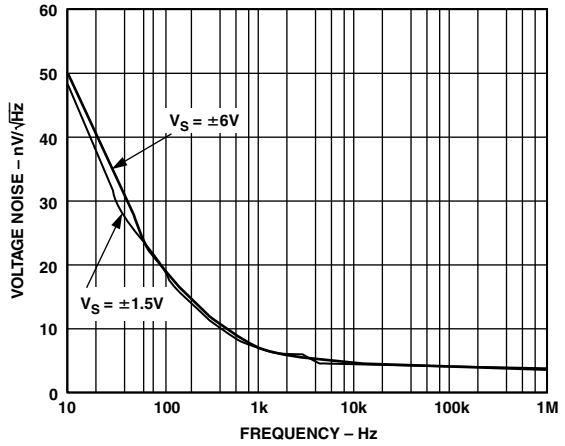
TPC 11. Output Saturation Voltage vs. Load



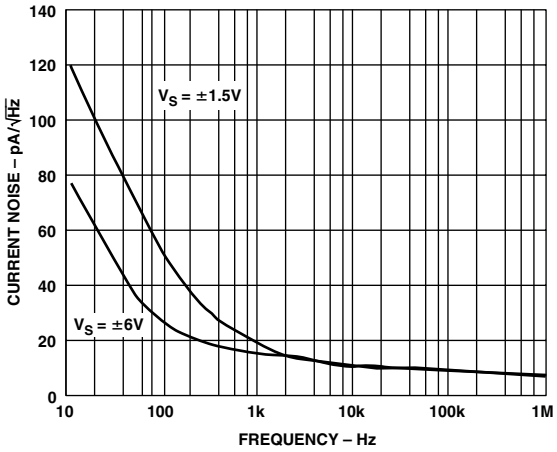
TPC 9. Small Signal Frequency Response



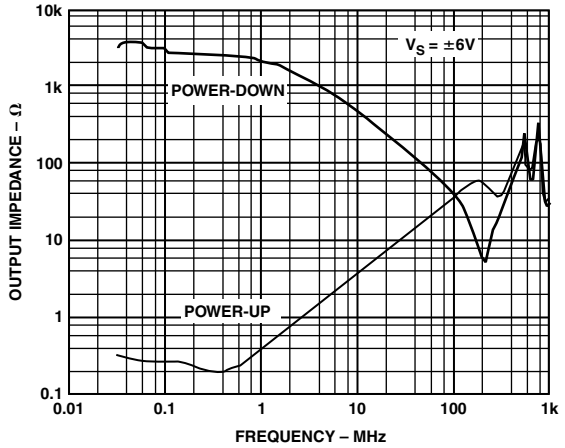
TPC 12. Small Signal Frequency Response



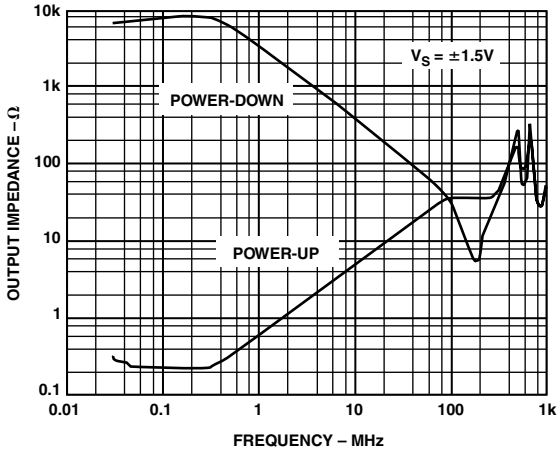
TPC 13. Voltage Noise vs. Frequency (RTI)



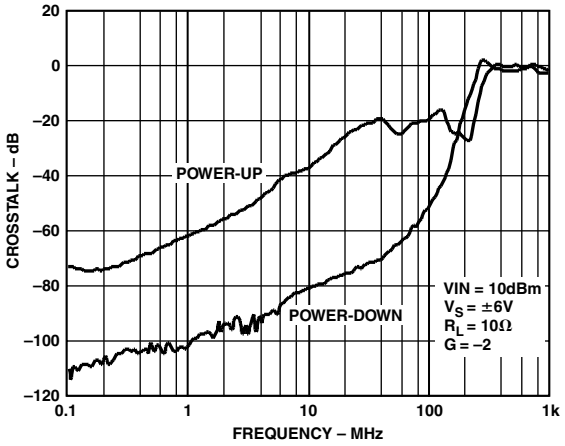
TPC 16. Current Noise vs. Frequency (RTI)



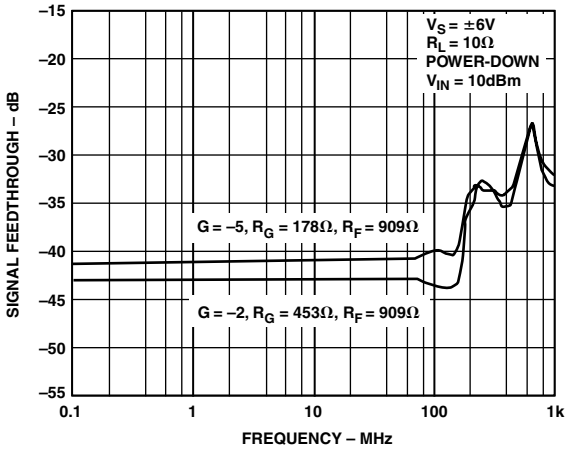
TPC 14. Output Impedance vs. Frequency



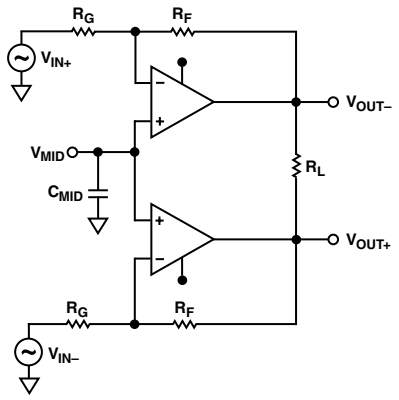
TPC 17. Output Impedance vs. Frequency



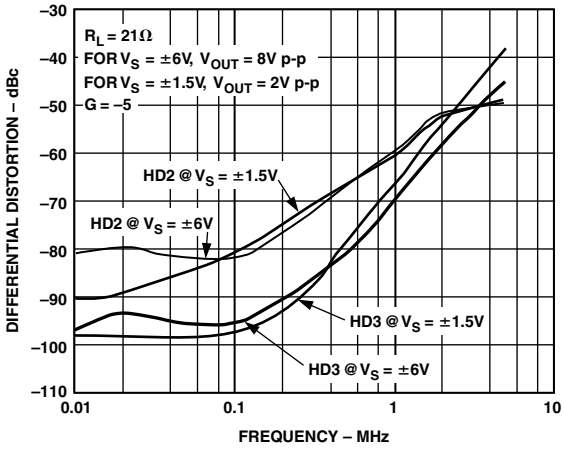
TPC 15. Crosstalk (Output to Output) vs. Frequency



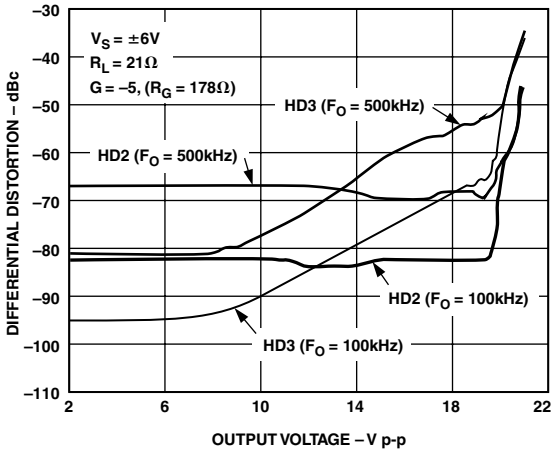
TPC 18. Signal Feedthrough vs. Frequency



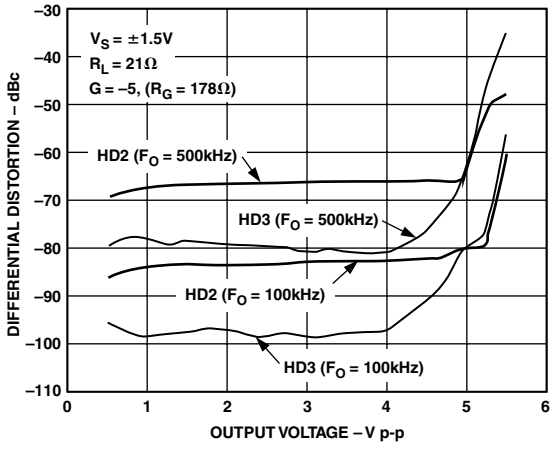
TPC 19. Differential Output Test Setup



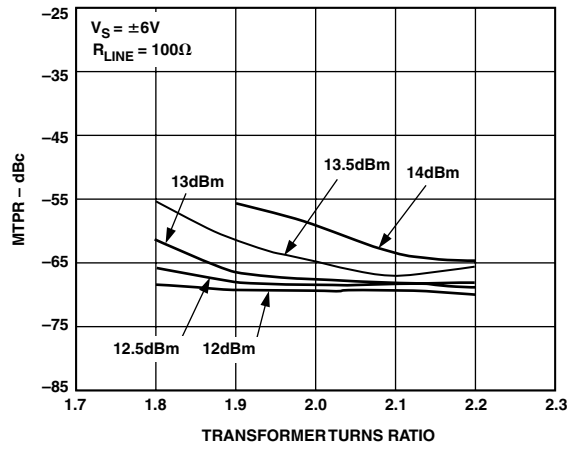
TPC 22. Differential Distortion vs. Frequency



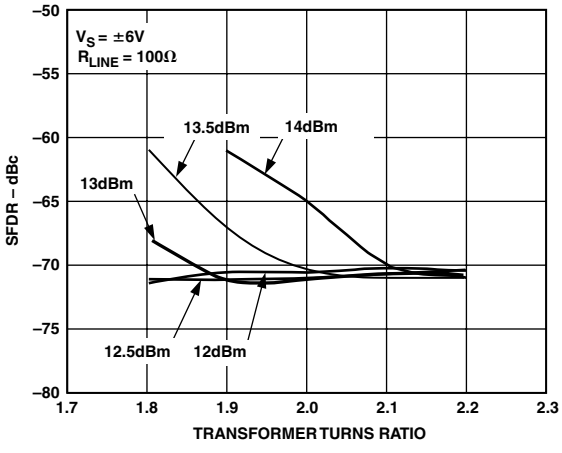
TPC 20. Differential Distortion vs. Output Voltage



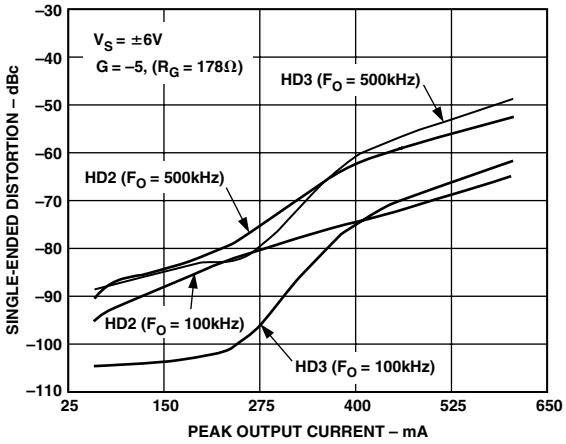
TPC 23. Differential Distortion vs. Output Voltage



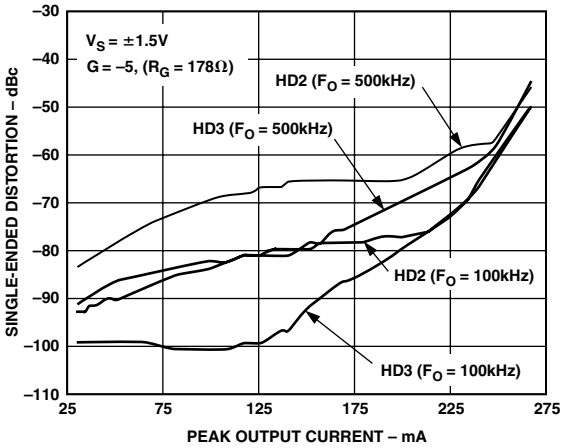
TPC 21. MTPR vs. Transformer Turns Ratio



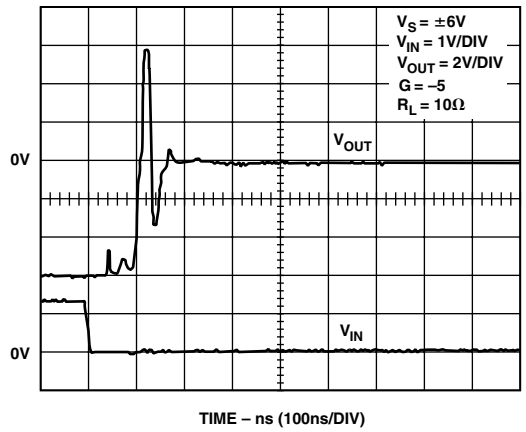
TPC 24. SFDR vs. Transformer Turns Ratio



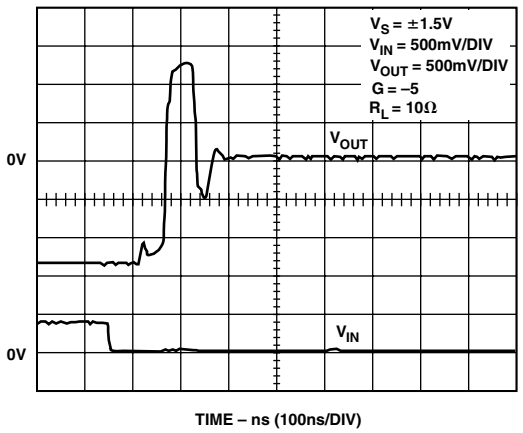
TPC 25. Single-Ended Distortion vs. Peak Output Current



TPC 27. Single-Ended Distortion vs. Peak Output Current



TPC 26. Overload Recovery



TPC 28. Overload Recovery

GENERAL INFORMATION

Theory of Operation

The AD8391 is a dual current feedback amplifier with high output current capability. It is fabricated on Analog Devices' proprietary eXtra Fast Complementary Bipolar Process (XFCB) that enables the construction of PNP and NPN transistors with f_T's greater than 3 GHz. The process uses dielectrically isolated transistors to eliminate the parasitic and latch-up problems caused by junction isolation. These features enable the construction of high-frequency, low-distortion amplifiers.

The AD8391 has a unique pin out. The two noninverting inputs of the amplifier are connected to the V_{MID} pin, which is internally biased by two 5 kΩ resistors forming a voltage divider between $+V_S$ and $-V_S$. V_{MID} is accessible through Pin 7. There is also a 10 pF internal capacitor from V_{MID} to $-V_S$. The two inverting pins are available at Pin 1 and Pin 8, allowing the gain of the amplifiers to be set with external resistors. See the front page for a connection diagram of the AD8391.

A simplified schematic of an amplifier is shown in Figure 3. Emitter followers buffer the positive input, V_P, to provide low-input current and current noise. The low-impedance current feedback summing junction is at the negative input, V_N. The output stage is another high-gain amplifier used as an integrator to provide frequency compensation. The complementary common-emitter output provides the extended output swing.

A current feedback amplifier's bandwidth and distortion performance are relatively insensitive to its closed-loop signal gain, which is a distinct advantage over a voltage-feedback architecture. Figure 4 shows a simplified model of a current feedback amplifier. The feedback signal is an error current that flows into the inverting node. R_{IN} is inversely proportional to the transconductance of the amplifier's input stage, g_{mi}. Circuit analysis of the pictured follower with gain circuit yields:

$$\frac{V_{OUT}}{V_{IN}} = \frac{G \times Tz(s)}{Tz(s) + R_F + G \times R_{IN}}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$$Tz(s) = \frac{R_F}{1 + sC_T(R_T)}$$

$$R_{IN} = \frac{1}{g_{mi}} \cong 125\ \Omega$$

Recognizing that $G \times R_{IN} << R_F$, and that the –3 dB point is set when $Tz(s) = R_F$, one can see that the amplifier's bandwidth depends primarily on the feedback resistor. There is a value of R_F below which the amplifier will be unstable, as the amplifier will have additional poles that will contribute excess phase shift. The optimum value for R_F depends on the gain and the amount of peaking tolerable in the application. For more information about current feedback amplifiers, see ADI's High-Speed Design Techniques at www.analog.com/technology/amplifiersLinear/designTools/evaluationBoards/pdf/1.pdf.

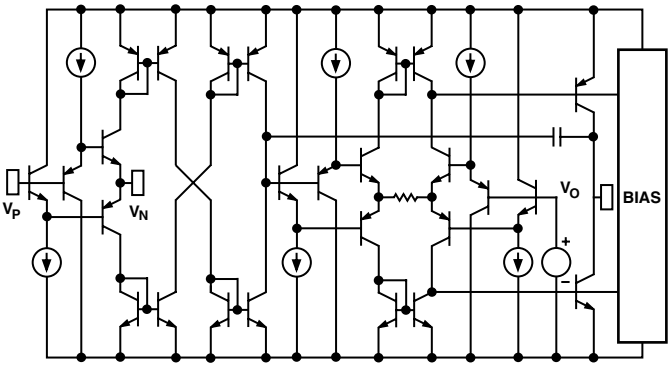


Figure 3. Simplified Schematic

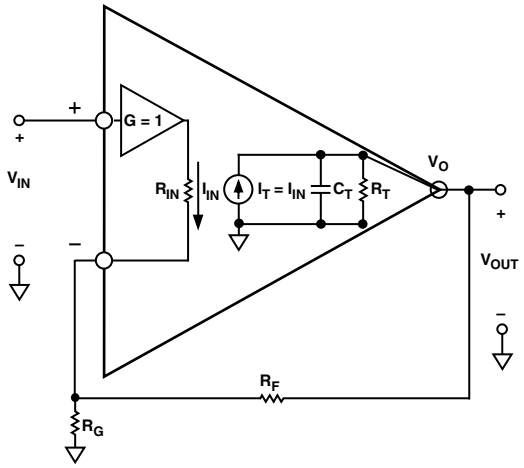


Figure 4. Model of Current Feedback Amplifier

Feedback Resistor Selection

In current feedback amplifiers, selection of the feedback and gain resistors will impact distortion, bandwidth, noise, and gain flatness. Care should be exercised in the selection of these resistors so that the optimum performance is achieved. Table I shows the recommended resistor values for use in a variety of gain settings for the test circuits in TPC 1 and TPC 19. These values are only intended to be a starting point when designing for any application.

Table I. Resistor Selection Guide

Gain	R_F (Ω)	R_G (Ω)
–1	909	909
–2	909	453
–3	909	303
–4	909	227
–5	909	178

Power-Down Feature

A three-state power-down function is available via the PWDN pin. It allows the user to select among three operating conditions: full on, standby, or shutdown. The $-V_S$ pin is the logic reference for the PWDN function. The full shutdown state is maintained when the PWDN is at 0.8 V or less above $-V_S$. In shutdown the AD8391 will draw only 4 mA. If the PWDN pin floats, the AD8391 operates in a standby mode with low impedance outputs and draws approximately 10 mA.

Power Supply and Decoupling

The AD8391 can be powered with a good quality (i.e., low-noise) supply anywhere in the range from 3 V to 12 V. The AD8391 can also operate on dual supplies, from ±1.5 V to ±6 V. In order to optimize the ADSL upstream drive capability of +13 dBm and maintain the best Spurious Free Dynamic Range (SFDR), the AD8391 circuit should be powered with a well-regulated supply.

Careful attention must be paid to decoupling the power supply. High-quality capacitors with low equivalent series resistance (ESR) such as multilayer ceramic capacitors (MLCCs) should be used to minimize supply voltage ripple and power dissipation. In addition, 0.1 µF MLCC decoupling capacitors should be located no more than 1/8 inch away from each of the power supply pins. A large, usually tantalum, 10 µF capacitor is required to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the AD8391 outputs.

Bypassing capacitors should be laid out in such a manner to keep return currents away from the inputs of the amplifiers. This will minimize any voltage drops that can develop due to ground currents flowing through the ground plane. A large ground plane will also provide a low impedance path for the return currents.

The V_{MID} pin should also be decoupled to ground by using a 0.1 µF ceramic capacitor. This will help prevent any high frequency components from finding their way to the noninverting inputs of the amplifiers.

Design Considerations

There are some unique considerations that must be taken into account when designing with the AD8391. The V_{MID} pin is internally biased by two 5 kΩ resistors forming a voltage divider between V_{CC} and ground. These resistors will contribute approximately 6.3 nV/$\sqrt{\text{Hz}}$ of input-referred (RTI) noise. This noise source is common mode and will not contribute to the output noise when the AD8391 is used differentially. In a single-supply system, this is unavoidable. In a dual-supply system, V_{MID} can be connected directly to ground, eliminating this source of noise.

When V_{MID} is left floating, a change in the power supply voltage (ΔV) will result in a change of one-half ΔV at the V_{MID} pin. If the amplifiers' inverting inputs are ac-coupled, one-half ΔV will appear at the output, resulting in a PSRR of –6 dB. If the inputs are dc-coupled, $\Delta V \times (1 + R_f/R_g)$ will appear at the outputs.

Power Dissipation

It is important to consider the total power dissipation of the AD8391 to size the heat sink area of an application properly. Figure 5 is a simple representation of a differential driver. With some simplifying assumptions the total power dissipated in this circuit can be estimated. If the output current is large compared to the quiescent current, computing the dissipation in the output devices and adding it to the quiescent power dissipation will give a close approximation of the total power dissipation in the package. A factor α corrects for the slight error due to the Class A/B operation of the output stage. The value of α depends on what portion of the quiescent current is in the output stage and varies from 0 to 1. For the AD8391, $\alpha \cong 0.72$.

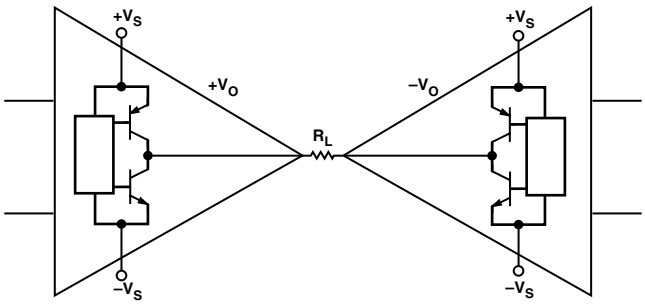


Figure 5. Simplified Differential Driver

Remembering that each output device only dissipates power for half the time gives a simple integral that computes the power for each device:

$$\frac{1}{2}\int\left[(V_S - V_O)\times\frac{2V_O}{R_L}\right]$$

The total supply power can then be computed as:

$$P_{TOT} = 4\left(V_S \int|V_O| - \int {V_O}^2\right)\times\frac{1}{R_L} + 2\,\alpha\, I_Q V_S$$

In this differential driver, V_O is the voltage at the output of one amplifier, so 2 V_O is the voltage across R_L. R_L is the total impedance seen by the differential driver, including any back termination. Now, with two observations the integrals are easily evaluated. First, the integral of ${V_O}^2$ is simply the square of the rms value of V_O. Second, the integral of $|V_O|$ is equal to the average rectified value of V_O, sometimes called the mean average deviation, or MAD. It can be shown that for a DMT signal, the MAD value is equal to 0.8 times the rms value:

$$P_{TOT} = 4\,(0.8\,V_O\ rms\,V_S - V_O\ rms^2)\times\frac{1}{R_L} + 2\,\alpha\, I_Q\, V_S$$

For the AD8391 operating on a single 12 V supply and delivering a total of 16 dBm (13 dBm to the line and 3 dBm to account for the matching network) into 50 Ω (100 Ω reflected back through a 1:2 transformer plus back termination), the dissipated power is 395 mW.

Using these calculations and a θ_{JA} of 100°C/W for the SOIC, Table II shows junction temperature versus power delivered to the line for several supply voltages while operating at an ambient temperature of 85°C. Operation at a junction temperature over the absolute maximum rating of 150°C should be avoided.

Table II. Junction Temperature vs. Line Power and Operating Voltage for SOIC at 858C Ambient

	V_{SUPPLY}	
P_{LINE}, dBm	12	12.5
13	125	126
14	127	129
15	129	131

Thermal stitching, which connects the outer layers to the internal ground planes(s), can help to use the thermal mass of the PCB to draw heat away from the line driver and other active components.

Layout Considerations

As is the case with all high-speed applications, careful attention to printed circuit board layout details will prevent associated board parasitics from becoming problematic. Proper RF design techniques are mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low-impedance return path. Removing the ground plane on all layers from the areas near the input and output pins will reduce stray capacitance, particularly in the area of the inverting inputs. The signal routing should be short and direct in order to minimize parasitic inductance and capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) through the board. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize balanced performance. When running differential signals over a long distance, the traces on the PCB should be close. This will reduce the radiated energy and make the circuit less susceptible to RF interference. Adherence to stripline design techniques for long signal traces (greater than about one inch) is recommended.

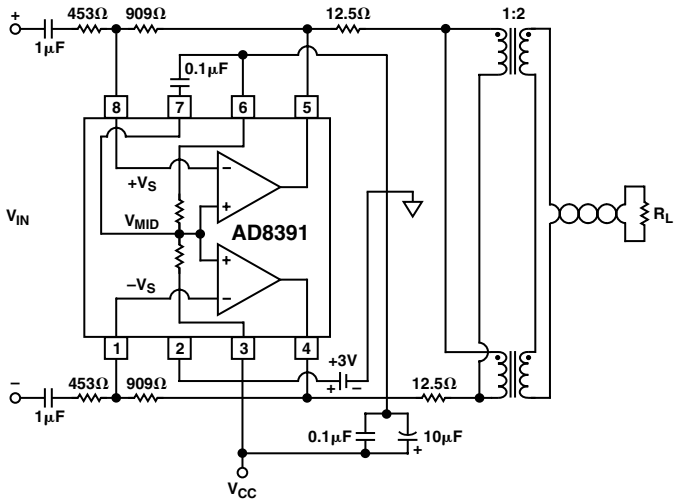


Figure 6. Single-Supply Voltage Differential Drive Circuit

Evaluation Board

The AD8391 is available installed on an evaluation board. Figure 10 shows the schematics for the evaluation board. AC-coupling capacitors of 0.1 μF, C6 and C11, in combination with 10 kΩ, resistors R25 and R26, will form a first order high-pass pole at 160 Hz.

The bill of materials included as Table III represents the components that are installed in the evaluation board when it is shipped to a customer. There are footprints for additional components, such as an AD8138, that will convert a single-ended signal into a differential signal. There is also a place for an AD9632, which can be used to convert a differential signal into a single-ended signal.

Transformer Selection

Customer premise ADSL requires the transmission of a 13 dBm (20 mW) DMT signal. The DMT signal has a crest factor of 5.3, requiring the line driver to provide peak line power of 560 mW. 560 mW peak line power translates into a 7.5 V peak voltage on a 100 Ω telephone line. Assuming that the maximum low distortion output swing available from the AD8391 line driver on a 12 V supply is 11 V, and taking into account the power lost due to the termination resistance, a step-up transformer with turns ratio of 1:2 is adequate for most applications. If the modem designer desires to transmit more than 13 dBm down the twisted pair, a higher turns ratio can be used for the transformer. This trade-off comes at the expense of higher power dissipation by the line driver as well as increased attenuation of the downstream signal that is received by the transceiver.

In the simplified differential drive circuit shown in Figure 6 the AD8391 is coupled to the phone line through a step-up transformer with a 1:2 turns ratio. R45 and R46 are back termination or line matching resistors, each 12.5 Ω [1/2 (100 Ω/2^2)] where 100 Ω is the approximate phone line impedance. A transformer reflects impedance from the line side to the IC side as a value inversely proportional to the square of the turns ratio. The total differential load for the AD8391, including the termination resistors, is 50 Ω. Even under these conditions the AD8391 provides low distortion signals to within 0.5 V of the power supply rails.

One must take care to minimize any capacitance present at the outputs of a line driver. The sources of such capacitance can include but are not limited to EMI suppression capacitors, overvoltage protection devices and the transformers used in the hybrid. Transformers have two kinds of parasitic capacitances: distributed or bulk capacitance, and interwinding capacitance. Distributed capacitance is a result of the capacitance created between each adjacent winding on a transformer. Interwinding capacitance is the capacitance that exists between the windings on the primary and secondary sides of the transformer. The existence of these capacitances is unavoidable and limiting both distributed and interwinding capacitance to less than 20 pF each should be sufficient for most applications.

It is also important that the transformer operates in its linear region throughout the entire dynamic range of the driver. Distortion introduced by the transformer can severely degrade DSL performance, especially when operating at long loop lengths.

Receive Channel Considerations

A transformer used at the output of the differential line driver to step up the differential output voltage to the line has the inverse effect on signals received from the line. A voltage reduction or attenuation equal to the inverse of the turns ratio is realized in the receive channel of a typical bridge hybrid. The turns ratio of the transformer may also be dictated by the ability of the receive circuitry to resolve low-level signals in the noisy twisted pair telephone plant. While higher turns ratio transformers boost transmit signals to the appropriate level, they also effectively reduce the received signal-to-noise ratio due to the reduction in the received signal strength. Using a transformer with as low a turns ratio as possible will limit degradation of the received signal.

The AD8022, a dual amplifier with typical RTI voltage noise of only 2.5 nV/$\sqrt{\text{Hz}}$ and a low supply current of 4 mA/amplifier is recommended for the receive channel. If power-down is required for the receive amplifier, two AD8021 low-noise amplifiers can be used instead.

DMT Modulation, Multitone Power Ratio (MTPR) and Out-of-Band SFDR

ADSL systems rely on Discrete Multitone (DMT) modulation to carry digital data over phone lines. DMT modulation appears in the frequency domain as power contained in several individual frequency subbands, sometimes referred to as tones or bins, each of which are uniformly separated in frequency. A uniquely encoded, Quadrature Amplitude Modulation (QAM) like signal occurs at the center frequency of each subband or tone. See Figure 7 for an example of a DMT waveform in the frequency domain, and Figure 8 for a time domain waveform. Difficulties will exist when decoding these subbands if a QAM signal from one subband is corrupted by the QAM signal(s) from other subbands regardless of whether the corruption comes from an adjacent subband or harmonics of other subbands.

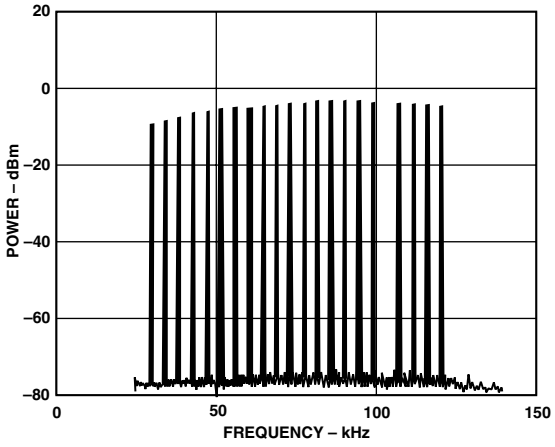


Figure 7. DMT Waveform in the Frequency Domain

Conventional methods of expressing the output signal integrity of line drivers such as single-tone harmonic distortion or THD, two-tone InterModulation Distortion (IMD) and third order intercept (IP3) become significantly less meaningful when amplifiers are required to process DMT and other heavily modulated waveforms. A typical ADSL upstream DMT signal can contain as many as 27 carriers (subbands or tones) of QAM signals. Multitone Power Ratio (MTPR) is the relative difference between the measured power in a typical subband (at one tone or carrier) versus the power at another subband specifically selected to contain no QAM data. In other words, a selected subband (or tone) remains open or void of intentional power (without a QAM signal) yielding an empty frequency bin. MTPR, sometimes referred to as the "empty bin test," is typically expressed in dBc, similar to expressing the relative difference between single-tone fundamentals and second or third harmonic distortion components. Measurements of MTPR are typically made on the line side or secondary side of the transformer.

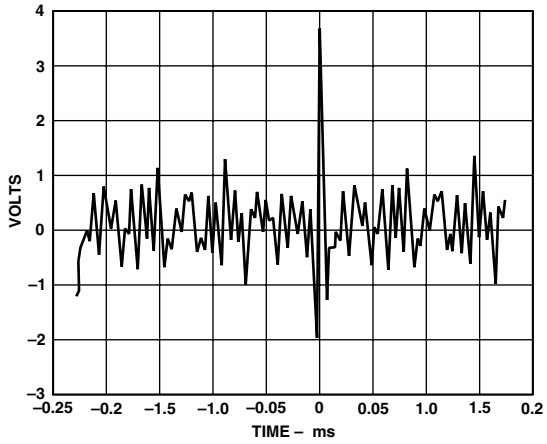


Figure 8. DMT Signal in the Time Domain

TPC 21 and TPC 24 depict MTPR and SFDR versus transformer turns respectively for a variety of line power ranging from 12 dBm to 14 dBm. As the turns ratio increases, the driver hybrid can deliver more undistorted power to the load due to the high output current capability of the AD8391. Significant degradation of MTPR will occur if the output transistors of the driver saturate, causing clipping at the DMT voltage peaks. Driving DMT signals to such extremes not only compromises "in-band" MTPR, but will also produce spurs that exist outside of the frequency spectrum containing the transmitted signal. "Out-of-band" spurious-free dynamic range (SFDR) can be defined as the relative difference in amplitude between these spurs and a tone in one of the upstream bins. Compromising out-of-band SFDR is the equivalent to increasing near-end crosstalk (NEXT). Regardless of terminology, maintaining high out-of-band SFDR while reducing NEXT will improve the overall performance of the modems connected at either end of the twisted pair.

Generating DMT Signals

At this time, DMT-modulated waveforms are not typically menu-selectable items contained within arbitrary waveform generators. Even using AWG software to generate DMT signals, AWGs that are available today may not deliver DMT signals sufficient in performance with regard to MTPR due to limitations in the D/A converters and output drivers used by AWG manufacturers. MTPR evaluation requires a DMT signal generator capable of delivering MTPR performance better than that of the driver under evaluation. Generating DMT signals can be accomplished using a Tektronics AWG 2021 equipped with option 4, (12-/24-bit, TTL Digital Data Out), digitally coupled to Analog Devices' AD9754, a 14-bit TxDAC, buffered by an AD8002 amplifier configured as a differential driver. Note that the DMT waveforms, available on the Analog Devices website (www.analog.com) are similar. WFM files are needed to produce the necessary digital data required to drive the TxDAC from the optional TTL Digital Data output of the TEK AWG2021.

Video Driver

The AD8391 can be used as a noninverting amplifier by applying a signal at the V_{MID} pin and grounding the gain resistors. See Figure 9 for an example circuit. The signal applied to the V_{MID} pin would be present at both outputs, making this circuit ideal for any application where one signal needs to be sent to two different locations, such as a video distribution system. As previously stated, the AD8391 can operate on split supplies in this case, eliminating the need for ac-coupling.

The termination resistor should be 76.8 Ω to maintain a 75 Ω input impedance.

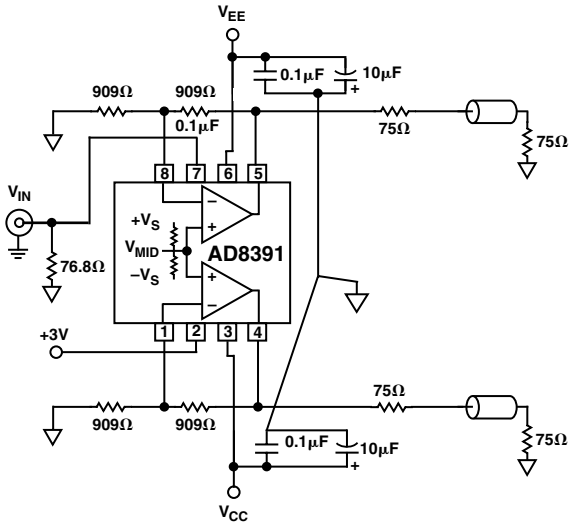


Figure 9. Driving Two Video Loads from the Same Source

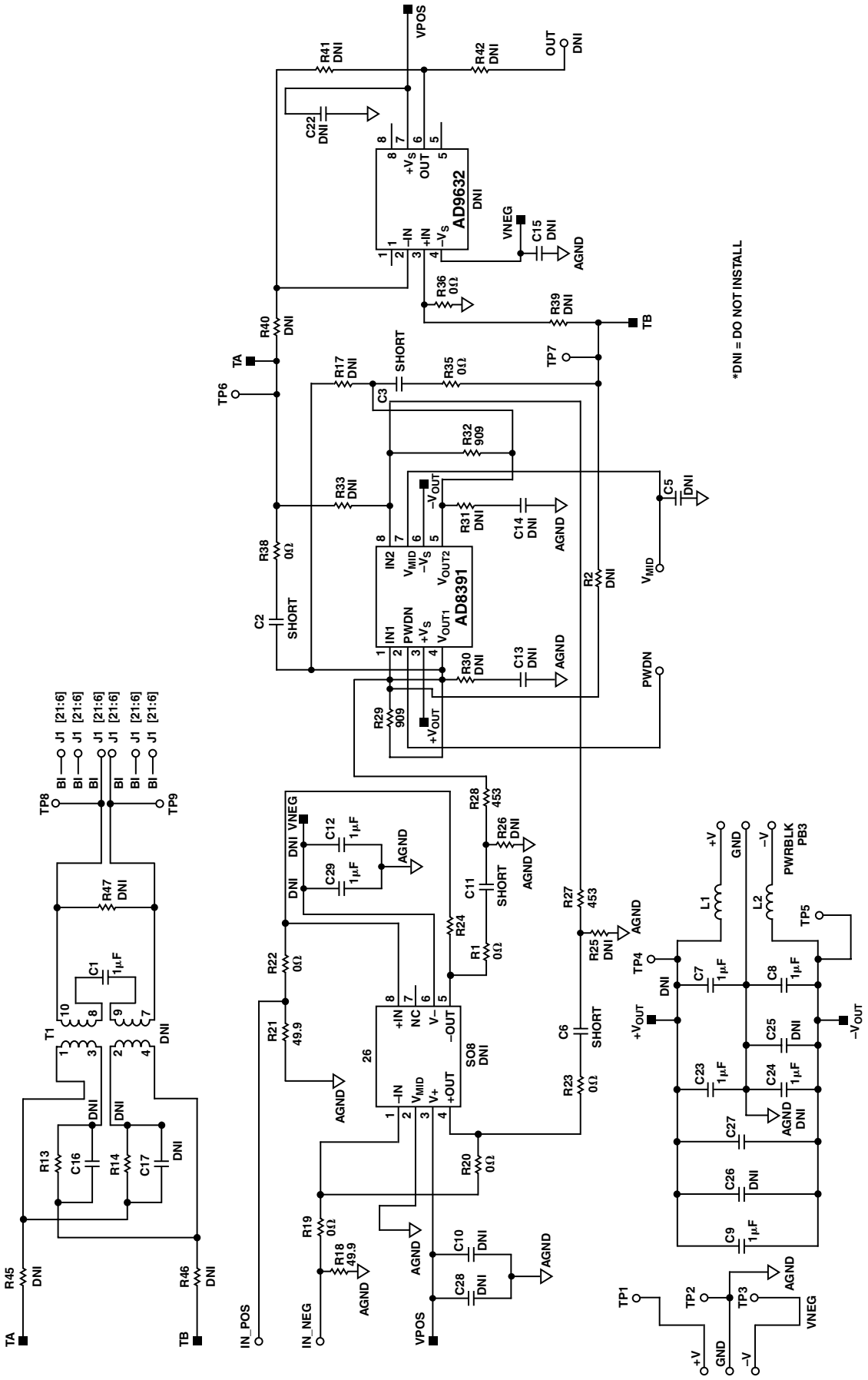


Figure 10. Evaluation Board Schematic

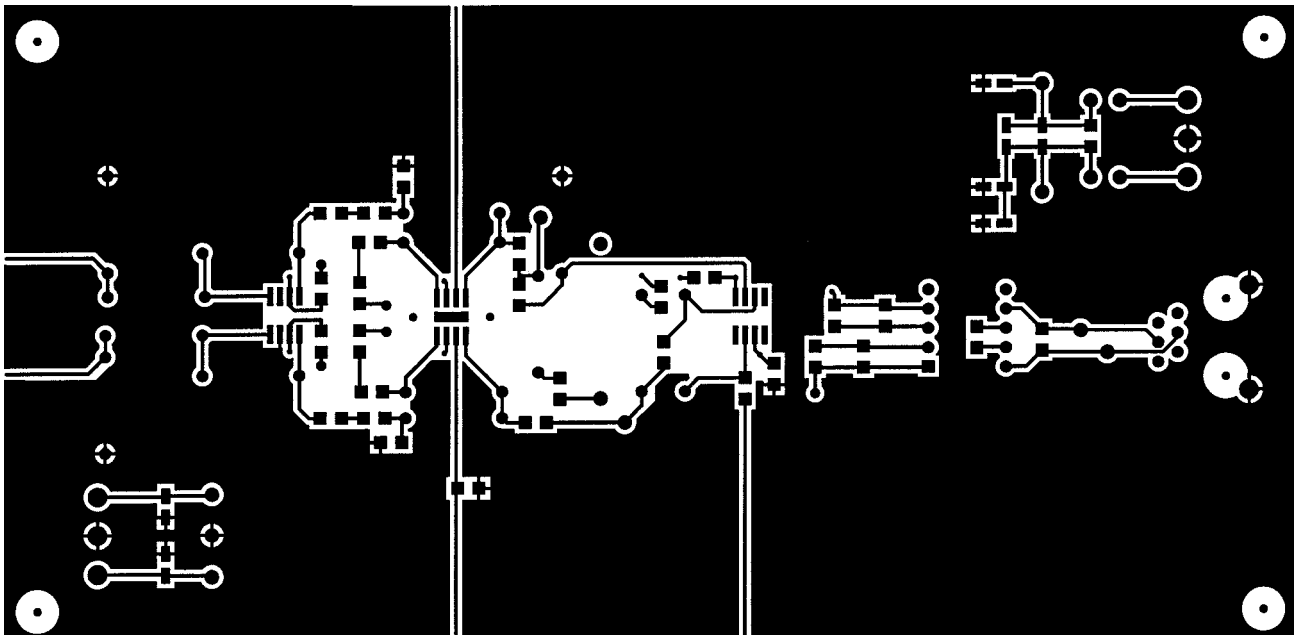


Figure 11. Layer 1—Primary Side

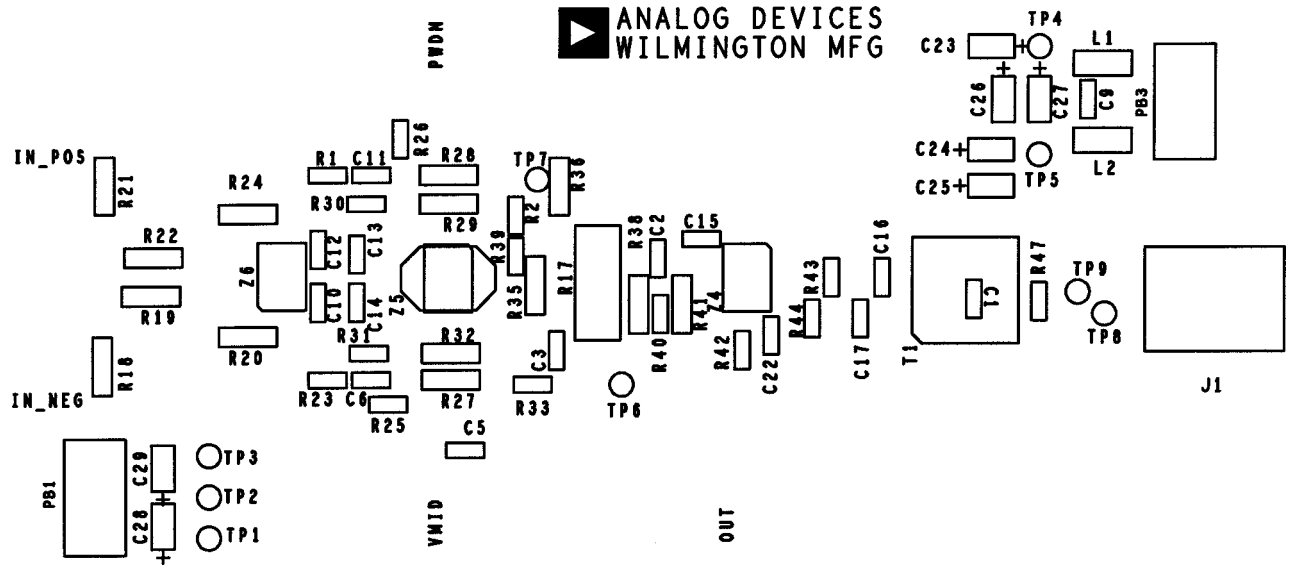


Figure 12. Silkscreen—Primary Side

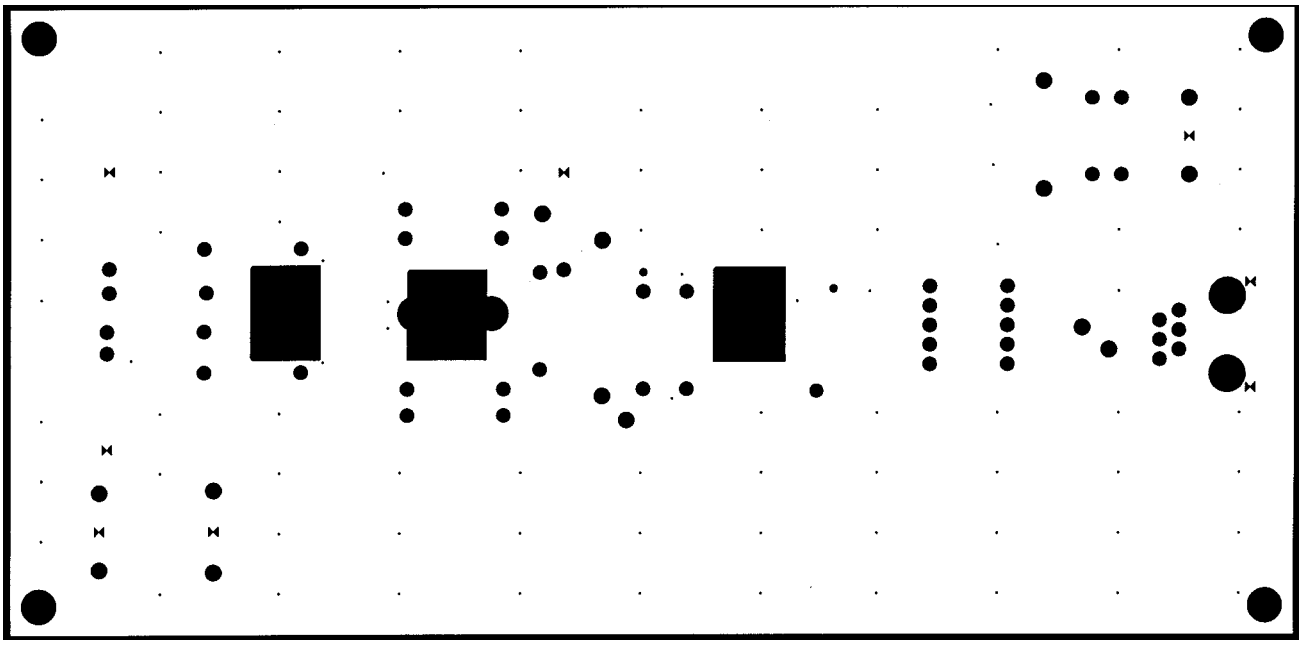


Figure 13. Layer 2—Ground Plane

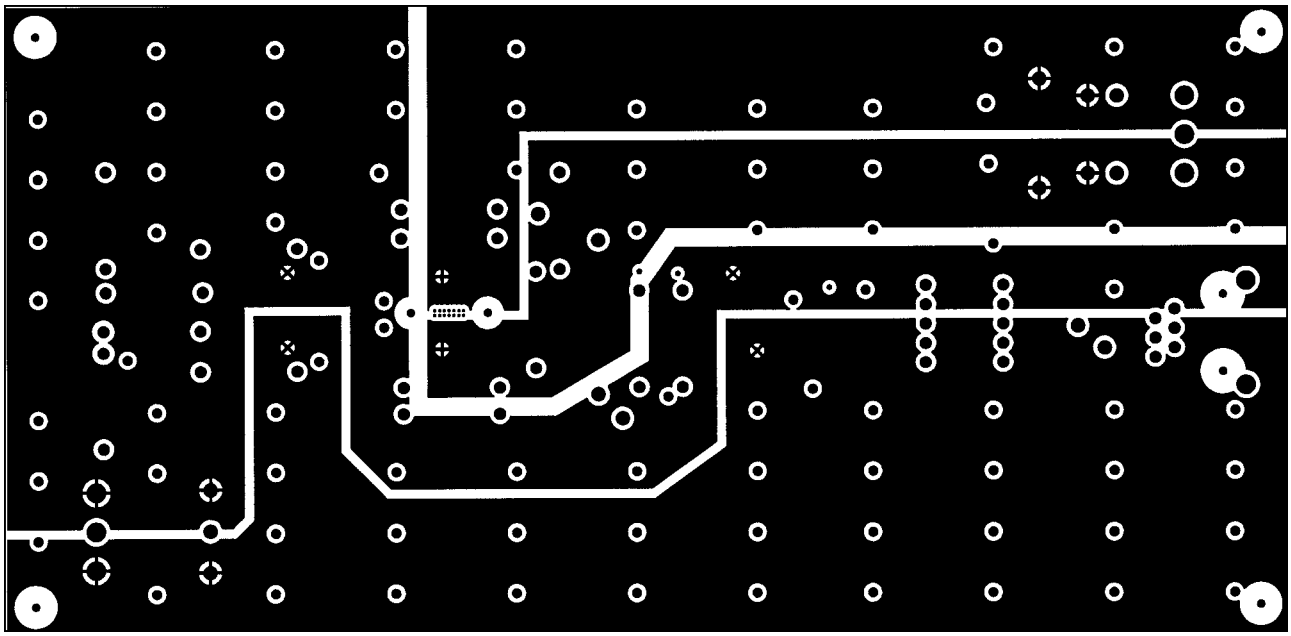


Figure 14. Layer 3—Power Plane

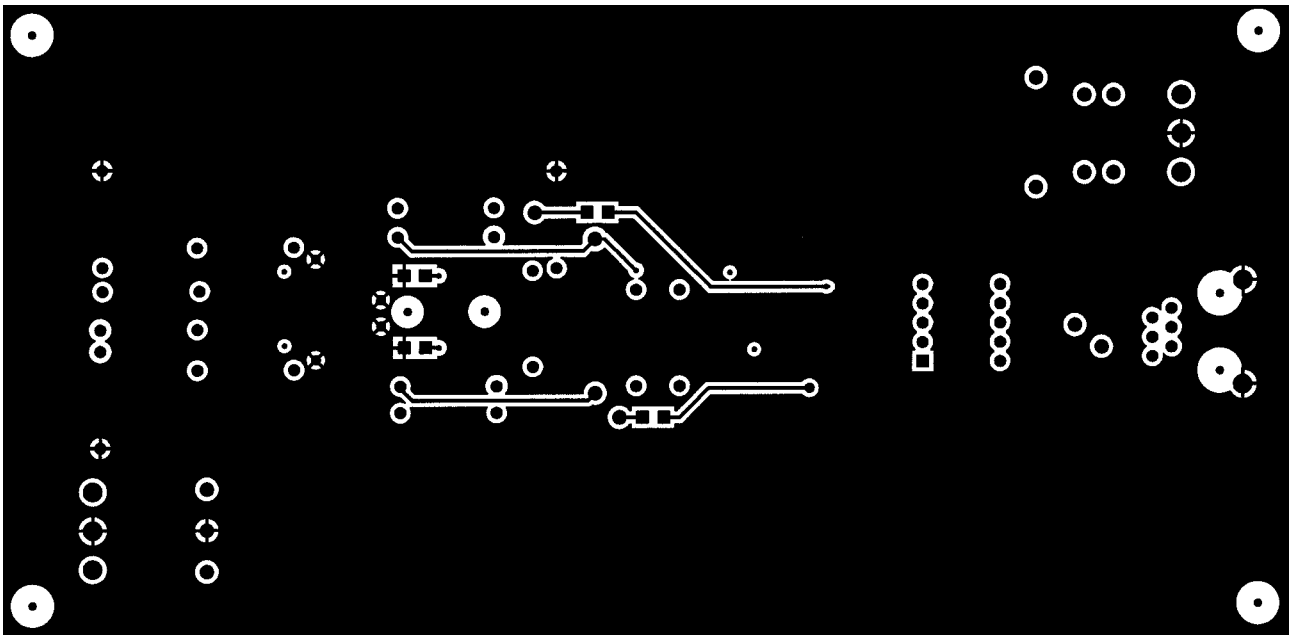


Figure 15. Layer 4—Secondary Side

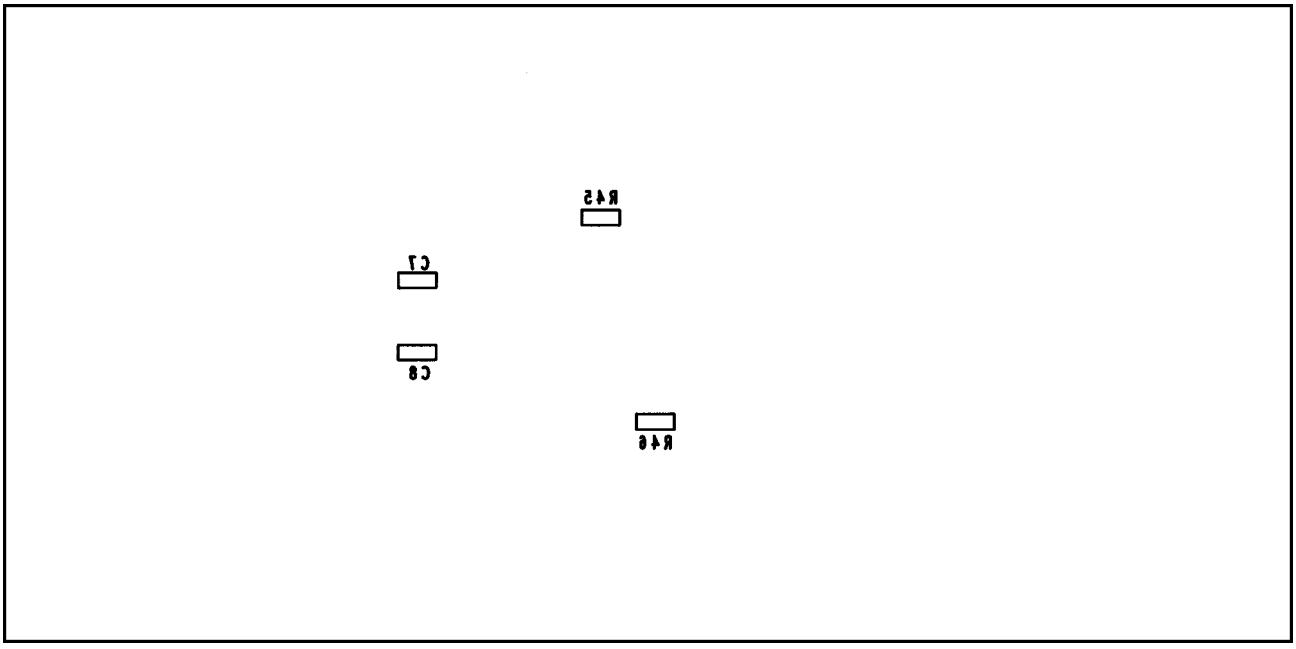


Figure 16. Layer 4—Silkscreen

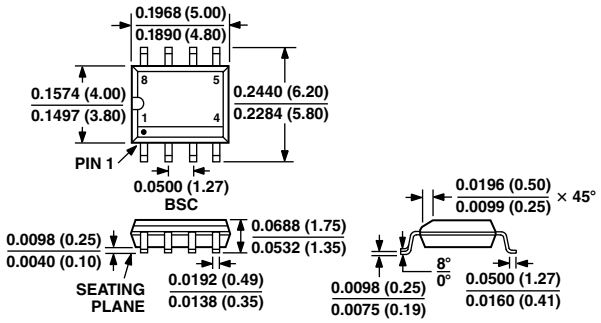
Table III. Evaluation Board Bill of Materials

Qty.	Description	Vendor	Ref Des
4	0.1 µF 50 V 1206 Size Ceramic Chip Capacitor	ADS #4-5-18	C1, C7–C9
4	0 Ω 5% 1/8 W 1206-Size Chip Resistor	ADS #3-18-88	C2, C3, C6, C11
14	DNI		C5, C10, C12–C17 C22, C25–C29
2	10 µF 16 V 'B'-Size Tantalum Chip Capacitor	ADS #4-7-24	C23–C24
4	SMA End Launch Jack (E F JOHNSON #142-0701-801)	ADS #12-1-31	IN_NEG, IN_POS PWDN, V_{MID}
1	DNI		OUT
1	AMP #555154-1 MOD. JACK (SHIELDED) 6 6	D-K #A 9024	J1
2	FERRITE CORE 1/8 inch BEAD FB43101	ADS #48-1-1	L1, L2
1	DNI	ADS #12-19-14	PB1
1	3 Green Terminal Block ONSHORE #EDZ250/3		PB3
2	0 Ω 5% 1/8 W 1206-Size Chip Resistor	ADS #3-18-88	R1, R23
2	DNI		R2, R33
1	DNI		R17
2	49.9 Ω Metal Film Resistor	ADS #3-15-3	R18, R21
6	0 Ω Metal Film Resistor	ADS #3-2-177	R19, R20, R22, R24, R35, R38
12	DNI		R25, R26, R30, R31, R39, R40 R42, R43, R44, R45, R46, R47
2	DNI		R36, R41
2	453 Ω Metal Film Resistor	ADS #3-53-1	R27, R28
2	909 Ω Metal Film Resistor	ADS #3-53-2	R29, R32
1	DNI		T1
2	Red Test Point	ADS #12-18-43	TP1, TP4
1	Black Test Point	ADS #12-18-44	TP2
2	Blue Test Point	ADS #12-18-62	TP3, TP5
2	Orange Test Point	ADS #12-18-60	TP6, TP7
2	White Test Point	ADS #12-18-42	TP8, TP9
1	AD9632 (DNI)	ADI #AD9632AR	Z4
1	AD8391	ADI #AD8391AR	Z5
1	AD8138 (DNI)	ADI #AD8138AR	Z6
4	#4-40 × 1/4 inch STAINLESS Panhead Machine Screw	ADS #30-1-1	
4	#4-40 × 3/4 inch-long Aluminum Round Stand-Off	ADS #30-16-3	

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC
(R-8)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS, INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

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