4+1-CHANNEL BUFFER FOR TFT LCD

FEATURES

- 4+1-Channel:
  4 Channels with an Output Current of ±30mA (MAX); 1 V_{com} with an Output Current of ±100mA (MAX)
- Unity Gain Buffer Capable of Driving Large Capacitive Loads
- Input Range Matched to LCD Reference Requirements
- V_{DD} Specified for 6.5V to 16V
- TSSOP14 Package

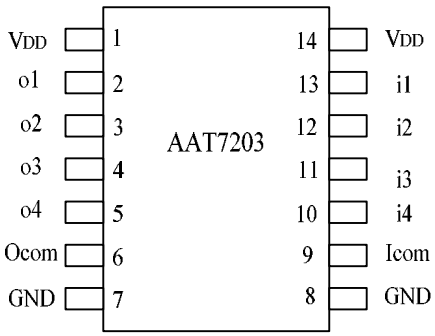
GENERAL DESCRIPTION

The AAT7203 is a 4+1-channel buffer designed for thin film transistor liquid crystal display (TFT LCD). This device consists of a V_{com} buffer circuit, two rail-to-rail buffer amplifier circuits, and 2 buffer amplifier circuits. Each buffer is capable of driving heavy capacitive loads and providing fast load current (V_{com}: 100mA, and the others: 30mA).

AAT7203 comes in a compact TSSOP14 package, which makes it an ideal component for space-sensitive designs of LCD monitors and LCD TVs.

PIN CONFIGURATION

TOP VIEW



TSSOP14

PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	V_{DD}	I	Power Supply
2	o1	O	Buffer Channel 1 Output
3	o2	O	Buffer Channel 2 Output
4	o3	O	Buffer Channel 3 Output
5	o4	O	Buffer Channel 4 Output
6	O_{com}	O	Com Buffer Output
7	GND	I	Ground
8	GND	I	Ground
9	I_{com}	I	Com Buffer Input
10	i4	I	Buffer Channel 4 Input
11	i3	I	Buffer Channel 3 Input
12	i2	I	Buffer Channel 2 Input
13	i1	I	Buffer Channel 1 Input
14	V_{DD}	I	Power Supply

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	+18	V
Input Voltage	V_I	-0.5 to $V_{DD}+0.5$	V
Output Voltage	V_O	-0.5 to $V_{DD}+0.5$	V
Output Loading Current for Gamma, Rail-to-Rail Buffer	I_L	± 30	mA
Output Loading Current for Com Buffer		± 100	mA
Maximum Junction Temperature	T_J	+125	^oC
Operating Temperature	T_C	-20 to +85	^oC
Storage Temperature	$T_{storage}$	-45 to +125	^oC
Lead Temperature (Soldering for 10 Seconds)	---	260	^oC

Note: Values beyond absolute maximum ratings may cause permanent damage to the device.

ELECTRICAL CHARACTTERISTICS (V_{DD}=10V, T_C=25°C UNLESS OTHERWISE SPECIFIED)

POWER SUPPLY PERFORMANCE

PARAMETER		TEST CONDITIONS	MN	TYP	MAX	UNITS
Power Supply Rejection Ratio	PSRR	V_{DD} varies from 6.5V to 16.0V	-	80	-	dB
Supply Current	I_S		-	6.3	-	mA

INPUT CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_I = V_{DD}/2$, $V_O = V_{DD}/2$	-	2	12	mV
Input Bias Current	I_B	$V_I = V_{DD}/2$, $V_O = V_{DD}/2$	-	2	50	nA

Note 2: Slew rate is measured on rising and falling edges.

ELECTRICAL CHARACTTERISTICS (V_{DD}=10V, T_C=25°C UNLESS OTHERWISE SPECIFIED)

OUTPUT CHARACTERISTICS

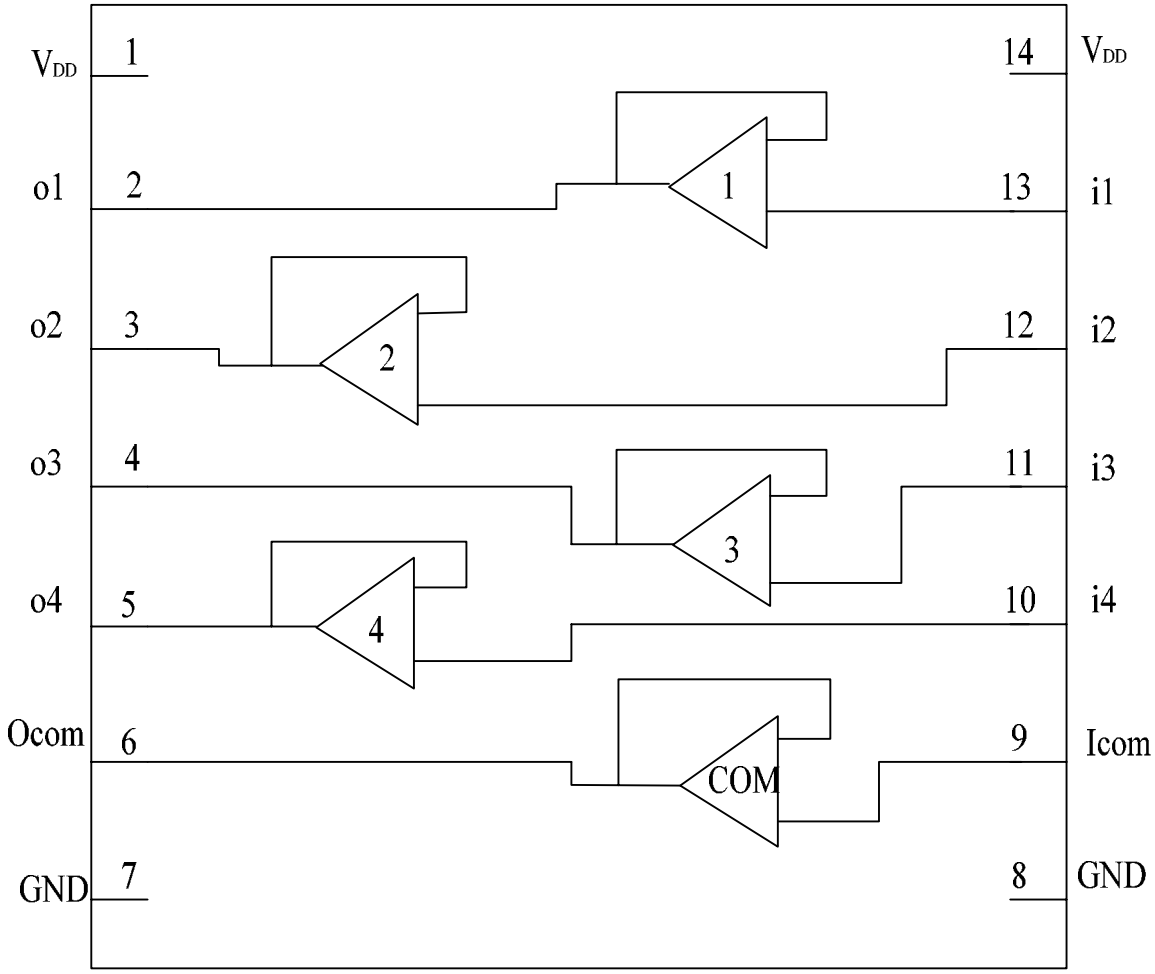
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Swing Low	V_{OL}	I_L =5mA (Buffer 1, 4) V_I =0V	-	0.08	0.15	V
		I_L =10mA (Buffer 2, 3) V_I =1V	-	1.02	1.05	V
Output Swing High	V_{OH}	I_L = – 5 mA (Buffer 1, 4) V_I =10V	9.85	9.92	-	V
		I_L = – 10 mA (Buffer 2, 3) V_I =9V	8.95	8.98	-	V
Output Swing (Buffer 2,3)	V_{OL}	I_L =10mA, V_I =5V	-	5.02	5.04	V
	V_{OH}	I_L = – 10 mA, V_I =5V	4.96	4.98	-	V
Output Swing (COM)	V_{OL}	I_L =50mA, V_I =5V	-	5.03	5.05	V
	V_{OH}	I_L = – 50 mA, V_I =5V	4.95	4.97	-	V
Short Circuit Current	I_{SC}	(Buffer 2,3)	-	± 70	-	mA
		(Com Buffer, Buffer 1, 4)	-	±180	-	mA

AC CHARACTERISTICS

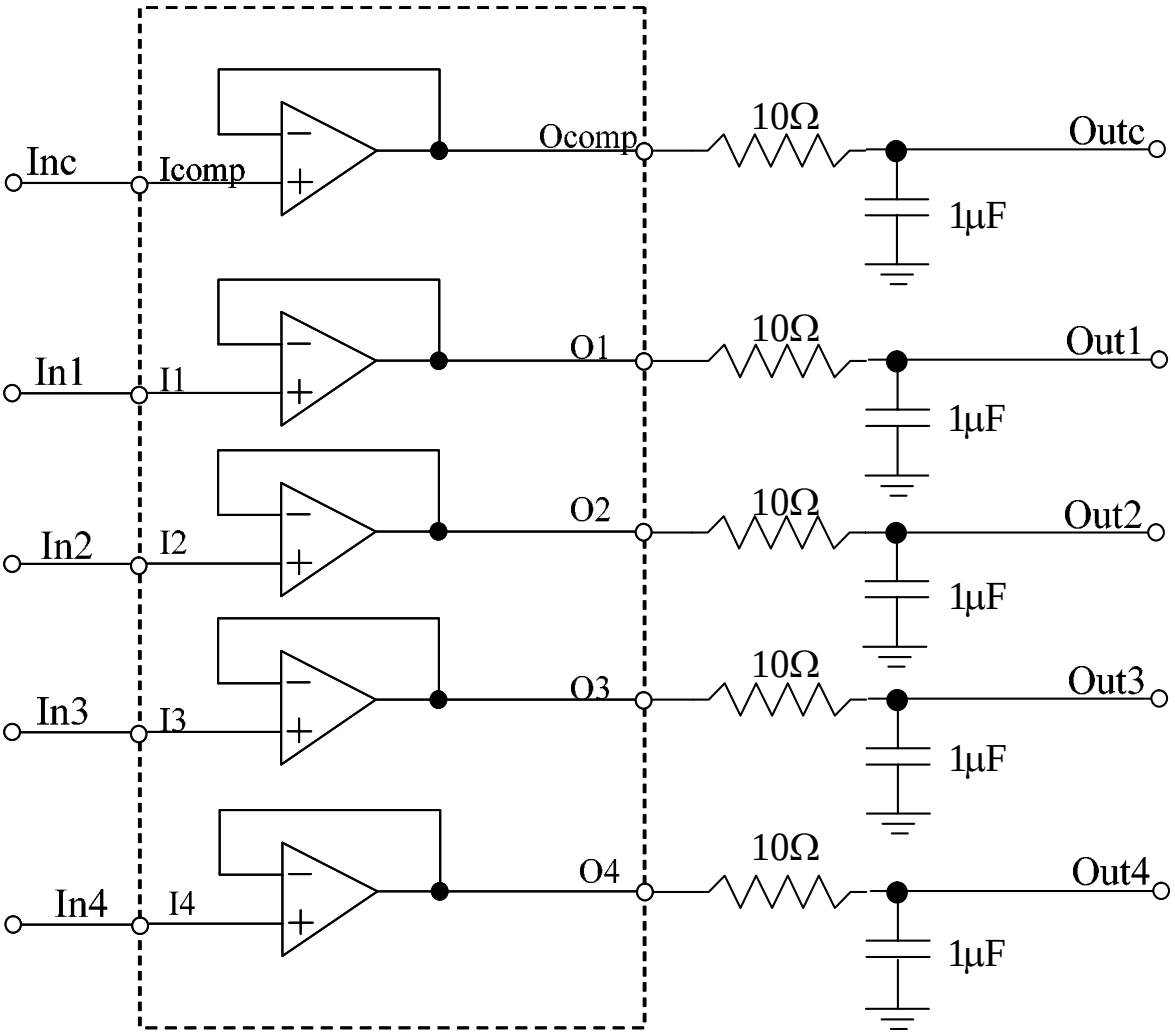
Parameter		Test Conditions	Min	Typ	Max	Units
Slew Rate (Note 2)	SR	V_I =2V to 8V, 20% to 80%	-	1	-	V/μs
Settling Time	t_s	V_I =4.5V to 5.5V 0.1% V_I =5.5V to 4.5V 0.1%	-	5	-	μs

Note 2: Slew rate is measured on rising and falling edges.

BLOCK DIAGRAM

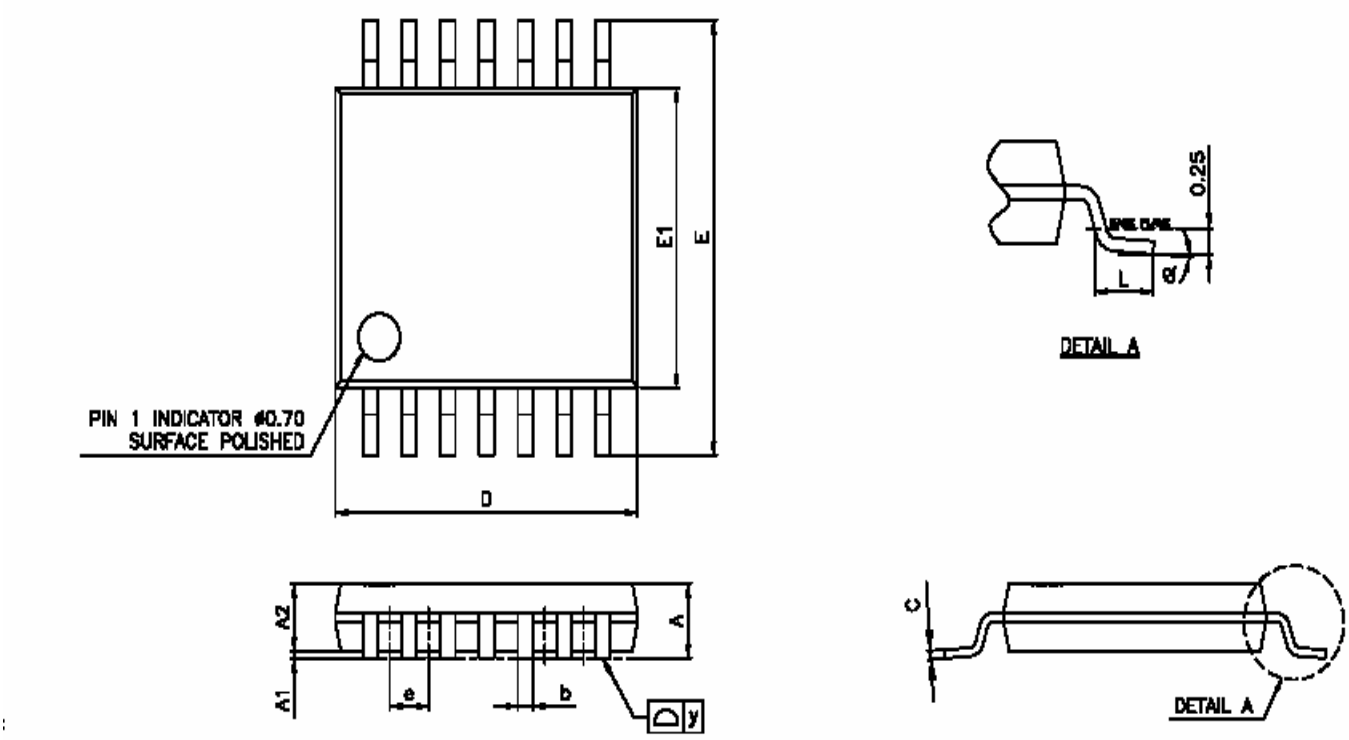


APPLICATION CIRCUIT



PACKAGE DIMENSION

TSSOP14



PACKAGE DIMENSION (CONT.)

TSSOP14

SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	---	0.30	0.007	---	0.012
C	0.09	---	0.20	0.0035	---	0.0080
D	4.90	5.00	5.10	0.193	0.197	0.201
E	---	6.40	---	0.193	0.252	0.201
E1	4.30	4.40	4.50	0.170	0.173	0.177
e	---	0.65	---	---	0.026	---
L	0.45	0.60	0.75	0.0177	0.0240	0.0295
y	---	---	0.076	---	---	0.003
θ	0°	---	8°	0°	---	8°

Note:

1. CONTROLLING DIMENSION: MILLIMETERS
2. LEAD FRAME MATERIAL: OLIN C7025/EFTEC 64T
3. DIMENSION “D” DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006” [0.15 MILLIMETERS] PER END. DIMENSION “E1” DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010” [0.25 MILLIMETERS] PER SIDE.
4. DIMENSION “b” DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003” [0.08 MILLIMETERS] TOTAL IN EXCESS OF THE “b” DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028” [0.07 MILLIMETERS]
5. TOLERANCE: ± 0.010” [0.25 MILLIMETERS] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT: JEDEC SPEC MO-153

ORDERING INFORMATION