GreenFIELD V600AT

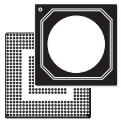
RECONFIGURABLE MICRO-CONTROLLER

DATA BRIEF

1 Product Features

- System-On-Chip integrating an ARM926 Micro-Controller, Embedded FPGA and embedded DRAM
- 16 Mbit of embedded SDRAM
- ARM926: 32/16-bit RISC Architecture with instruction set for maximum performance, flexibility and high code density running at 300 MHz, and with AMBA Bus Architecture operating at ½ CPU Frequency.
- Built-in Memory Management Unit for OS Support
- 32 kBytes L1 Program Cache and 16kBytes L1 Data Cache
- Embedded FPGA Array: 150kGates ASIC Equivalent running at 200MHz
- Power-On Reset Module with Power Supply Voltage Monitoring
- Two 10-bit 8-Channel Analog-to-Digital Converters with sampling rate of 1 Msps
- Four 10-bit Single Channel Analog-to-Digital Converters with sampling rate of 1 Msps
- Three 10-bit Digital-to-Analog Converters with sampling rate of 1 Msps
- External Memory Controller with DDR SDRAM support
- Five I^2C Bus Interfaces
- Synchronous Serial Port, including SPI and Microware compatible
- Dual Single-Channel HDLC Controllers
- 16-bit General Purpose I/O
- 32-bit Timers
- UART
- 32-channel DMA Engines
- Vectored Interrupt Controller
- System Controller, PLL and Power On Reset

Figure 1. Package



PBGA/HSP-561

Table 1. Order Codes

Part Numbers	Package
V600AT	**PBGA/HSP-561**
V600ATR	**PBGA/HSP-561 in Tape & Reel**

- Ethernet MAC
- Two HDLC
- Multi-Channel Serial Port
- Watchdog
- On-Chip Emulation / Real-Time Embedded Trace
- Development tools available

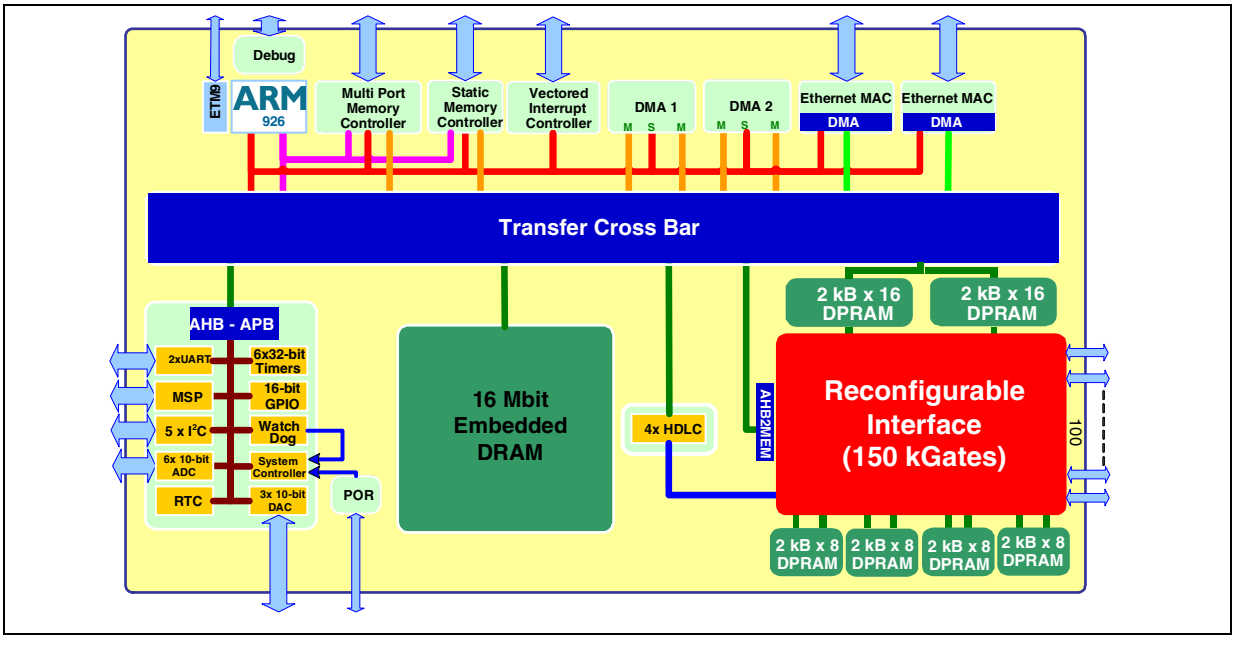
2 Overview/Description

The GreenFIELD System-On-Chip is a low-cost, versatile high performance and reconfigurable micro-controller able to manage control tasks within complex Telecommunication Infrastructure equipment such as Base Transceiver Stations.

The GreenFIELD ASSP is designed to be extremely flexible and it can be used in many places within Telecom Equipment. It can fulfill control tasks as well as monitoring. Figure 1 shows a block diagram of the GreenFIELD.

The Embedded FPGA technology offers a high degree of flexibility. It allows the GreenFIELD to be reconfigured. The Embedded FPGA can be used to remap I/Os or to implement specific custom logic.

Figure 2. GreenFIELD Block Diagram



3 Architecture Overview

The GreenFIELD micro-controller includes an ARM926 micro-controller, used as a master for the complete system. It allows the setup of peripherals within the system, as well as the control of the data flow. The GreenFIELD used with external Flash Devices can boot in stand-alone mode. The Embedded FPGA can be setup using an external Serial Flash, with the help of an I^2C or SPI Bus Interface.

The DMA Controller, allows data exchanges between specific parts of the system such as the High Speed Communication Peripherals, or the ADC/DAC converters.

The GreenFIELD bus architecture is based on the Multi-Layer AHB. This bus architecture provides a large amount of bandwidth in the system, and prevents the bus architecture from being a bottleneck.

An 16MBit memory provides data storage capability shared among the CPU, and I/O peripherals. It allows storage of a collection of data coming from HDLC Controllers, Ethernet or other DMA-based peripherals.

The Embedded FPGA offers 150k Gates of reconfigurable logic, which can represent simple custom interfaces, as well, as more complex logic designs. The FPGA Array is connected to the rest of the system, through built-in AHB Interfaces. It is connected to specific system parts such as Interrupt Controller, timer, Clock Generation, System Controller, etc… DPRAM Memories are available around the FPGA Macro, to allow processing storage or data exchange between the Embedded FPGA prototyped logic and the rest of the system.

4 ARM926 Overview

The GreenFIELD is based on the open ARM PrimeXSys platform built around the ARM926 core and includes a set of Peripherals and an AMBA Multi-Layer AHB system bus for maximized throughput.

The ARM Sub System contains a set of standard Peripherals including Timers, Watchdog, 32-bit GPIOs, and Clock/System Controller.

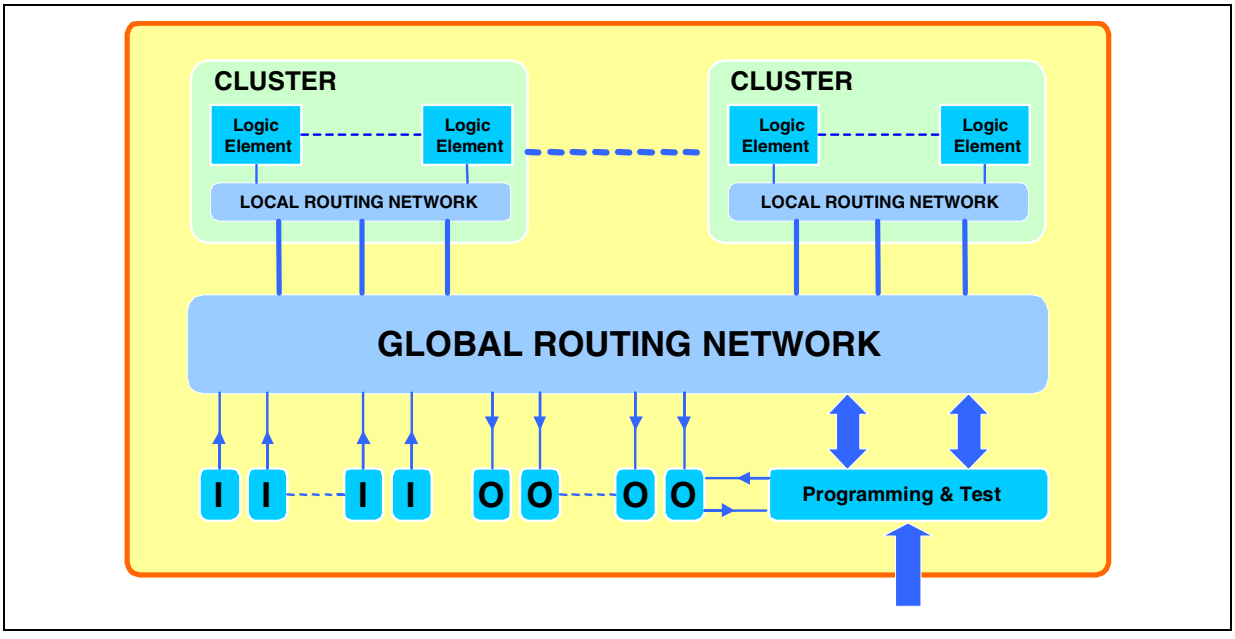
Beside the standard peripherals the ARM Sub system also contains a set of high-speed DMA Peripherals including SERDES Interface, HDLC Controller, and Ethernet MAC.

A Two Master Ports DMA Engine manages all DMA operations over the System. An Interrupt Controller with 32 standard interrupts and 16-vectored interrupts provides a simple software interface to the interrupt system. For expansion purpose, one External Memory Controller can address SRAM, Flash, ROM or I/O Devices.

5 Embedded FPGA Overview

The GreenFIELD includes an Embedded FPGA array, composed of 7168 Logic Elements over 56 clusters. 1 Cluster includes 128 Logic Elements. Overall, the Array is equivalent to 150k ASIC Gates. The macro architecture is a multi-stage hierarchical Interconnect Network ensuring a predictable and bounded delay between any programmable element and/or I/Os. A Logic Element is composed of 4 inputs and 1 output SRAM programmable element, including a 4 input LUT and a general-purpose storage element.

Figure 3. Embedded FPGA Macro Architecture



6 ADC-DAC OVERVIEW

The GreenFIELD includes two 8-input 10-bit Analog-to-Digital converters, with sampling rates of 1 Msps. The ADCs have an input range of 0 to 2.4 V.
It includes also, four 10-bit Digital-to-Analog converter, delivering 1 Msps with an output range from 0 to 2V. Both ADC and DAC implement Low-Power modes with fast wake-up times.

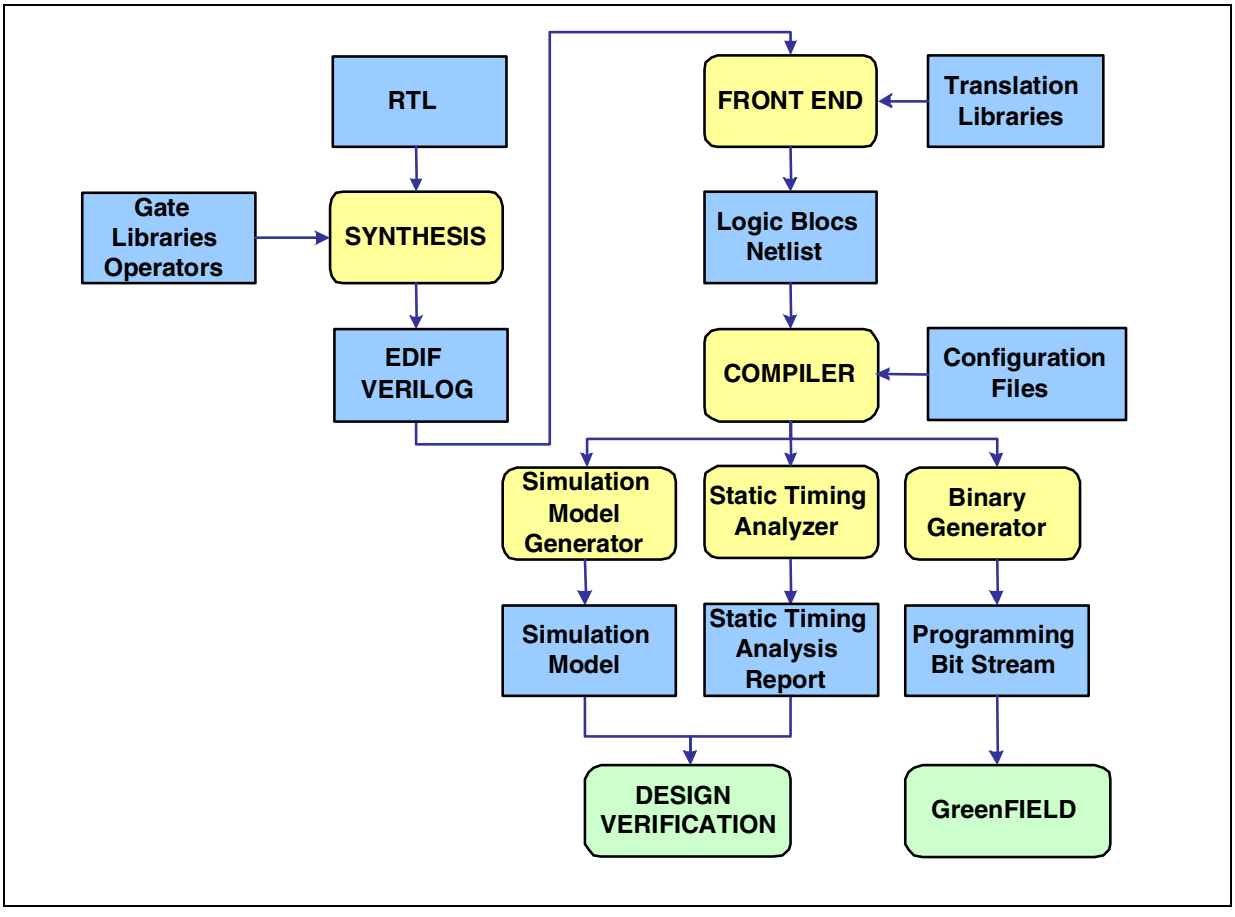
7 Development Support

STMicroelectronics provides a complete set of development tools around the GreenFIELD Micro-Controller, to evaluate performance, develop, debug and integrate Application Code.

7.1 FPGA Development Tools:

To design and program the Embedded FPGA Array, a comprehensive and standard development flow allows the use of 3rd Party tools for Synthesis. The mapping on the Embedded FPGA array is performed by dedicated proprietary tools which take advantage of the FPGA technology to obtain optimal results.

Figure 4. Embedded FPGA Design Flow



7.2 Software Development Tools:

Software Development Tools for the ARM926 include an Integrated Development Environment tool, the C/C++ Compiler, Assembler and Linker, Instruction Set Simulator and OS-aware Debugger for Simulation and Emulation Debug. Beside standard Software Development Tools, RTOS dedicated tools for application-level debugging and analysis of embedded applications are also available. They include Runtime Debugging, System and Process information viewing, Manual Process Control, System Event Tracing and Monitoring, Memory Analysis and Message Search, CPU usage analysis and more.

7.3 Hardware development tools

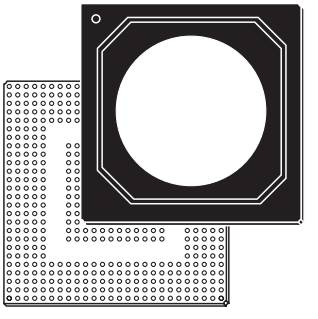
In addition to the Software Development Tools, a complete set of Hardware tools help GreenFIELD users to speed-up the development of new applications. The GreenFIELD Starter Kit can be used to evaluate GreenFIELD performance, as well as to develop Software Applications. The Starter Kit offers a basic set of peripherals in addition to the GreenFIELD built-in peripherals. The starter kit is usable as a stand-alone board, or as a daughter card. In the latter case, multiple daughter cards can be plugged on a System Application Backbone (mother board), which represents the prototype system. The GreenFIELD Starter kit includes a complete Board Support Package.

8 Package Information

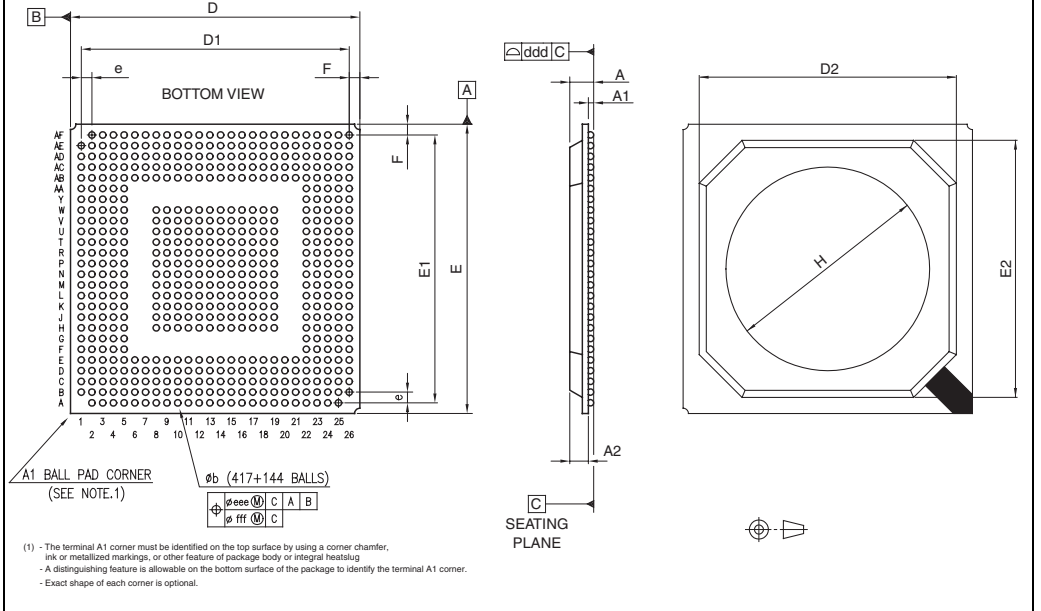
Figure 5. PBGA/HSP-561 (27x27x2.36mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.36			0.093
A1	0.30			0.012		
A2		1.73			0.068	
b	0.50	0.60	0.70	0.020	0.024	0.027
D	26.80	27.00	27.20	1.055	1.071	1.070
D1		25.00			0.984	
D2		24.00			0.945	
E	26.80	27.00	27.20	1.055	1.071	1.070
E1		25.00			0.984	
E2		24.00			0.945	
e		1.00			0.039	
F		1.00			0.039	
H		19.50			0.768	
ddd			0.20			0.008
eee			0.25			0.010
fff			0.10			0.004

OUTLINE AND MECHANICAL DATA



PBGA/HSp-561 (27x27x2.36mm)
Heat Spreader Plastic Ball Grid Array



9 Revision History

Table 2. Revision History

Date	Revision	Description of Changes
January 2005	1	First Issue
February 2005	2	Slightly modified Feature section on page 1.
14th February 2005	3	Modified Feature on page 1 and changed the Block Diagram on page 2.