

# SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS707E – SEPTEMBER 1997 – REVISED OCTOBER 2003

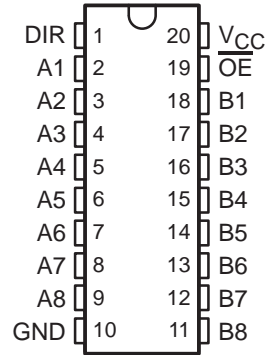
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- B-Port Outputs Have Equivalent 22- $\Omega$  Series Resistors, So No External Resistors Are Required
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## description/ordering information

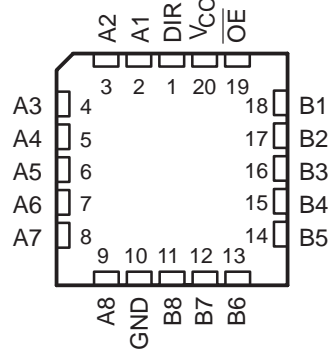
These octal bus transceivers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the devices so the buses are effectively isolated.

SN54LVTH2245 . . . J OR W PACKAGE  
SN74LVTH2245 . . . DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LVTH2245 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74LVTH2245DW	LVTH2245
		Tape and reel	SN74LVTH2245DWR	
	SOP – NS	Tape and reel	SN74LVTH2245NSR	LVTH2245
	SSOP – DB	Tape and reel	SN74LVTH2245DBR	LK245
	TSSOP – PW	Tube	SN74LVTH2245PW	LK245
		Tape and reel	SN74LVTH2245PWR	
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74LVTH2245DGVR	LK245
	CDIP – J	Tube	SNJ54LVTH2245J	SNJ54LVTH2245J
	CFP – W	Tube	SNJ54LVTH2245W	SNJ54LVTH2245W
	LCCC – FK	Tube	SNJ54LVTH2245FK	SNJ54LVTH2245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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SN54LVTH2245, SN74LVTH2245  
3.3-V ABT OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

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description/ordering information (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

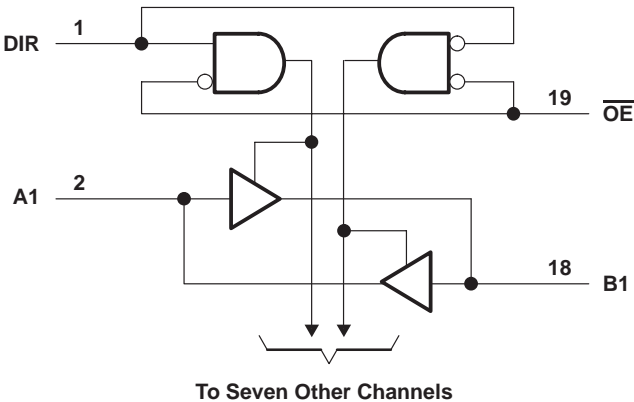
When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



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## 3

# SN54LVTH2245, SN74LVTH2245

## 3.3-V ABT OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH2245			SN74LVTH2245			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V <sub>IK</sub>		V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = −18 mA		−1.2			−1.2			V	
V <sub>OH</sub>	A port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = −100 μA		V <sub>CC</sub> −0.2			V <sub>CC</sub> −0.2			V	
		V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = −8 mA		2.4			2.4				
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = −24 mA		2						
			I <sub>OH</sub> = −32 mA					2			
	B port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = −100 μA		V <sub>CC</sub> −0.2			V <sub>CC</sub> −0.2				
		V <sub>CC</sub> = 3 V, I <sub>OH</sub> = −12 mA		2			2				
V <sub>OL</sub>	A port	V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 μA		0.2			0.2			V
			I <sub>OL</sub> = 24 mA		0.5			0.5			
		V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA		0.4			0.4			
			I <sub>OL</sub> = 32 mA		0.5			0.5			
			I <sub>OL</sub> = 48 mA		0.55						
			I <sub>OL</sub> = 64 mA					0.55			
	B port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OL</sub> = 100 μA		0.2			0.2				
		V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 12 mA		0.8			0.8				
	I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1			±1			
V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V			10			10					
A or B ports‡		V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = 5.5 V		20			20			
			V <sub>I</sub> = V <sub>CC</sub>		1			1			
			V <sub>I</sub> = 0		−5			−5			
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V					±100			μA	
I <sub>I</sub> (hold)	A or B ports	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V		75			75			μA
			V <sub>I</sub> = 2 V		−75			−75			
		V <sub>CC</sub> = 3.6 V§, V <sub>I</sub> = 0 to 3.6 V					500 −750				
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I <sub>OZPD</sub>		V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		0.19			0.1 0.19		mA	
			Outputs low		5			3 5			
			Outputs disabled		0.19			0.1 0.19			
ΔI <sub>CC</sub> ¶		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.2			0.2			mA	
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0		4			4			pF	
C <sub>io</sub>		V <sub>O</sub> = 3 V or 0		9			9			pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused terminals are at  $V_{CC}\text{ or GND}$ .

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}\text{ or GND}$ .

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH2245				SN74LVTH2245				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
tPLH	A	B	1	4.6	5.3		1.1	2.9	4.4	5.1		ns
tPHL			1	4.6	5.3		1.1	2.6	4.4	5.1		
tPLH	B	A	1	3.7	4.2		1.1	2.2	3.5	4		ns
tPHL			1	3.7	4.2		1.1	2	3.5	4		
tPZH	$\overline{OE}$	A	1.2	5.7	7.4		1.3	3.1	5.5	7.1		ns
tPZL			1.6	5.7	6.8		1.7	3.2	5.5	6.5		
tPHZ	$\overline{OE}$	A	2	6.2	6.8		2.2	3.6	5.9	6.5		ns
tPLZ			2	5.3	5.5		2.2	3.4	5	5.1		
tPZH	$\overline{OE}$	B	1.2	6.4	7.6		1.3	3.5	6.2	7.3		ns
tPZL			1.6	6.4	7.5		1.7	3.7	6.2	7.3		
tPHZ	$\overline{OE}$	B	2	6.1	6.8		2.2	3.9	5.9	6.5		ns
tPLZ			2	5.7	5.9		2.2	3.7	5.4	5.7		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

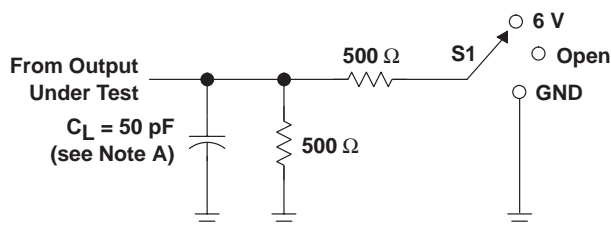
# SN54LVTH2245, SN74LVTH2245

## 3.3-V ABT OCTAL BUS TRANSCEIVERS

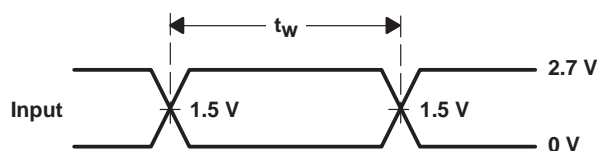
### WITH 3-STATE OUTPUTS

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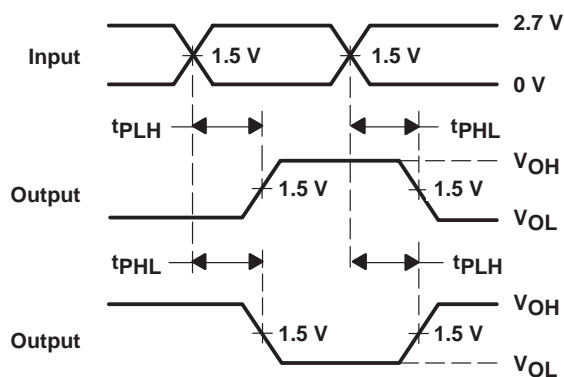
#### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

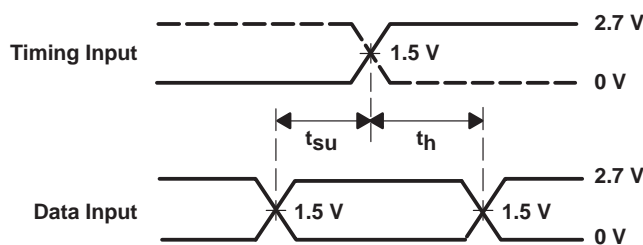


VOLTAGE WAVEFORMS  
PULSE DURATION

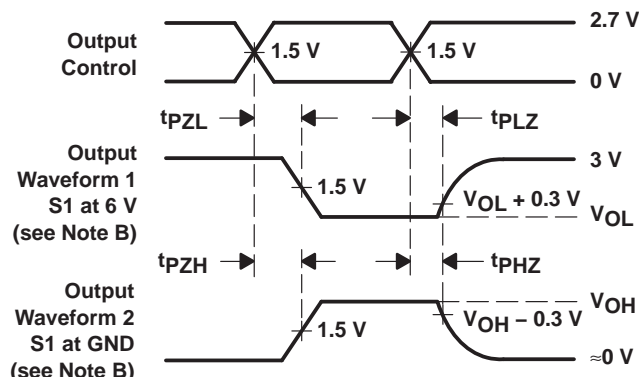


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVTH2245DBLE	OBSOLETE	SSOP	DB	20		None	Call TI	Call TI
SN74LVTH2245DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVTH2245DGVR	ACTIVE	TVSOP	DGV	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVTH2245DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LVTH2245DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LVTH2245NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVTH2245PW	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVTH2245PWLE	OBSOLETE	TSSOP	PW	20		None	Call TI	Call TI
SN74LVTH2245PWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN

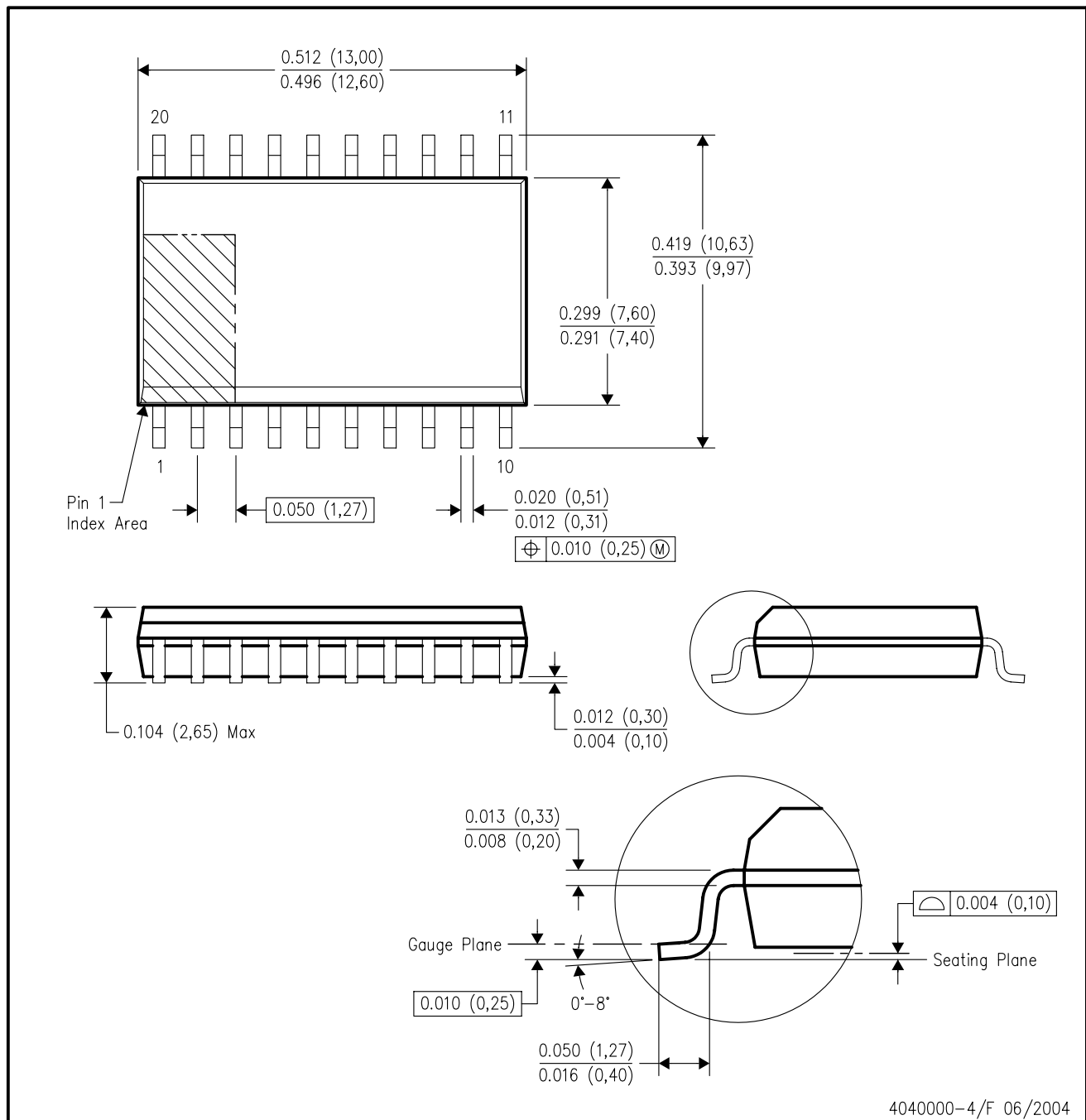


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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