SN54LVTH16500, SN74LVTH16500
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
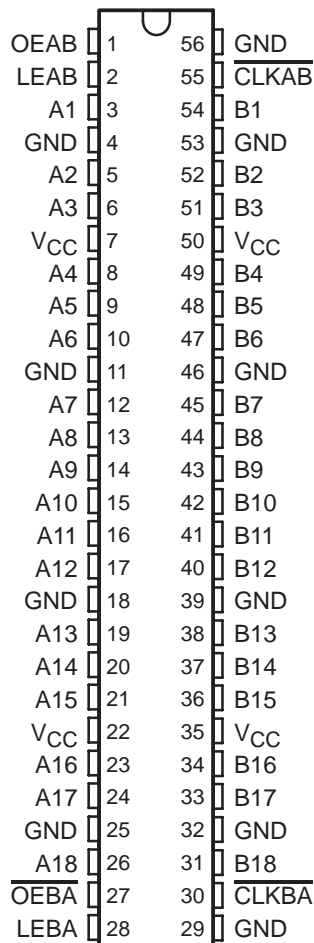
- Members of the Texas Instruments Widebus™ Family
- UBT™ Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
  – 200-V Machine Model (A115-A)
  – 1000-V Charged-Device Model (C101)

SN54LVTH16500 . . . WD PACKAGE
SN74LVTH16500 . . . DGG OR DL PACKAGE
(TOP VIEW)

```
         ┌───────⌄───────┐
  OEAB  [│1            56│]  GND
  LEAB  [│2            55│]  CLKAB
    A1  [│3            54│]  B1
   GND  [│4            53│]  GND
    A2  [│5            52│]  B2
    A3  [│6            51│]  B3
   VCC  [│7            50│]  VCC
    A4  [│8            49│]  B4
    A5  [│9            48│]  B5
    A6  [│10           47│]  B6
   GND  [│11           46│]  GND
    A7  [│12           45│]  B7
    A8  [│13           44│]  B8
    A9  [│14           43│]  B9
   A10  [│15           42│]  B10
   A11  [│16           41│]  B11
   A12  [│17           40│]  B12
   GND  [│18           39│]  GND
   A13  [│19           38│]  B13
   A14  [│20           37│]  B14
   A15  [│21           36│]  B15
   VCC  [│22           35│]  VCC
   A16  [│23           34│]  B16
   A17  [│24           33│]  B17
   GND  [│25           32│]  GND
   A18  [│26           31│]  B18
  OEBA  [│27           30│]  CLKBA
  LEBA  [│28           29│]  GND
         └───────────────┘
```

description/ordering information

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74LVTH16500DL	LVTH16500
		Tape and reel	SN74LVTH16500DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH16500DGGR	LVTH16500
	VFBGA – GQL	Tape and reel	SN74LVTH16500GQLR	LL500
	VFBGA – ZQL (Pb-free)		SN74LVTH16500ZQLR	
−55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16500WD	SNJ54LVTH16500WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE
(TOP VIEW)
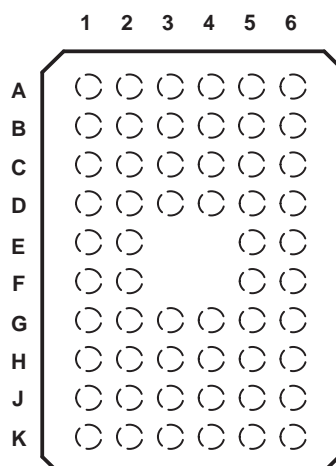
terminal assignments

	1	2	3	4	5	6
A	A1	LEAB	OEAB	GND	$\overline{\text{CLKAB}}$	B1
B	A3	A2	GND	GND	B2	B3
C	A5	A4	V_{CC}	V_{CC}	B4	B5
D	A7	A6	GND	GND	B6	B7
E	A9	A8			B8	B9
F	A10	A11			B11	B10
G	A12	A13	GND	GND	B13	B12
H	A14	A15	V_{CC}	V_{CC}	B15	B14
J	A16	A17	GND	GND	B17	B16
K	A18	$\overline{\text{OEBA}}$	LEBA	GND	$\overline{\text{CLKBA}}$	B18

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FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.
‡ Output level before the indicated steady-state input conditions were established
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low

logic diagram (positive logic)

To 17 Other Channels
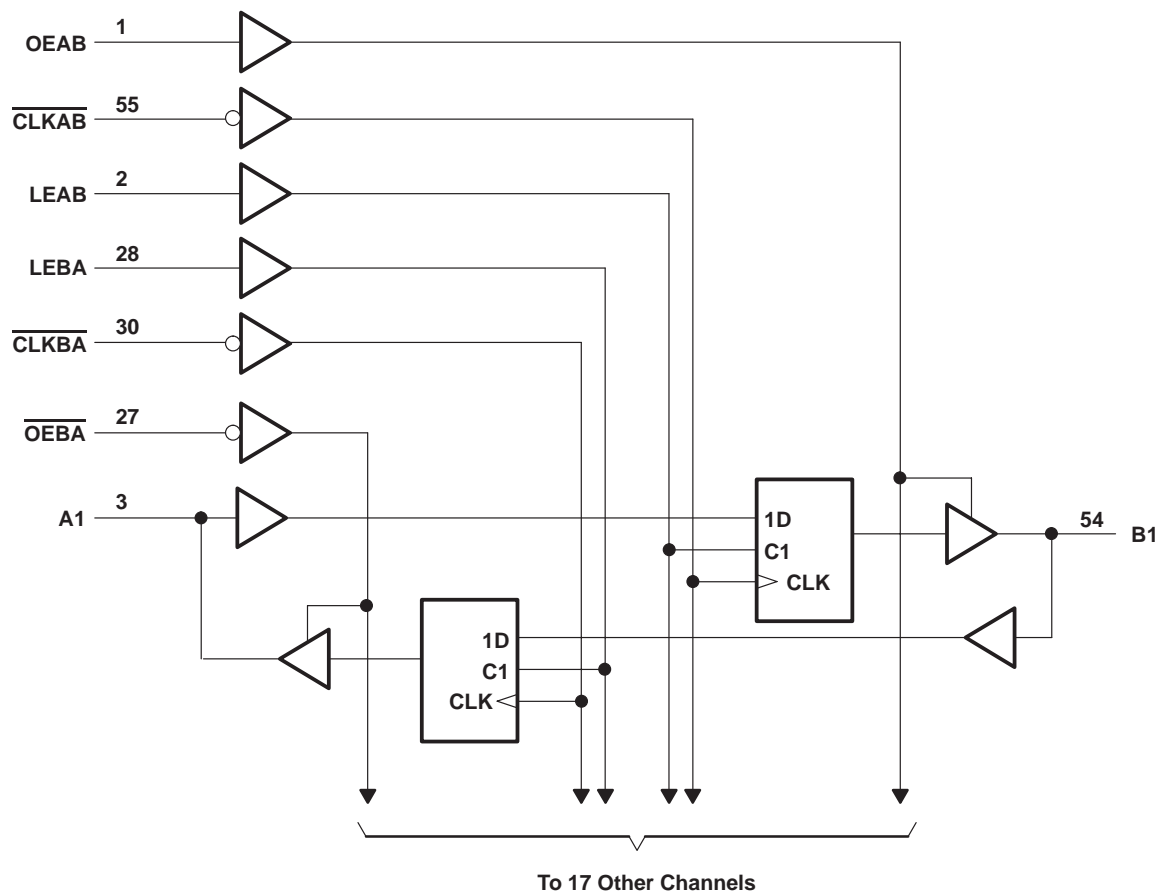
Pin numbers shown are for the DGG, DL, and WD packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V

Voltage range applied to any output in the high-impedance
   or power-off state, V_O (see Note 1) .... −0.5 V to 7 V

Voltage range applied to any output in the high state, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V

Current into any output in the low state, I_O: SN54LVTH16500 .... 96 mA
                                         SN74LVTH16500 .... 128 mA

Current into any output in the high state, I_O (see Note 2): SN54LVTH16500 .... 48 mA
                                              SN74LVTH16500 .... 64 mA

Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA

Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA

Package thermal impedance, θ_{JA} (see Note 3): DGG package .... 64°C/W
                                           DL package .... 56°C/W
                                           GQL/ZQL package .... 42°C/W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
       2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
       3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVTH16500		SN74LVTH16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16500 MIN	TYP†	MAX	SN74LVTH16500 MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B ports‡	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	A or B ports	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	−75			−75			
		V_{CC} = 3.6 V§,	V_I = 0 to 3.6 V						±500	
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$/OE = don't care				±100*			±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$/OE = don't care				±100*			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}¶		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0				4			4	pF
C_{io}		V_O = 3 V or 0				10			10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Unused pins at V_{CC} or GND
§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH16500				SN74LVTH16500				UNIT
			V_{CC} = 3.3 V $\pm$ 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150		150	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before CLKAB↓	3.1		3.1		2.9		2.9		ns
		B before CLKBA↓	3.1		3.1		2.9		2.9		
		A or B before LE↓ — CLK high	1.5		0.6		1.4		0.5		
		A or B before LE↓ — CLK low	3.1		2.5		2.9		2.3		
t_h	Hold time	A or B after CLK↓	0.4		0.4		0.4		0.4		ns
		A or B after LE↓	1.7		1.7		1.6		1.6		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)
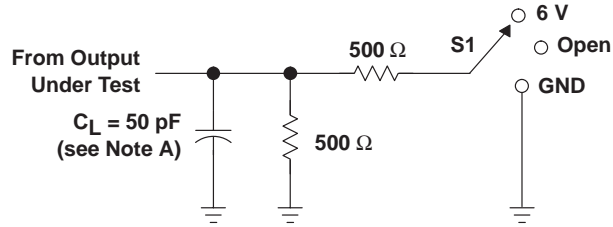
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16500				SN74LVTH16500					UNIT
			V_{CC} = 3.3 V $\pm$ 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP[†]	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	B or A	A or B	1.2	3.9		4.1	1.3	2.8	3.7		4	ns
t_{PHL}			1.2	3.9		4.1	1.3	2.6	3.7		4	
t_{PLH}	LEBA or LEAB	A or B	1.4	5.5		5.9	1.5	3.8	5.1		5.7	ns
t_{PHL}			1.4	5.5		5.9	1.5	3.8	5.1		5.7	
t_{PLH}	CLKBA or CLKAB	A or B	1.2	5.3		6.1	1.3	3.6	5		5.9	ns
t_{PHL}			1.2	5.3		6.1	1.3	3.5	5		5.9	
t_{PZH}	OEBA or OEAB	A or B	1.2	5.1		5.8	1.3	3.6	4.8		5.5	ns
t_{PZL}			1.2	5.1		5.8	1.3	3.6	4.8		5.5	
t_{PHZ}	OEBA or OEAB	A or B	1.6	6.1		6.6	1.7	4.5	5.8		6.3	ns
t_{PLZ}			1.6	6.1		6.6	1.7	4.1	5.8		6.3	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION

From Output Under Test

500 Ω S1

6 V
Open
GND

C_L = 50 pF
(see Note A)

500 Ω

TEST	S1
t_{PHL}/t_{PLH}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

Timing Input

2.7 V
1.5 V
0 V

t_{su} t_h

Data Input

2.7 V
1.5 V 1.5 V
0 V

Input

t_w

2.7 V
1.5 V 1.5 V
0 V

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

Input

2.7 V
1.5 V 1.5 V
0 V

t_{PLH} t_{PHL}

Output

V_{OH}
1.5 V 1.5 V
V_{OL}

t_{PHL} t_{PLH}

Output

V_{OH}
1.5 V 1.5 V
V_{OL}
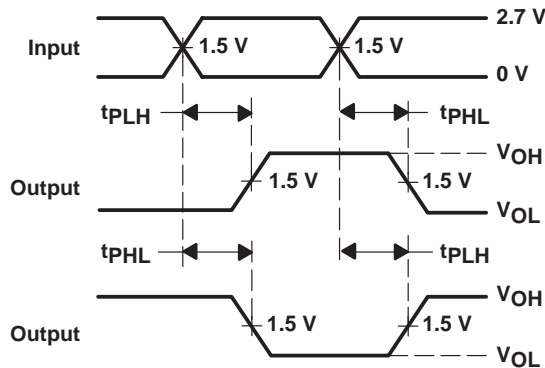
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

Output Control

2.7 V
1.5 V 1.5 V
0 V

t_{PZL} t_{PLZ}

Output
Waveform 1
S1 at 6 V
(see Note B)

3 V
1.5 V
V_{OL} + 0.3 V V_{OL}

t_{PZH} t_{PHZ}

Output
Waveform 2
S1 at GND
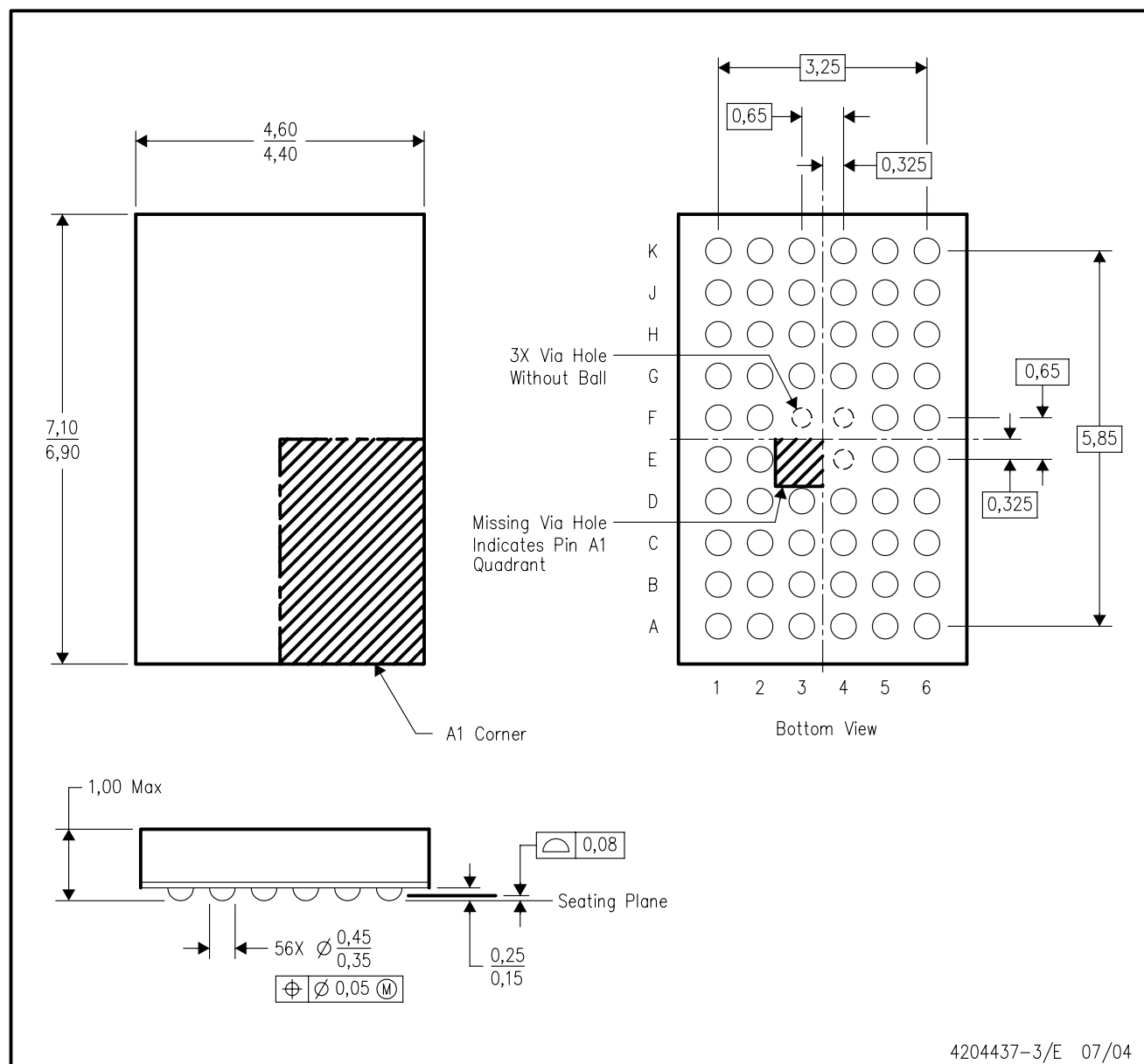(see Note B)

V_{OH}
1.5 V V_{OH} – 0.3 V
≈0 V
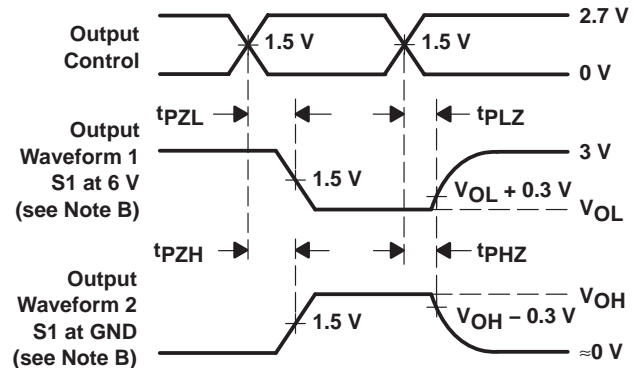
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

ZQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY

4,60
4,40

7,10
6,90

A1 Corner

3,25

0,65

0,325

K
J
H

3X Via Hole
Without Ball

G

F

E

Missing Via Hole
Indicates Pin A1
Quadrant

D
C
B
A

1 2 3 4 5 6

Bottom View

0,65

5,85

0,325

1,00 Max

0,08

Seating Plane

56X Ø 0,45
       0,35
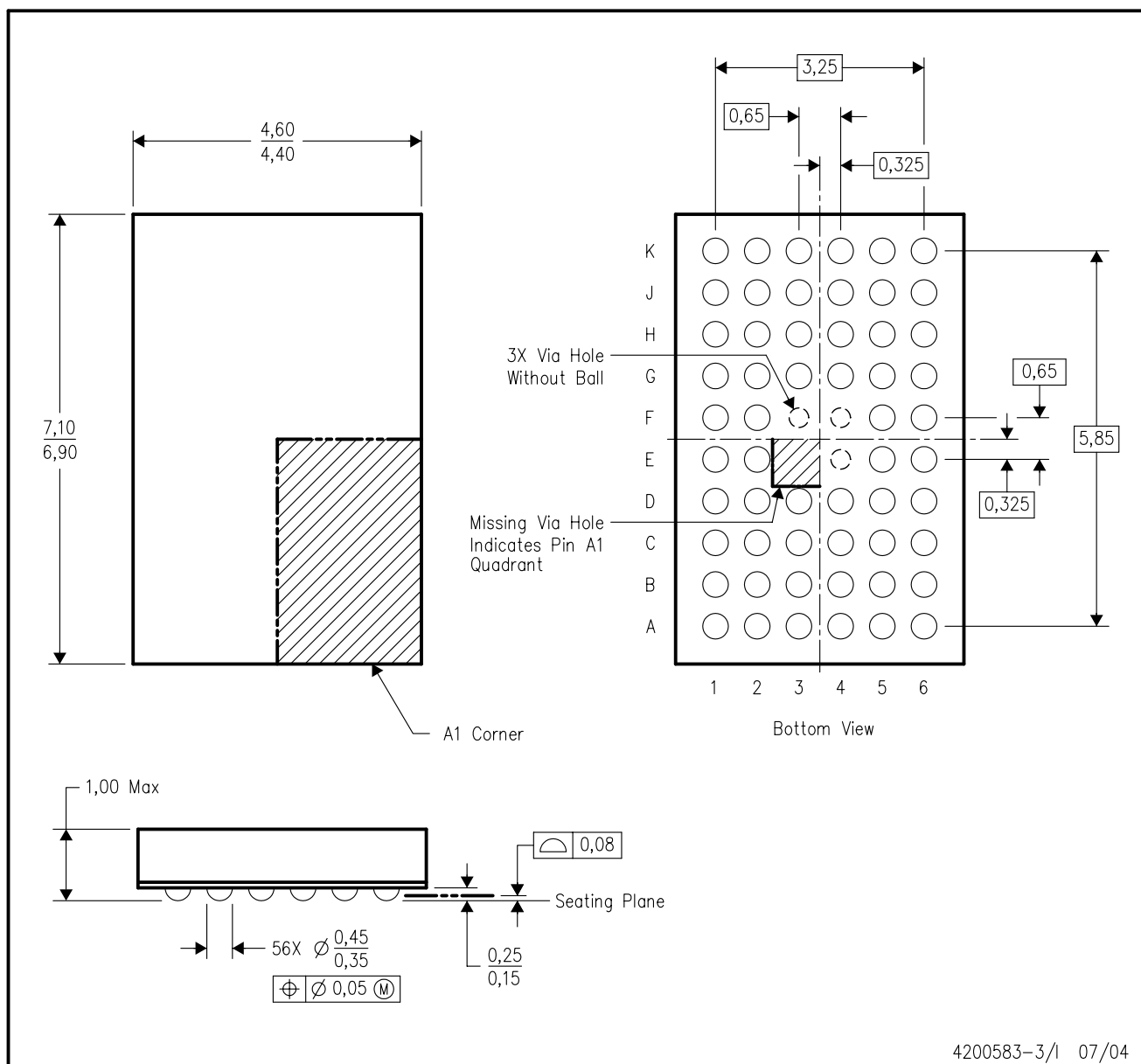
0,25
0,15

⊕ Ø 0,05 Ⓜ

4204437−3/E 07/04

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MO−225 variation BA.
        D. This package is lead−free. Refer to the 56 GQL package (drawing 4200583) for tin−lead (SnPb).

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GQL (R−PBGA−N56) PLASTIC BALL GRID ARRAY

4,60 / 4,40

7,10 / 6,90

A1 Corner

3,25

0,65

0,325

3X Via Hole Without Ball

Missing Via Hole Indicates Pin A1 Quadrant

0,65

5,85

0,325

K J H G F E D C B A

1 2 3 4 5 6

Bottom View

1,00 Max

56X Ø 0,45 / 0,35

⊕ Ø 0,05 Ⓜ

0,08

Seating Plane

0,25 / 0,15

4200583−3/I 07/04

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO−225 variation BA.
D. This package is tin−lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead−free.

DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
　　　　B. This drawing is subject to change without notice.
　　　　C. Body dimensions do not include mold protrusion not to exceed 0,15.
　　　　D. Falls within JEDEC MO-153

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