

32Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.7μm CMOS
- Organization : 32Kx8
- Power Supply Voltage : Single 5V ±10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
- 28-DIP, 28-SOP, 28-TSOP I -Forward/Reverse

GENERAL DESCRIPTION

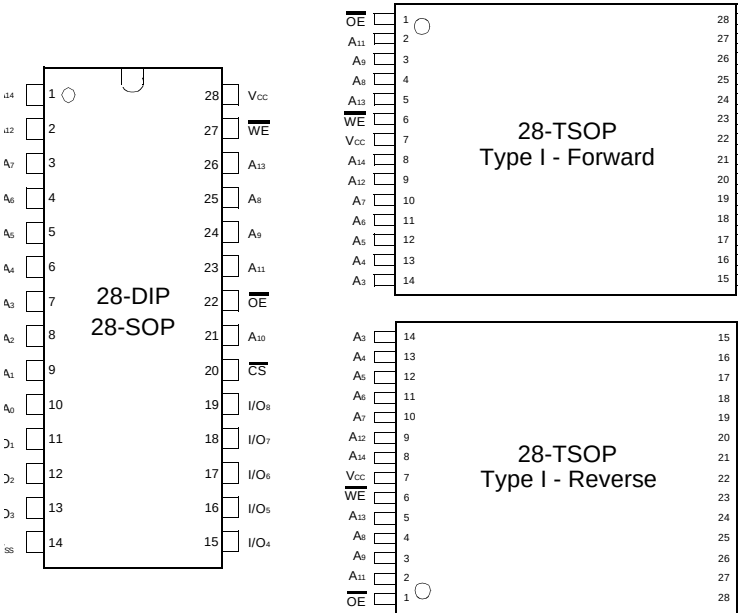
The KM62256C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

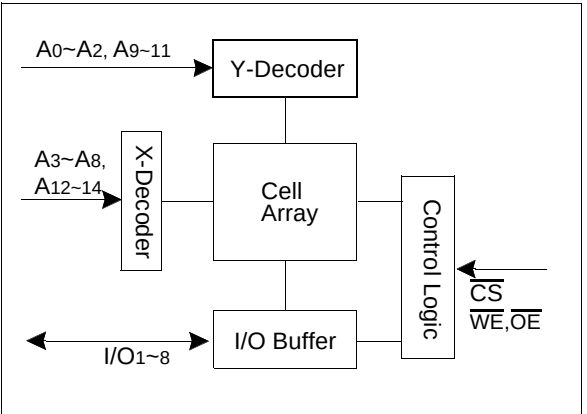
| Product Family             | Operating Temperature. | Speed (ns)  | PKG Type                        | Power Dissipation                |                               |
|----------------------------|------------------------|-------------|---------------------------------|----------------------------------|-------------------------------|
|                            |                        |             |                                 | Standby (I <sub>SB1</sub> , Max) | Operating (I <sub>CC2</sub> ) |
| KM62256CL<br>KM62256CL-L   | Commercial (0~70°C)    | 45*/55/70ns | 28-DIP, 28-SOP<br>28-TSOP I R/F | 100μW<br>20μW                    | 70mA                          |
| KM62256CLE<br>KM62256CLE-L | Extended (-25~85°C)    | 70/100ns    | 28-SOP<br>28-TSOP I R/F         | 100μW<br>50μW                    |                               |
| KM62256CLI<br>KM62256CLI-L | Industrial (-40~85°C)  | 70/100ns    | 28-SOP<br>28-TSOP I R/F         | 100μW<br>50μW                    |                               |

\* The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



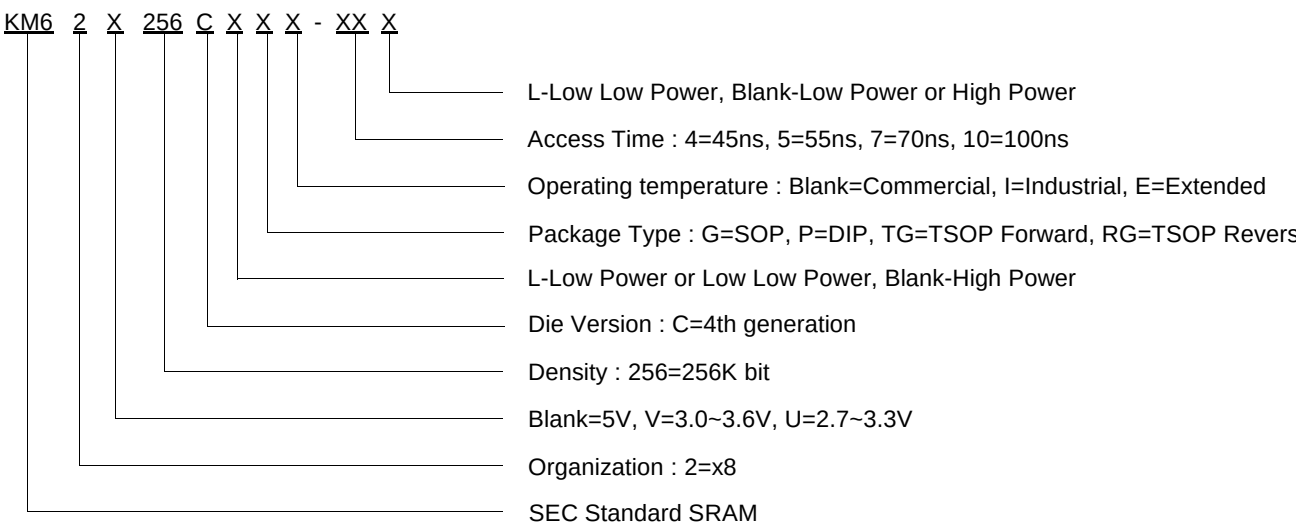
| Name                               | Function            |
|------------------------------------|---------------------|
| A <sub>0</sub> ~A <sub>14</sub>    | Address Inputs      |
| WE                                 | Write Enable Input  |
| CS                                 | Chip Select Input   |
| OE                                 | Output Enable Input |
| I/O <sub>1</sub> ~I/O <sub>8</sub> | Data Inputs/Outputs |
| V <sub>CC</sub>                    | Power(5V)           |
| V <sub>SS</sub>                    | Ground              |

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

| Commercial Temp Product<br>(0~70jE) |                         | Extended Temp Products<br>(-25~85jE) |                          | Industrial Temp Products<br>(-40~85jE) |                          |
|-------------------------------------|-------------------------|--------------------------------------|--------------------------|----------------------------------------|--------------------------|
| Part Name                           | Function                | Part Name                            | Function                 | Part Name                              | Function                 |
| KM62256CLP-4                        | 28-DIP, 45ns, L-pwr     | KM62256CLGE-7                        | 28-SOP, 70ns, L-pwr      | KM62256CLGI-7                          | 28-SOP, 70ns, L-pwr      |
| KM62256CLP-4L                       | 28-DIP, 45ns, LL-pwr    | KM62256CLGE-7L                       | 28-SOP, 70ns, LL-pwr     | KM62256CLGI-7L                         | 28-SOP, 70ns, LL-pwr     |
| KM62256CLP-5                        | 28-DIP, 55ns, L-pwr     | KM62256CLGE-10                       | 28-SOP, 100ns, L-pwr     | KM62256CLGI-10                         | 28-SOP, 100ns, L-pwr     |
| KM62256CLP-5L                       | 28-DIP, 55ns, LL-pwr    | KM62256CLGE-10L                      | 28-SOP, 100ns, LL-pwr    | KM62256CLGI-10L                        | 28-SOP, 100ns, LL-pwr    |
| KM62256CLP-7                        | 28-DIP, 70ns, L-pwr     | KM62256CLTGE-7                       | 28-TSOP F, 70ns, L-pwr   | KM62256CLTGI-7                         | 28-TSOP F, 70ns, L-pwr   |
| KM62256CLP-7L                       | 28-DIP, 70ns, LL-pwr    | KM62256CLTGE-7L                      | 28-TSOP F, 70ns, LL-pwr  | KM62256CLTGI-7L                        | 28-TSOP F, 70ns, LL-pwr  |
| KM62256CLG-4                        | 28-SOP, 45ns, L-pwr     | KM62256CLTGE-10                      | 28-TSOP F, 100ns, L-pwr  | KM62256CLTGI-10                        | 28-TSOP F, 100ns, L-pwr  |
| KM62256CLG-4L                       | 28-SOP, 45ns, LL-pwr    | KM62256CLTGE-10L                     | 28-TSOP F, 100ns, LL-pwr | KM62256CLTGI-10L                       | 28-TSOP F, 100ns, LL-pwr |
| KM62256CLG-5                        | 28-SOP, 50ns, L-pwr     | KM62256CLRGE-7                       | 28-TSOP R, 70ns, L-pwr   | KM62256CLRGI-7                         | 28-TSOP R, 70ns, L-pwr   |
| KM62256CLG-5L                       | 28-SOP, 50ns, LL-pwr    | KM62256CLRGE-7L                      | 28-TSOP R, 70ns, LL-pwr  | KM62256CLRGI-7L                        | 28-TSOP R, 70ns, LL-pwr  |
| KM62256CLG-7                        | 28-SOP, 70ns, L-pwr     | KM62256CLRGE-10                      | 28-TSOP R, 100ns, L-pwr  | KM62256CLRGI-10                        | 28-TSOP R, 100ns, L-pwr  |
| KM62256CLG-7L                       | 28-SOP, 70ns, LL-pwr    | KM62256CLRGE-10L                     | 28-TSOP R, 100ns, LL-pwr | KM62256CLRGI-10L                       | 28-TSOP R, 100ns, LL-pwr |
| KM62256CLTG-4                       | 28-TSOP F, 45ns, L-pwr  |                                      |                          |                                        |                          |
| KM62256CLTG-4L                      | 28-TSOP F, 45ns, LL-pwr |                                      |                          |                                        |                          |
| KM62256CLTG-5                       | 28-TSOP F, 55ns, L-pwr  |                                      |                          |                                        |                          |
| KM62256CLTG-5L                      | 28-TSOP F, 55ns, LL-pwr |                                      |                          |                                        |                          |
| KM62256CLTG-7                       | 28-TSOP F, 70ns, L-pwr  |                                      |                          |                                        |                          |
| KM62256CLTG-7L                      | 28-TSOP F, 70ns, LL-pwr |                                      |                          |                                        |                          |
| KM62256CLRG-4                       | 28-TSOP R, 45ns, L-pwr  |                                      |                          |                                        |                          |
| KM62256CLRG-4L                      | 28-TSOP R, 45ns, LL-pwr |                                      |                          |                                        |                          |
| KM62256CLRG-5                       | 28-TSOP R, 55ns, L-pwr  |                                      |                          |                                        |                          |
| KM62256CLRG-5L                      | 28-TSOP R, 55ns, LL-pwr |                                      |                          |                                        |                          |
| KM62256CLRG-7                       | 28-TSOP R, 70ns, L-pwr  |                                      |                          |                                        |                          |
| KM62256CLRG-7L                      | 28-TSOP R, 70ns, LL-pwr |                                      |                          |                                        |                          |

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS\*

| Item                                  | Symbol   | Ratings                  | Unit | Remark          |
|---------------------------------------|----------|--------------------------|------|-----------------|
| Voltage on any pin relative to Vss    | VIN,VOUT | -0.5 to Vcc+0.5          | V    | -               |
| Voltage on Vcc supply relative to Vss | VCC      | -0.5 to 7.0              | V    | -               |
| Power Dissipation                     | Pd       | 1.0                      | W    | -               |
| Storage temperature                   | TSTG     | -65 to 150               | °C   | -               |
| Operating Temperature                 | TA       | 0 to 70                  | °C   | KM62256CL/L-L   |
|                                       |          | -25 to 85                | °C   | KM62256CLE/LE-L |
|                                       |          | -40 to 85                | °C   | KM62256CLI/LI-L |
| Soldering temperature and time        | TSOLDER  | 260°C, 10sec (Lead Only) | -    | -               |

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS\*

| Item               | Symbol | Min     | Typ** | Max      | Unit |
|--------------------|--------|---------|-------|----------|------|
| Supply voltage     | Vcc    | 4.5     | 5.0   | 5.5      | V    |
| Ground             | Vss    | 0       | 0     | 0        | V    |
| Input high voltage | VIH    | 2.2     | -     | Vcc+0.5V | V    |
| Input low voltage  | VIL    | -0.5*** | -     | 0.8      | V    |

\* 1) Commercial Product : TA=0 to 70°C, unless otherwise specified  
2) Extended Product : TA=-25 to 85°C, unless otherwise specified  
3) Industrial Product : TA=-40 to 85°C, unless otherwise specified  
\*\* TA=25°C  
\*\*\* VIL(min)=-3.0V for tÂ 50ns pulse width

CAPACITANCE\* (f=1MHz, TA=25°C)

| Item                     | Symbol | Test Condition | Min | Max | Unit |
|--------------------------|--------|----------------|-----|-----|------|
| Input capacitance        | CIN    | VIN=0V         | -   | 6   | pF   |
| Input/Output capacitance | CIO    | VIO=0V         | -   | 8   | pF   |

\* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

| Item                           |                            | Symbol           | Test Conditions*                                                                                                                            |                 | Min | Typ** | Max    | Unit |
|--------------------------------|----------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-------|--------|------|
| Input leakage current          |                            | I <sub>LI</sub>  | V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>                                                                                         |                 | -1  | -     | 1      | §Ė   |
| Output leakage current         |                            | I <sub>LO</sub>  | $\overline{CS}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub><br>V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>                 |                 | -1  | -     | 1      | §Ė   |
| Operating power supply current |                            | I <sub>CC</sub>  | $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>IO</sub> =0mA                               |                 | -   | 7     | 15***  | mA   |
| Average operating current      |                            | I <sub>CC1</sub> | Cycle time=1§Ė 100% duty<br>$\overline{CS}$ Ė 0.2V, V <sub>IL</sub> Ė 0.2V<br>V <sub>IN</sub> ĖĖV <sub>CC</sub> -0.2V, I <sub>IO</sub> =0mA |                 | -   | -     | 7****  | mA   |
|                                |                            | I <sub>CC2</sub> | Min cycle, 100% duty<br>$\overline{CS}$ =V <sub>IL</sub> , I <sub>IO</sub> =0mA                                                             |                 | -   | -     | 70     | mA   |
| Output low voltage             |                            | V <sub>OL</sub>  | I <sub>OL</sub> =2.1mA                                                                                                                      |                 | -   | -     | 0.4    | V    |
| Output high voltage            |                            | V <sub>OH</sub>  | I <sub>OH</sub> =-1.0mA                                                                                                                     |                 | 2.4 | -     | -      | V    |
| Standby Current(TTL)           |                            | I <sub>SB</sub>  | $\overline{CS}$ =V <sub>IH</sub>                                                                                                            |                 | -   | -     | 1***** | mA   |
| Standby Current (CMOS)         | KM62256CL<br>KM62256CL-L   | I <sub>SB1</sub> | $\overline{CS}$ ĖĖV <sub>CC</sub> -0.2V<br>V <sub>IN</sub> ĖĖ 0.2V or<br>V <sub>IN</sub> ĖĖĖV <sub>CC</sub> -0.2V                           | L(Low Power)    | -   | 2     | 100    | §Ė   |
|                                |                            |                  |                                                                                                                                             | LL(L Low Power) | -   | 1     | 20     | §Ė   |
|                                | KM62256CLE<br>KM62256CLE-L |                  |                                                                                                                                             | L(Low Power)    | -   | -     | 100    | §Ė   |
|                                |                            |                  |                                                                                                                                             | LL(L Low Power) | -   | -     | 50     | §Ė   |
|                                | KM62256CLI<br>KM62256CLI-L |                  |                                                                                                                                             | L(Low Power)    | -   | -     | 100    | §Ė   |
|                                |                            |                  |                                                                                                                                             | LL(L Low Power) | -   | -     | 50     | §Ė   |

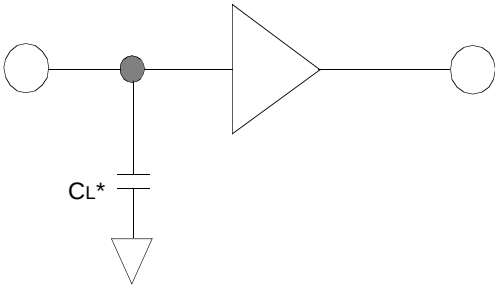
\* 1) Commercial Product : T<sub>A</sub>=0 to 70Ė, V<sub>CC</sub>=5VĖĖ10% unless otherwise specified  
 2) Extended Product : T<sub>A</sub>=-25 to 85Ė, V<sub>CC</sub>=5VĖĖ10% nless otherwise specified  
 3) Industrial Product : T<sub>A</sub>=-40 to 85Ė, V<sub>CC</sub>=5VĖĖ10% unless otherwise specified  
 \*\* T<sub>A</sub>=25Ė  
 \*\*\* 20mA for Extended and Industrial Products  
 \*\*\*\*10mA for Extended and Industrial Products  
 \*\*\*\*\*2mA for Extended and Industrial Products

A.C CHARACTERISTICS

TEST CONDITIONS(1.Test Load and Test Input/Output Reference)\*

| Item                               | Value                       | Remark |
|------------------------------------|-----------------------------|--------|
| Input pulse level                  | 0.8 to 2.4V                 | -      |
| Input rising & falling time        | 5ns                         | -      |
| input and output reference voltage | 1.5V                        | -      |
| Output load (See right)            | C <sub>L</sub> =100pF+1TTL  | -      |
|                                    | **C <sub>L</sub> =30pF+1TTL | -      |

\* See DC Operating conditions  
 \*\* Test load for 45ns commercial products



\* Including scope and jig capacitance

KM62256C Family

CMOS SRAM

TEST CONDITIONS(2. Temperature and Vcc Conditions)

| Product Family  | Temperature | Power Supply(Vcc) | Speed Bin   | Comments   |
|-----------------|-------------|-------------------|-------------|------------|
| KM62256CL/L-L   | 0~70℃       | 5V ±10%           | 45*/55/70ns | Commercial |
| KM62256CLE/LE-L | -25~85℃     | 5V ±10%           | 70/100ns    | Extended   |
| KM62256CLI/LI-L | -40~85℃     | 5V ±10%           | 70/100ns    | Industrial |

\* The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

| Parameter List |                                 | Symbol | Speed Bins |     |      |     |      |     |       |     | Units |
|----------------|---------------------------------|--------|------------|-----|------|-----|------|-----|-------|-----|-------|
|                |                                 |        | 45ns*      |     | 55ns |     | 70ns |     | 100ns |     |       |
|                |                                 |        | Min        | Max | Min  | Max | Min  | Max | Min   | Max |       |
| Read           | Read cycle time                 | tRC    | 45         | -   | 55   | -   | 70   | -   | 100   | -   | ns    |
|                | Address access time             | tAA    | -          | 45  | -    | 55  | -    | 70  | -     | 100 | ns    |
|                | Chip select to output           | tCO    | -          | 45  | -    | 55  | -    | 70  | -     | 100 | ns    |
|                | Output enable to valid output   | tOE    | -          | 25  | -    | 25  | -    | 35  | -     | 50  | ns    |
|                | Chip select to low-Z output     | tLZ    | 10         | -   | 10   | -   | 10   | -   | 10    | -   | ns    |
|                | Output enable to low-Z output   | tOLZ   | 5          | -   | 5    | -   | 5    | -   | 5     | -   | ns    |
|                | Chip disable to high-Z output   | tHZ    | 0          | 20  | 0    | 20  | 0    | 30  | 0     | 35  | ns    |
|                | Output disable to high-Z output | tOHZ   | 0          | 20  | 0    | 20  | 0    | 30  | 0     | 35  | ns    |
|                | Output hold from address change | tOH    | 5          | -   | 5    | -   | 5    | -   | 5     | -   | ns    |
| Write          | Write cycle time                | tWC    | 45         | -   | 55   | -   | 70   | -   | 100   | -   | ns    |
|                | Chip select to end of write     | tCW    | 45         | -   | 45   | -   | 60   | -   | 80    | -   | ns    |
|                | Address set-up time             | tAS    | 0          | -   | 0    | -   | 0    | -   | 0     | -   | ns    |
|                | Address valid to end of write   | tAW    | 45         | -   | 45   | -   | 60   | -   | 80    | -   | ns    |
|                | Write pulse width               | tWP    | 40         | -   | 40   | -   | 50   | -   | 60    | -   | ns    |
|                | Write recovery time             | tWR    | 0          | -   | 0    | -   | 0    | -   | 0     | -   | ns    |
|                | Write to output high-Z          | tWHZ   | 0          | 20  | 0    | 20  | 0    | 25  | 0     | 35  | ns    |
|                | Data to write time overlap      | tDW    | 25         | -   | 25   | -   | 30   | -   | 50    | -   | ns    |
|                | Data hold from write time       | tDH    | 0          | -   | 0    | -   | 0    | -   | 0     | -   | ns    |
|                | End write to output low-Z       | tOW    | 5          | -   | 5    | -   | 5    | -   | 5     | -   | ns    |

\* The parameter is measured with 30pF test load

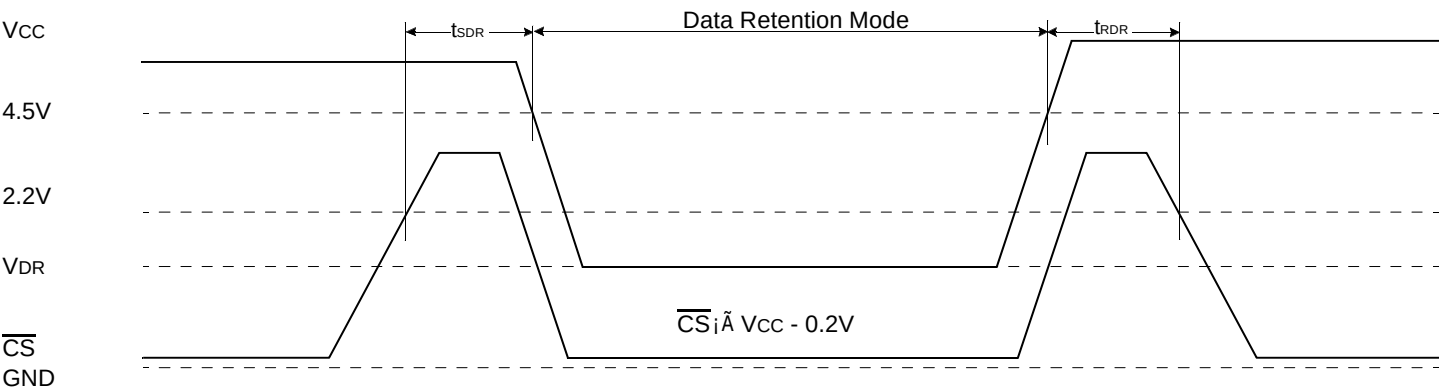
DATA RETENTION CHARACTERISTICS

| Item                       | Symbol |                            | Test Condition*                                             |                 | Min    | Typ**    | Max      | Unit    |
|----------------------------|--------|----------------------------|-------------------------------------------------------------|-----------------|--------|----------|----------|---------|
| Vcc for data retention     | VDR    |                            | $\overline{CS}_i \nrightarrow V_{cc}-0.2V$                  |                 | 2.0    | -        | 5.5      | V       |
| Data retention current     | IDR    | KM62256CL<br>KM62256CL-L   | $V_{cc}=3.0V$<br>$\overline{CS}_i \nrightarrow V_{cc}-0.2V$ | L-Ver<br>LL-Ver | -<br>- | 1<br>0.5 | 50<br>10 | $\mu A$ |
|                            |        | KM62256CLE<br>KM62256CLE-L |                                                             | L-Ver<br>LL-Ver | -<br>- | -<br>-   | 50<br>25 |         |
|                            |        | KM62256CLI<br>KM62256CLI-L |                                                             | L-Ver<br>LL-Ver | -<br>- | -<br>-   | 50<br>25 |         |
| Data retention set-up time | tSDR   |                            | See data retention waveform                                 |                 | 0      | -        | -        | ms      |
| Recovery time              | tRDR   |                            |                                                             |                 | 5      | -        | -        |         |

\* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified  
2) Extended Product : Ta=-25 to 85℃, unless otherwise specified  
3) Industrial Product : Ta=-40 to 85℃, unless otherwise specified  
\*\* TA=25℃

DATA RETENTION WAVE FORM

1)  $\overline{CS}$  Controlled



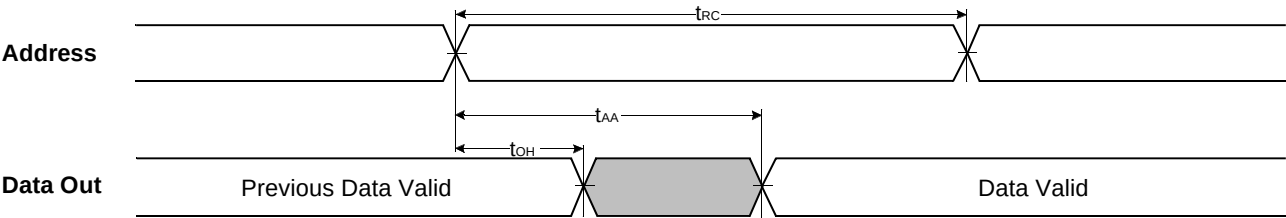
FUNCTIONAL DESCRIPTION

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Mode           | I/O Pin | Current Mode |
|-----------------|-----------------|-----------------|----------------|---------|--------------|
| H               | X               | X               | Power Down     | High-Z  | ISB ISB1     |
| L               | H               | H               | Output Disable | High-Z  | ICC          |
| L               | H               | L               | Read           | Dout    | ICC          |
| L               | L               | X               | Write          | Din     | ICC          |

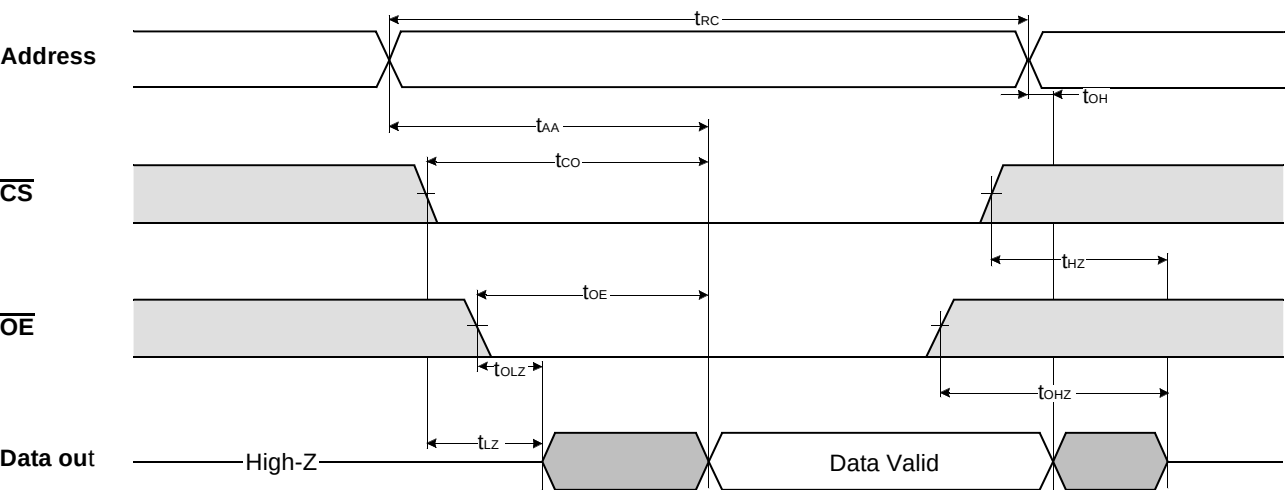
\* X means don't care

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1)Address Controlled)  
(CS=OE=VIL, WE=VIH)



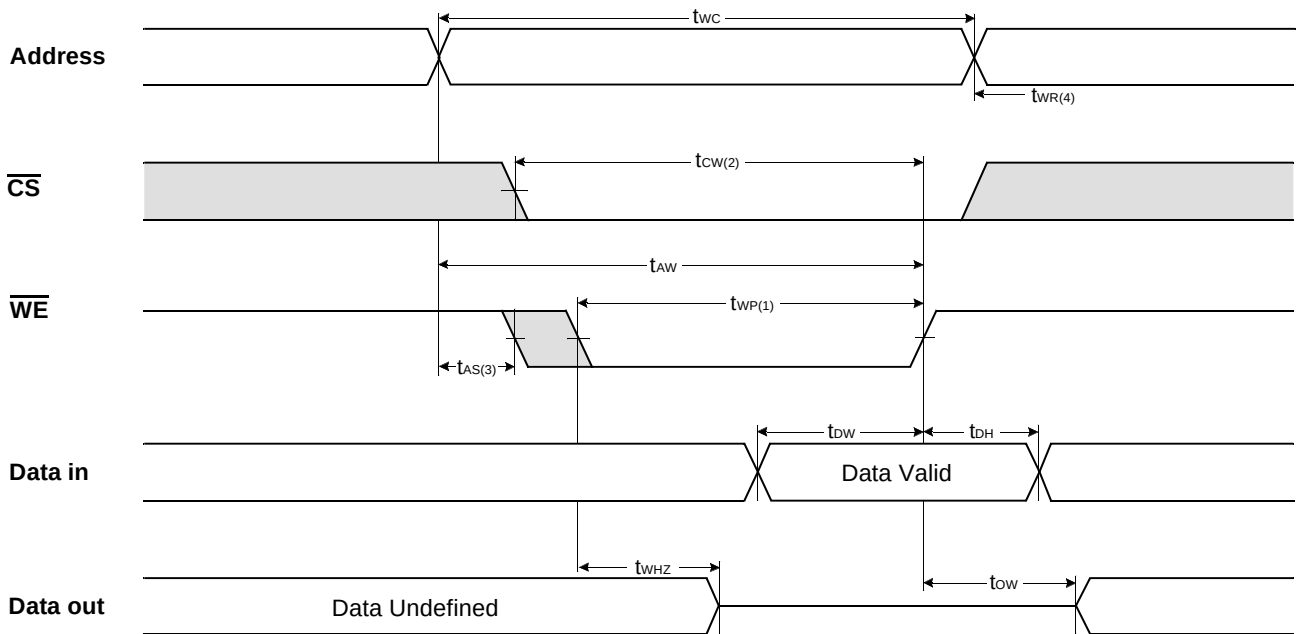
TIMING WAVEFORM OF READ CYCLE(2) $\overline{WE}=VIH$



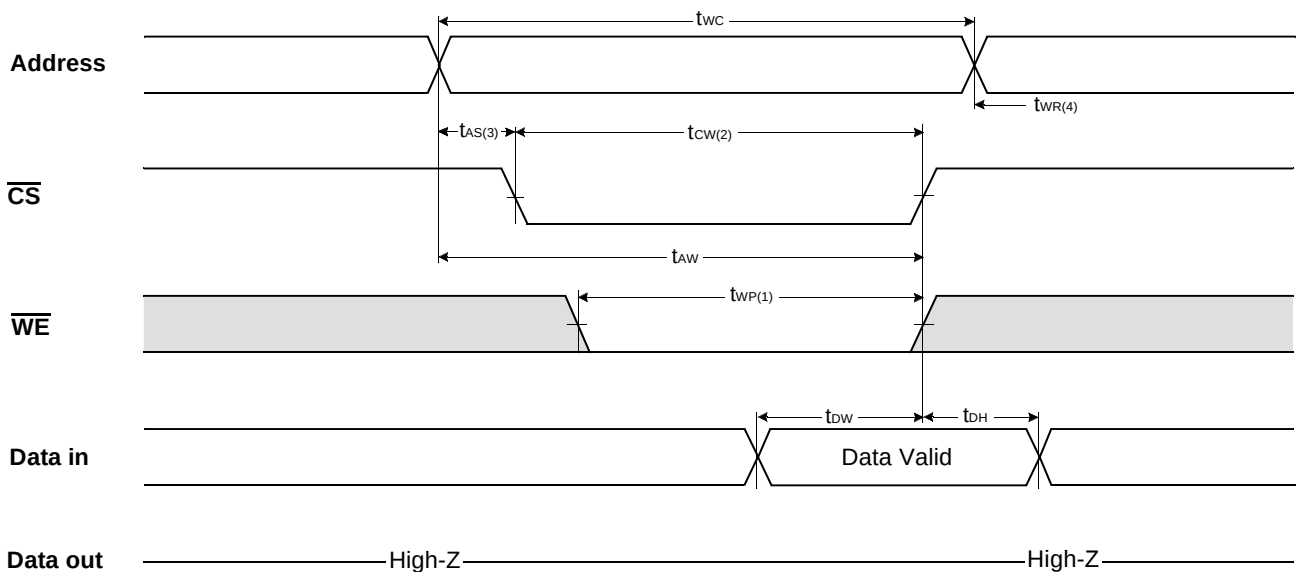
NOTES (READ CYCLE)

- 1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition,  $t_{HZ}(\text{max.})$  is less than  $t_{LZ}(\text{min.})$  both for a given device and from device to device.

## TIMING WAVEFORM OF WRITE CYCLE(1) $\overline{WE}$ Controlled



## TIMING WAVEFORM OF WRITE CYCLE(2) $\overline{CS}$ Controlled



### NOTES (WRITE CYCLE)

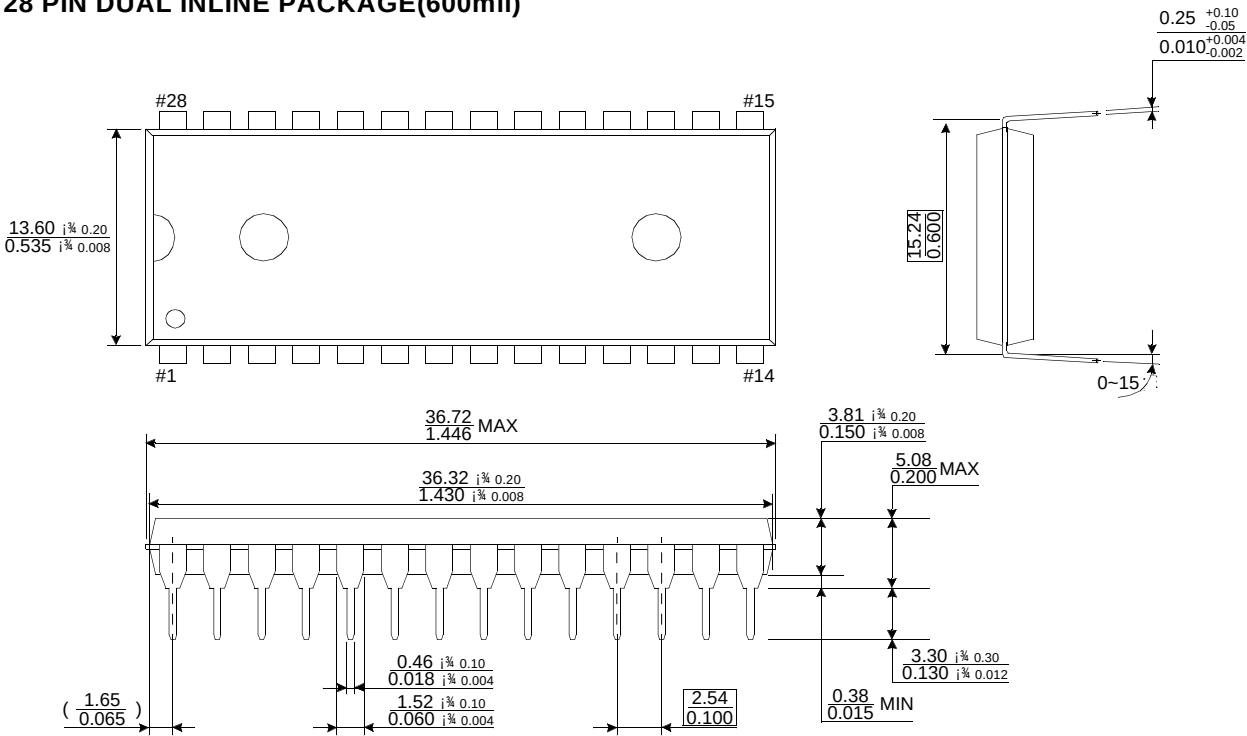
1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  goes low and  $\overline{WE}$  going low : A write end at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.



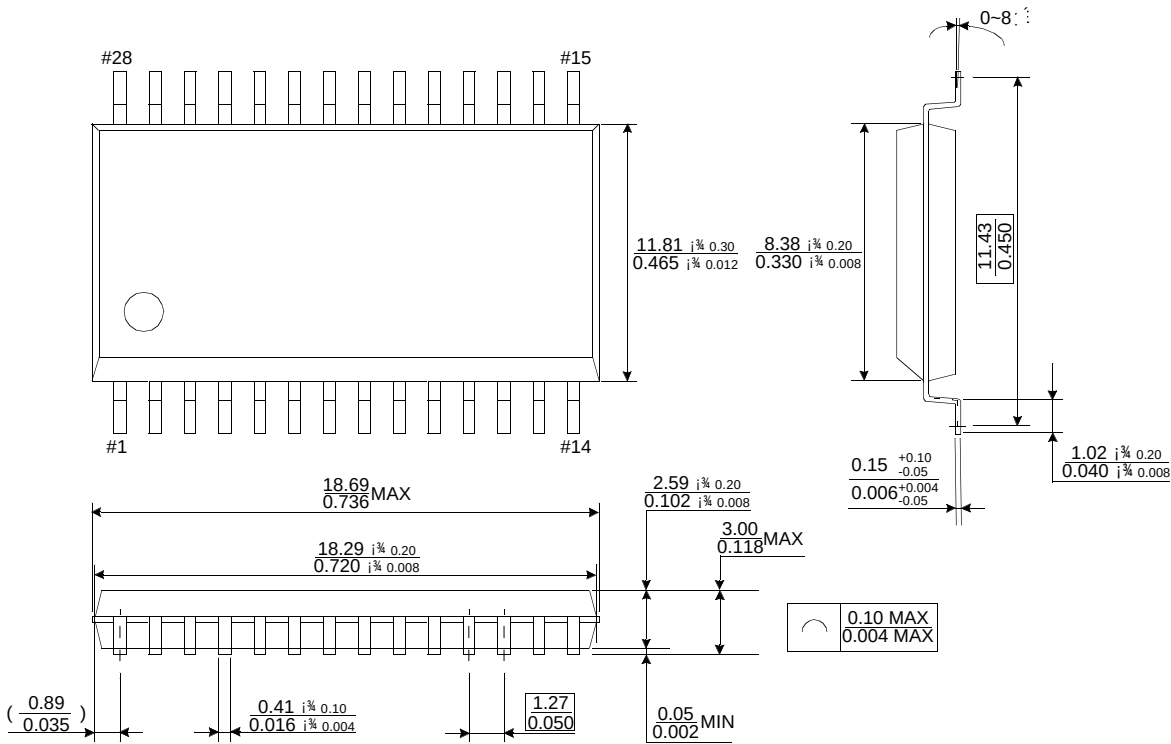
**PACKAGE DIMENSIONS**

Units :Millimeters(Inches )

28 PIN DUAL INLINE PACKAGE(600mil)



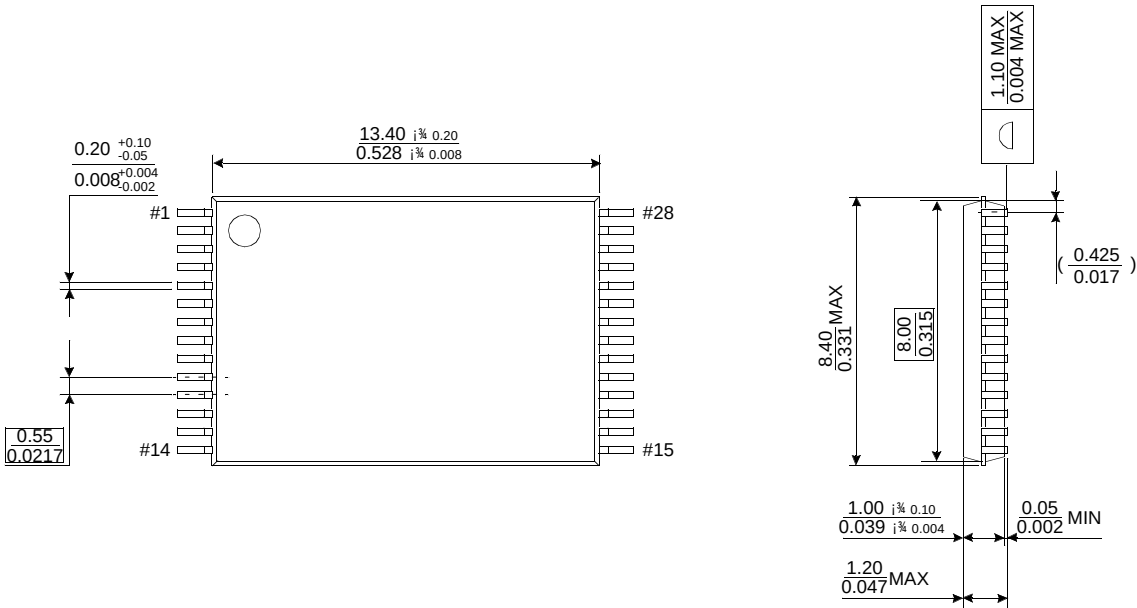
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



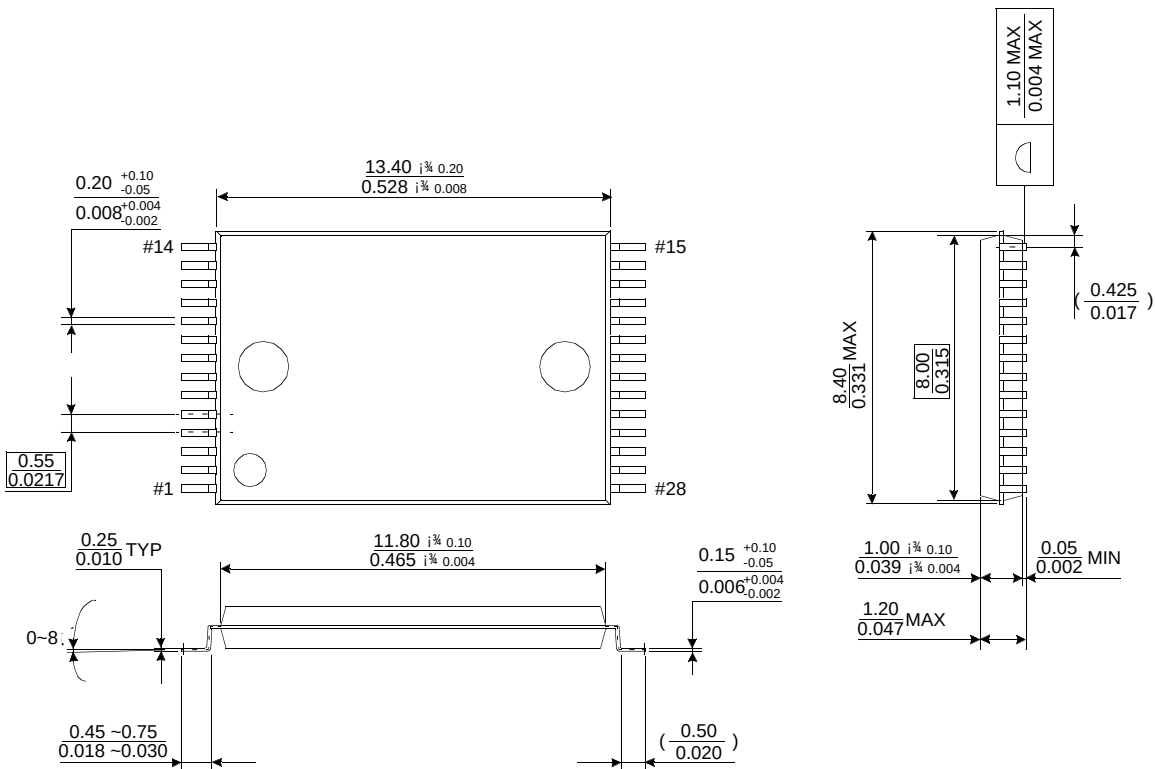
PACKAGE DIMENSIONS

Units :Millimeters(Inches )

28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)



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